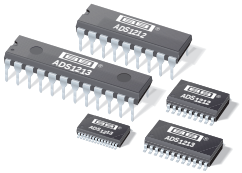


ADS1212
ADS1213

SBAS064B – JANUARY 1996 – REVISED FEBRUARY 2004

22-Bit ANALOG-TO-DIGITAL CONVERTER

FEATURES

- DELTA-SIGMA A/D CONVERTER
- 22 BITS NO MISSING CODES
- 20 BITS EFFECTIVE RESOLUTION AT 10Hz AND 16 BITS AT 1000Hz
- LOW POWER: 1.4mW
- DIFFERENTIAL INPUTS
- PROGRAMMABLE GAIN AMPLIFIER
- SPI™ COMPATIBLE SSI INTERFACE
- PROGRAMMABLE CUTOFF FREQUENCY UP TO 6.25kHz
- INTERNAL/EXTERNAL REFERENCE
- ON-CHIP SELF-CALIBRATION
- ADS1213 INCLUDES 4-CHANNEL MUX

APPLICATIONS

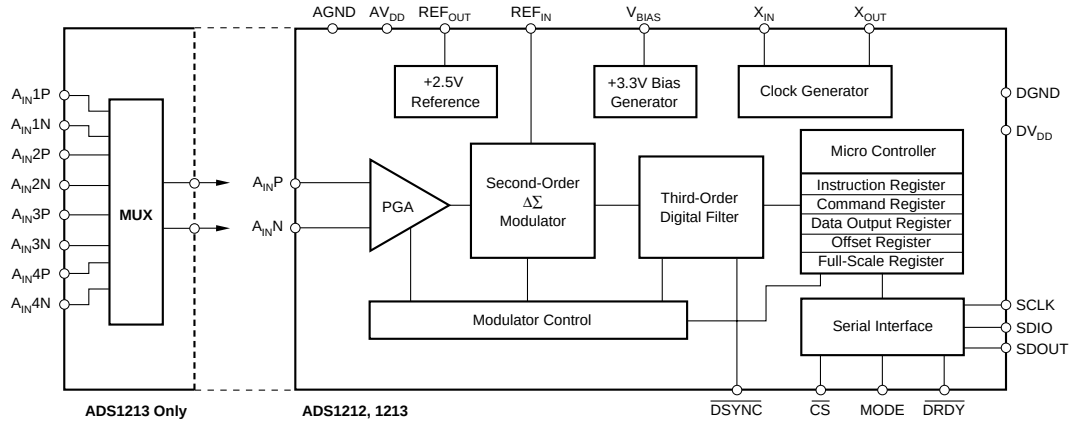
- INDUSTRIAL PROCESS CONTROL
- INSTRUMENTATION
- BLOOD ANALYSIS
- SMART TRANSMITTERS
- PORTABLE INSTRUMENTS
- WEIGH SCALES
- PRESSURE TRANSDUCERS

DESCRIPTION

The ADS1212 and ADS1213 are precision, wide dynamic range, delta-sigma Analog-to-Digital (A/D) converters with 24-bit resolution operating from a single +5V supply. The differential inputs are ideal for direct connection to transducers or low-level voltage signals. The delta-sigma architecture is used for wide dynamic range and to ensure 22 bits of no-missing-code performance. An effective resolution of 20 bits is achieved through the use of a very low-noise input amplifier at conversion rates up to 10Hz. Effective resolutions of 16 bits can be maintained up to a sample rate of 1kHz through the use of the unique Turbo Modulator mode of operation. The dynamic range of the converters is further increased by providing a low-noise programmable gain amplifier with a gain range of 1 to 16 in binary steps.

The ADS1212 and ADS1213 are designed for high-resolution measurement applications in smart transmitters, industrial process control, weigh scales, chromatography and portable instrumentation. Both converters include a flexible synchronous serial interface that is SPI compatible and also offers a two-wire control mode for low-cost isolation.

The ADS1212 is a single channel converter and is offered in both DIP-18 and SO-18 packages. The ADS1213 includes a 4-channel input multiplexer and is available in DIP-24, SO-24, and SSOP-28 packages.



PATENTS PENDING

SPECIFICATIONS

All specifications T_{MIN} to T_{MAX}, AV_{DD} = DV_{DD} = +5V, f_{XIN} = 1MHz, programmable gain amplifier setting of 1, Turbo Mode Rate of 1, REF_{OUT} disabled, V_{BIAS} disabled, and external 2.5V reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS1212U, P/ADS1213U, P, E MIN	TYP	MAX	UNITS
ANALOG INPUT					
Input Voltage Range[1]		0		+5	V
	With V_{BIAS}[2]	–10		+10	V
Input Impedance	G = Gain, TMR = Turbo Mode Rate		20/(G • TMR)[3]		MΩ
Programmable Gain Amplifier	User Programmable: 1, 2, 4, 8, or 16	1		16	
Input Capacitance			5		pF
Input Leakage Current	At +25°C		5	50	pA
	T_{MIN} to T_{MAX}			1	nA
SYSTEMS PERFORMANCE					
No Missing Codes	f_{DATA} = 10Hz	22			Bits
	f_{DATA} = 60Hz	19			Bits
	f_{DATA} = 100Hz, TMR of 4	21			Bits
	f_{DATA} = 250Hz, TMR of 8	20			Bits
	f_{DATA} = 500Hz, TMR of 16	20			Bits
	f_{DATA} = 1000Hz, TMR of 16	18			Bits
Integral Linearity	f_{DATA} = 60Hz			±0.0015	%FSR
	f_{DATA} = 1000Hz, TMR of 16			±0.0015	%FSR
Integral Linearity (Single-Ended)			0.01		%FSR
Unipolar Offset Error[4]			See Note 5		
Unipolar Offset Drift[6]			1		ppm/°C
Gain Error[4]			See Note 5		
Gain Error Drift[6]			4		ppm/°C
Common-Mode Rejection[9]	At DC, T_{MIN} to T_{MAX}	90	100		dB
	50Hz, f_{DATA} = 50Hz[7]	160			dB
	60Hz, f_{DATA} = 60Hz[7]	160			dB
Normal-Mode Rejection	50Hz, f_{DATA} = 50Hz[7]	100			dB
	60Hz, f_{DATA} = 60Hz[7]	100			dB
Output Noise		See Typical Performance Curves			
Power Supply Rejection	DC, 50Hz, and 60Hz	60			dB
VOLTAGE REFERENCE					
Internal Reference (REF_{OUT})		2.4	2.5	2.6	V
Drift			25		ppm/°C
Noise			50		µVp-p
Load Current	Source or Sink			1	mA
Output Impedance			2		Ω
External Reference (REF_{IN})		2.0		3.0	V
Load Current				2.5	µA
V_{BIAS} Output	Using Internal Reference	3.15	3.3	3.45	V
Drift			50		ppm/°C
Load Current	Source or Sink			10mA	
DIGITAL INPUT/OUTPUT					
Logic Family			TTL Compatible CMOS		
Logic Level: (all except X_{IN})					
V_{IH}	I_{IH} = +5µA	2.0		DV_{DD} +0.3	V
V_{IL}	I_{IL} = +5µA	–0.3		0.8	V
V_{OH}	I_{OH} = 2 TTL Loads	2.4			V
V_{OL}	I_{OL} = 2 TTL Loads			0.4	V
X_{IN} Input Levels: V_{IH}		3.5		DV_{DD} +0.3	V
V_{IL}		–0.3		0.8	V
X_{IN} Frequency Range (f_{XIN})		0.5		2.5	MHz
Output Data Rate (f_{DATA})	User Programmable and TMR = 1 to 16	0.96		6,250	Hz
	f_{XIN} = 500kHz	0.48		3,125	Hz
	f_{XIN} = 2.5MHz	2.4		15,625	Hz
Data Format	User Programmable		Two's Complement or Offset Binary		
SYSTEM CALIBRATION					
Offset and Full-Scale Limits	V_{FS} = Full-Scale Differential Voltage[8]	0.7 • (2 • REF_{IN})/G			
V_{FS} – | V_{OS} |	V_{OS} = Offset Differential Voltage[8]			1.3 • (2 • REF_{IN})/G	

SPECIFICATIONS (Cont.)

All specifications T_{MIN} to T_{MAX}, AV_{DD} = DV_{DD} = +5V, f_{XIN} = 1MHz, programmable gain amplifier setting of 1, Turbo Mode Rate of 1, REF_{OUT} disabled, V_{BIAS} disabled, and external 2.5V reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS1212U, P/ADS1213U, P, E			UNITS
		MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS					
Power Supply Voltage		4.75		5.25	V
Power Supply Current:					
Analog Current			95		µA
Digital Current			185		µA
Additional Analog Current with					
REF_{OUT} Enabled			1.8		mA
V_{BIAS} Enabled	No Load		1		mA
Power Dissipation	At +25°C		1.4		mW
	T_{MIN} to T_{MAX}			1.8	mW
	TMR of 16		6	8.5	mW
	f_{XIN} = 2.5MHz		2.2		mW
	f_{XIN} = 2.5MHz, TMR of 16		7.5		mW
	Sleep Mode		0.45		mW
TEMPERATURE RANGE					
Specified		–40		+85	°C
Storage		–60		+125	°C

NOTES: (1) In order to achieve the converter's full-scale range, the input must be fully differential ($A_{IN}N = 2 \cdot REF_{IN} – A_{IN}P$). If the input is single-ended ($A_{IN}N$ or $A_{IN}P$ is fixed), then the full-scale range is one-half that of the differential range. (2) This range is set with external resistors and V_{BIAS} (as described in the text). Other ranges are possible. (3) Input impedance is higher with lower f_{XIN}. (4) Applies after calibration. (5) After system calibration, these errors will be of the order of the effective resolution of the converter. Refer to the Typical Performance Curves which apply to the desired mode of operation. (6) Recalibration can remove these errors. (7) The specification also applies at f_{DATA}/i, where i is 2, 3, 4, etc. (8) Voltages at the analog inputs must remain within AGND to AV_{DD}. (9) The common-mode rejection test is performed with 100mV differential input.

ABSOLUTE MAXIMUM RATINGS

Analog Input: Current	±100mA, Momentary
	±10mA, Continuous
Voltage	AGND –0.3V to AV_{DD} +0.3V
AV_{DD} to DV_{DD}	–0.3V to 6V
AV_{DD} to AGND	–0.3V to 6V
DV_{DD} to DGND	–0.3V to 6V
AGND to DGND	±0.3V
REF_{IN} Voltage to AGND	–0.3V to AV_{DD} +0.3V
Digital Input Voltage to DGND	–0.3V to DV_{DD} +0.3V
Digital Output Voltage to DGND	–0.3V to DV_{DD} +0.3V
Lead Temperature (soldering, 10s)	+300°C
Power Dissipation (Any package)	500mW

PACKAGE/ORDERING INFORMATION

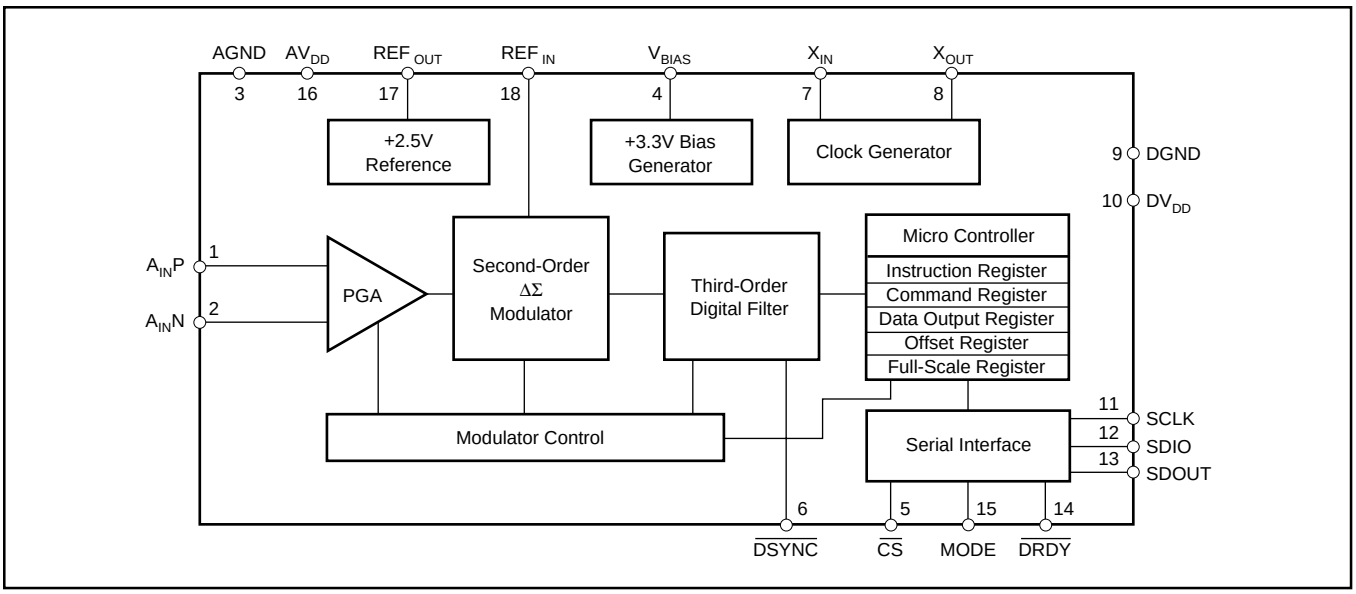
For the latest package and ordering information, see the Package Option Addendum located at the end of this data sheet.

ELECTROSTATIC DISCHARGE SENSITIVITY

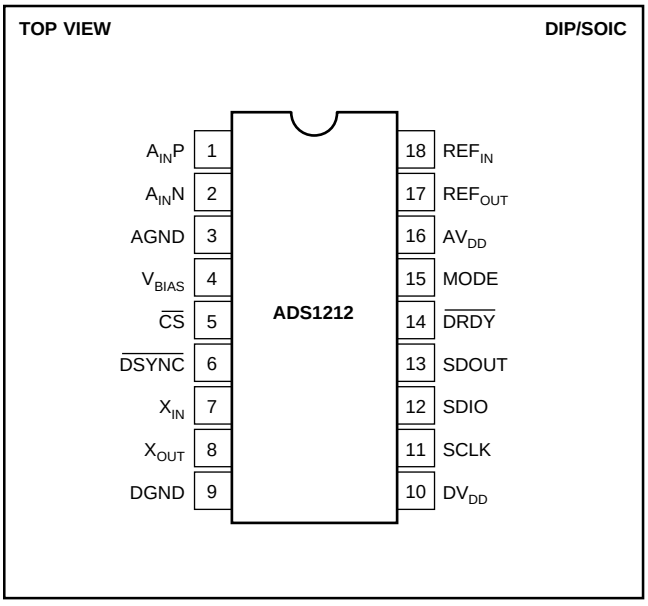
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ADS1212 SIMPLIFIED BLOCK DIAGRAM



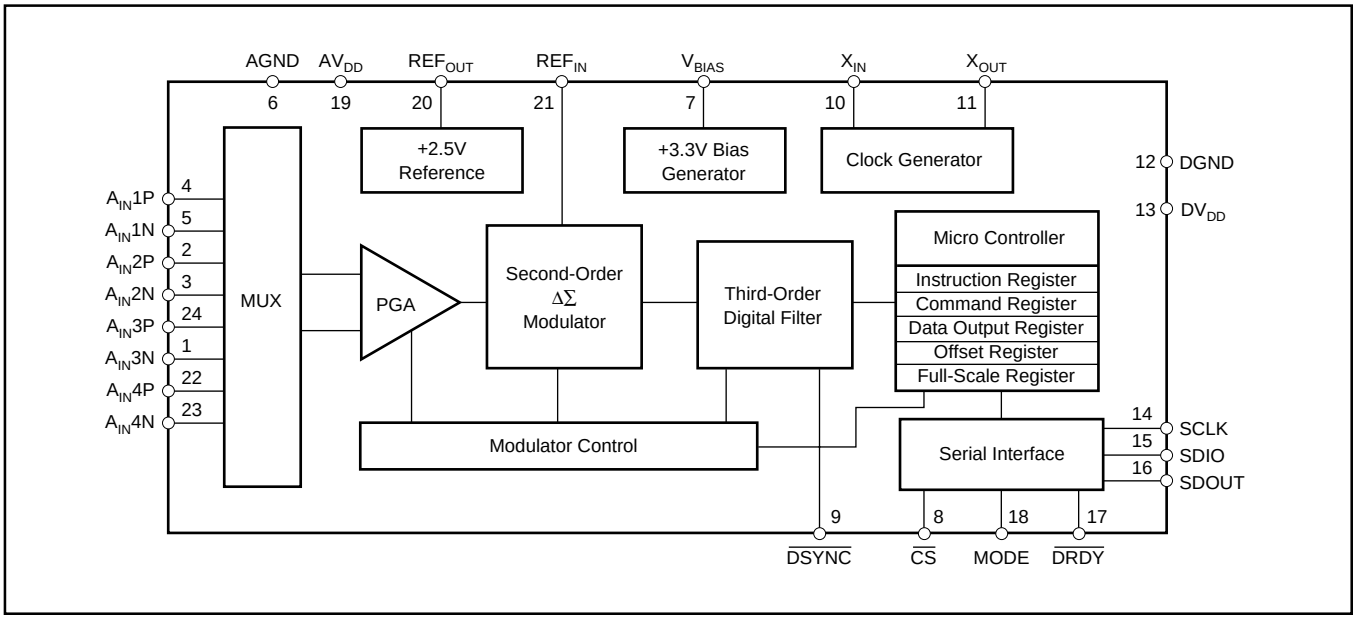
ADS1212 PIN CONFIGURATION



ADS1212 PIN DEFINITIONS

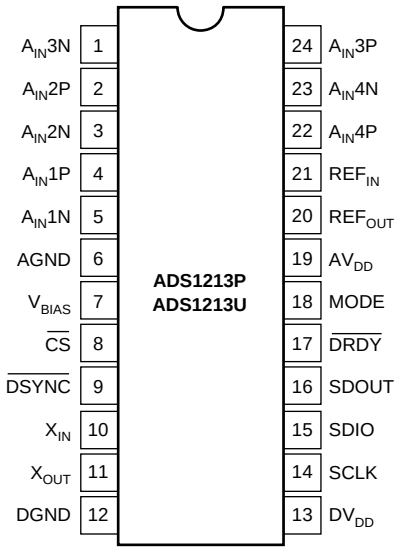
PIN NO	NAME	DESCRIPTION
1	$A_{IN}P$	Noninverting Input.
2	$A_{IN}N$	Inverting Input.
3	AGND	Analog Ground.
4	V_{BIAS}	Bias Voltage Output, +3.3V nominal.
5	$\overline{CS}$	Chip Select Input.
6	$\overline{DSYNC}$	Control Input to Synchronize Serial Output Data.
7	X_{IN}	System Clock Input.
8	X_{OUT}	System Clock Output.
9	DGND	Digital Ground.
10	DV_{DD}	Digital Supply, +5V nominal.
11	SCLK	Clock Input/Output for serial data transfer.
12	SDIO	Serial Data Input (can also function as Serial Data Output).
13	SDOUT	Serial Data Output.
14	$\overline{DRDY}$	Data Ready.
15	MODE	SCLK Control Input (Master = 1, Slave = 0).
16	AV_{DD}	Analog Supply, +5V nominal.
17	REF_{OUT}	Reference Output, +2.5V nominal.
18	REF_{IN}	Reference Input.

ADS1213 SIMPLIFIED BLOCK DIAGRAM



ADS1213P AND ADS1213U PIN CONFIGURATION

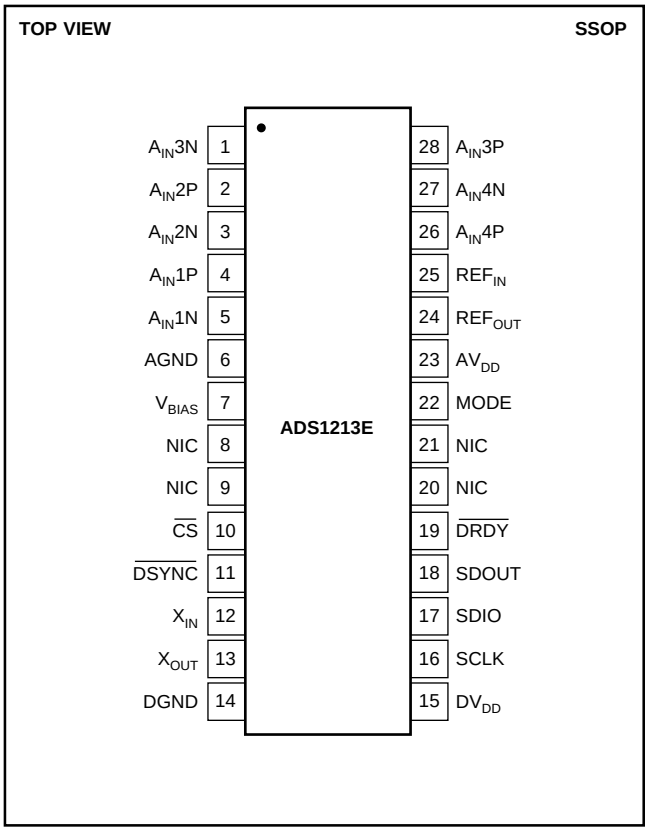
TOP VIEW **DIP/SOIC**



ADS1213P AND ADS1213U PIN DEFINITIONS

PIN NO	NAME	DESCRIPTION
1	$A_{IN}3N$	Inverting Input Channel 3.
2	$A_{IN}2P$	Noninverting Input Channel 2.
3	$A_{IN}2N$	Inverting Input Channel 2.
4	$A_{IN}1P$	Noninverting Input Channel 1.
5	$A_{IN}1N$	Inverting Input Channel 1.
6	AGND	Analog Ground.
7	V_{BIAS}	Bias Voltage Output, +3.3V nominal.
8	$\overline{CS}$	Chip Select Input.
9	$\overline{DSYNC}$	Control Input to Synchronize Serial Output Data.
10	X_{IN}	System Clock Input.
11	X_{OUT}	System Clock Output.
12	DGND	Digital Ground.
13	DV_{DD}	Digital Supply, +5V nominal.
14	SCLK	Clock Input/Output for serial data transfer.
15	SDIO	Serial Data Input (can also function as Serial Data Output).
16	SDOUT	Serial Data Output.
17	$\overline{DRDY}$	Data Ready.
18	MODE	SCLK Control Input (Master = 1, Slave = 0).
19	AV_{DD}	Analog Supply, +5V nominal.
20	REF_{OUT}	Reference Output: +2.5V nominal.
21	REF_{IN}	Reference Input.
22	$A_{IN}4P$	Noninverting Input Channel 4.
23	$A_{IN}4N$	Inverting Input Channel 4.
24	$A_{IN}3P$	Noninverting Input Channel 3.

ADS1213E PIN CONFIGURATION



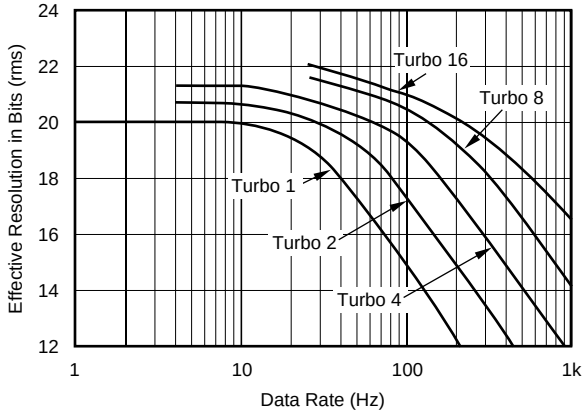
ADS1213E PIN DEFINITIONS

PIN NO	NAME	DESCRIPTION
1	$A_{IN}3N$	Inverting Input Channel 3.
2	$A_{IN}2P$	Noninverting Input Channel 2.
3	$A_{IN}2N$	Inverting Input Channel 2.
4	$A_{IN}1P$	Noninverting Input Channel 1.
5	$A_{IN}1N$	Inverting Input Channel 1.
6	AGND	Analog Ground.
7	V_{BIAS}	Bias Voltage Output, +3.3V nominal.
8	NIC	Not Internally Connected.
9	NIC	Not Internally Connected.
10	$\overline{CS}$	Chip Select Input.
11	$\overline{DSYNC}$	Control Input to Synchronize Serial Output Data.
12	X_{IN}	System Clock Input.
13	X_{OUT}	System Clock Output.
14	DGND	Digital Ground.
15	DV_{DD}	Digital Supply, +5V nominal.
16	SCLK	Clock Input/Output for serial data transfer.
17	SDIO	Serial Data Input (can also function as Serial Data Output).
18	SDOUT	Serial Data Output.
19	$\overline{DRDY}$	Data Ready.
20	NIC	Not Internally Connected.
21	NIC	Not Internally Connected.
22	MODE	SCLK Control Input (Master = 1, Slave = 0).
23	AV_{DD}	Analog Supply, +5V nominal.
24	REF_{OUT}	Reference Output: +2.5V nominal.
25	REF_{IN}	Reference Input.
26	$A_{IN}4P$	Noninverting Input Channel 4.
27	$A_{IN}4N$	Inverting Input Channel 4.
28	$A_{IN}3P$	Noninverting Input Channel 3.

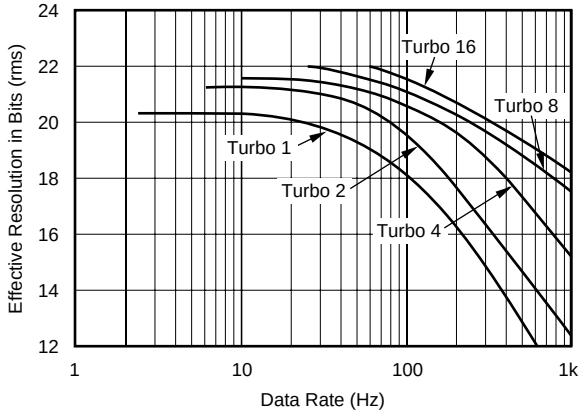
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, AV_{DD} = DV_{DD} = +5V, f_{XIN} = 1MHz, programmable gain amplifier setting of 1, Turbo Mode Rate of 1, REF_{OUT} disabled, V_{BIAS} disabled, and external 2.5V reference, unless otherwise noted.

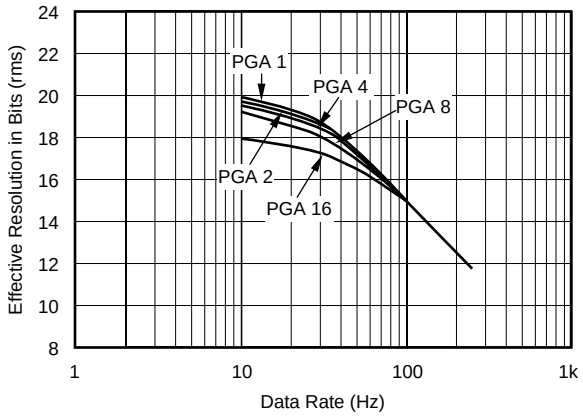
EFFECTIVE RESOLUTION vs DATA RATE
(1MHz Clock)



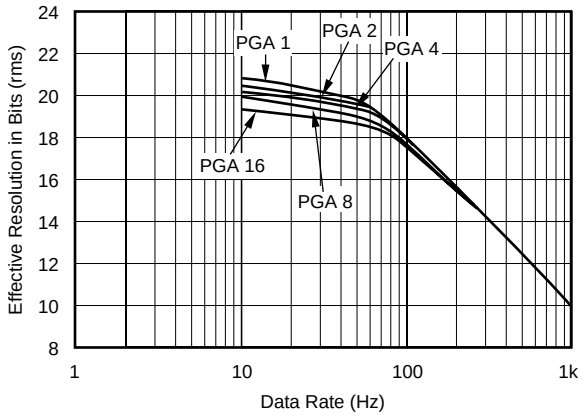
EFFECTIVE RESOLUTION vs DATA RATE
(2.5MHz Clock)



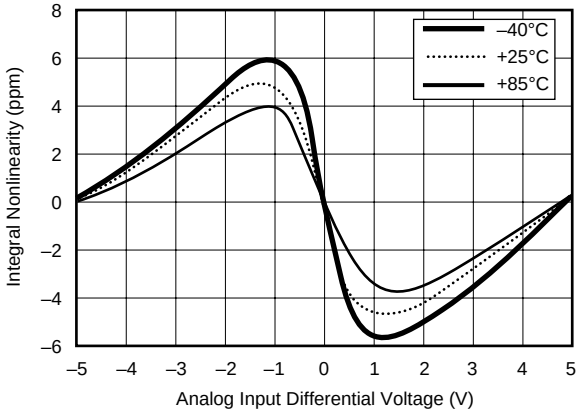
EFFECTIVE RESOLUTION vs DATA RATE
(1MHz Clock)



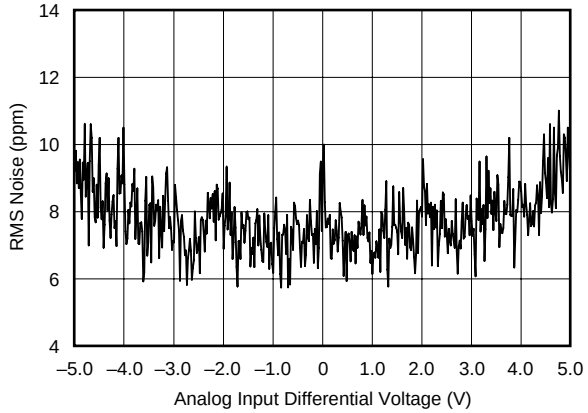
EFFECTIVE RESOLUTION vs DATA RATE
(2.5MHz Clock)



LINEARITY vs TEMPERATURE
(60Hz Data Rate)



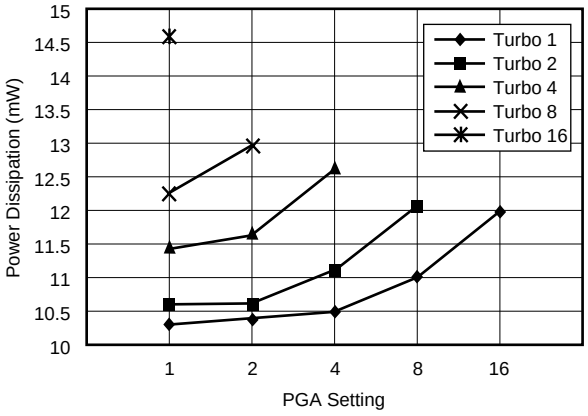
RMS NOISE vs INPUT VOLTAGE LEVEL
(60Hz Data Rate)



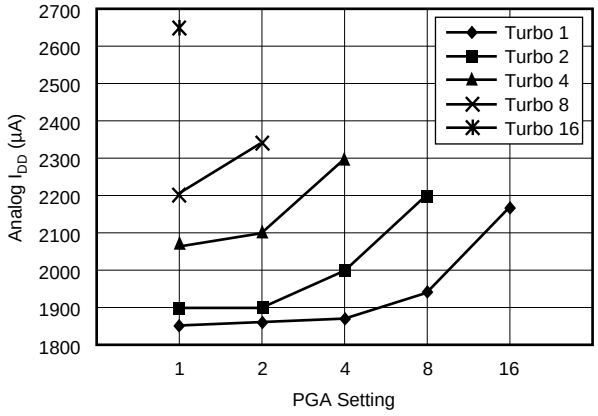
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, AV_{DD} = DV_{DD} = +5V, f_{XIN} = 1MHz, programmable gain amplifier setting of 1, Turbo Mode Rate of 1, REF_{OUT} disabled, V_{BIAS} disabled, and external 2.5V reference, unless otherwise noted.

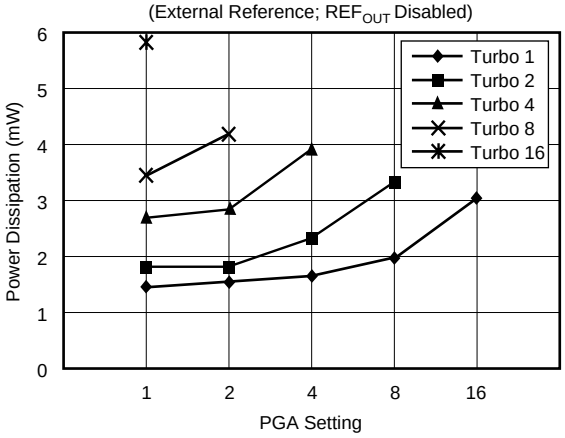
POWER DISSIPATION vs PGA SETTING
(REF_{OUT} Enabled)



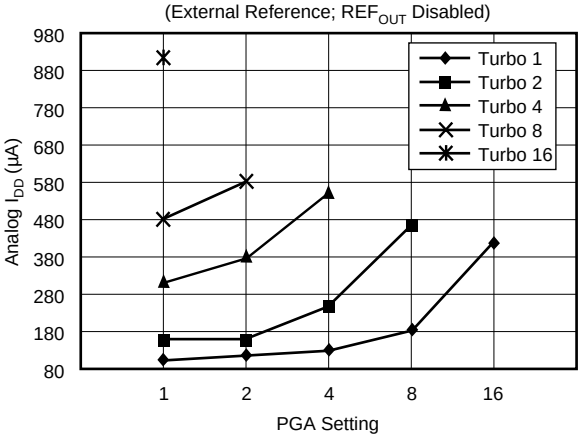
ANALOG CURRENT vs PGA SETTING
(REF_{OUT} Enabled)



POWER DISSIPATION vs PGA SETTING
(External Reference; REF_{OUT} Disabled)



ANALOG CURRENT vs PGA SETTING
(External Reference; REF_{OUT} Disabled)



THEORY OF OPERATION

The ADS1212 and ADS1213 are precision, high dynamic range, self-calibrating, 24-bit, delta-sigma A/D converters capable of achieving very high resolution digital results. Each contains a programmable gain amplifier (PGA); a second-order delta-sigma modulator; a programmable digital filter; a microcontroller including the Instruction, Command and Calibration registers; a serial interface; a clock generator circuit; and an internal 2.5V reference. The ADS1213 includes a 4-channel input multiplexer.

In order to provide low system noise, common-mode rejection of 100dB and excellent power supply rejection, the design topology is based on a fully differential switched capacitor architecture. Turbo Mode, a unique feature of the ADS1212/13, can be used to boost the sampling rate of the input capacitor, which is normally 7.8kHz with a 1MHz clock. By programming the Command Register, the sampling rate can be increased to 15.6kHz, 31.2kHz, 62.5kHz, or 125kHz. Each increase in sample rate results in an increase in performance when maintaining the same output data rate.

The programmable gain amplifier (PGA) of the ADS1212/13 can be set to a gain of 1, 2, 4, 8 or 16—substantially increasing the dynamic range of the converter and simplifying the interface to the more common transducers (see Table I). This gain is implemented by increasing the number of samples taken by the input capacitor from 7.8kHz for a gain of 1 to 125kHz for a gain of 16. Since the Turbo Mode and PGA functions are both implemented by varying the sampling frequency of the input capacitor, the combination of PGA gain and Turbo Mode Rate is limited to 16 (see Table II). For example, when using a Turbo Mode Rate of 8 (62.5kHz at 1MHz), the maximum PGA gain setting is 2.

GAIN SETTING	ANALOG INPUT[1]		ANALOG INPUT UTILIZING V_{BIAS}[1,2]	
	FULL-SCALE RANGE (V)	EXAMPLE VOLTAGE RANGE[3] (V)	FULL-SCALE RANGE (V)	EXAMPLE VOLTAGE RANGE[3] (V)
1	10	0 to 5	40	±10
2	5	1.25 to 3.75	20	±5
4	2.5	1.88 to 3.13	10	±2.5
8	1.25	2.19 to 2.81	5	±1.25
16	0.625	2.34 to 2.66	2.5	±0.625

NOTE: (1) With a 2.5V reference, such as the internal reference. (2) This example utilizes the circuit in Figure 12. Other input ranges are possible. (3) The ADS1212/13 allows common-mode voltage as long as the absolute input voltage on $A_{IN}P$ or $A_{IN}N$ does not go below AGND or above AV_{DD}.

TABLE I. Full-Scale Range vs PGA Setting.

TURBO MODE RATE	AVAILABLE PGA SETTINGS
1	1, 2, 4, 8, 16
2	1, 2, 4, 8
4	1, 2, 4
8	1, 2
16	1

TABLE II. Available PGA Settings vs Turbo Mode Rate.

The output data rate of the ADS1212/13 can be varied from less than 1Hz to as much as 6.25kHz, trading off lower resolution results for higher data rates. In addition, the data rate determines the first null of the digital filter and sets the –3dB point of the input bandwidth (see the Digital Filter section). Changing the data rate of the ADS1212/13 does not result in a change in the sampling rate of the input capacitor. The data rate effectively sets the number of samples which are used by the digital filter to obtain each conversion result. A lower data rate results in higher resolution, lower input bandwidth, and different notch frequencies than a higher data rate. It does not result in any change in input impedance or modulator frequency, or any appreciable change in power consumption.

The ADS1212/13 also includes complete on-board calibration that can correct for internal offset and gain errors or limited external system errors. Internal calibration can be run when needed, or automatically and continuously in the background. System calibration can be run as needed and the appropriate input voltages must be provided to the ADS1212/13. For this reason, there is no continuous system calibration mode. The calibration registers are fully readable and writable. This feature allows for switching between various configurations—different data rates, Turbo Mode Rates, and gain settings—without re-calibrating.

The various settings, rates, modes, and registers of the ADS1212/13 are read or written via a synchronous serial interface. This interface can operate in either a self-clocked mode (Master Mode) or an externally clocked mode (Slave Mode). In the Master Mode, the serial clock (SCLK) frequency is one-quarter of the ADS1212/13 X_{IN} clock frequency.

The high resolution and flexibility of the ADS1212/13 allow these converters to fill a wide variety of A/D conversion tasks. In order to ensure that a particular configuration will meet the design goals, there are several important items which must be considered. These include (but are certainly not limited to) the needed resolution, required linearity, desired input bandwidth, power consumption goal, and sensor output voltage.

The remainder of this data sheet discusses the operation of the ADS1212/13 in detail. In order to allow for easier comparison of different configurations, “effective resolution” is used as the figure of merit for most tables and graphs. For example, Table III shows a comparison between data rate (and –3dB input bandwidth) versus PGA setting at a Turbo Mode Rate of 1 and a clock rate of 1MHz. See the Definition of Terms section for a definition of effective resolution.

DATA RATE (HZ)	-3DB FREQUENCY (HZ)	EFFECTIVE RESOLUTION (BITS RMS)				
		G = 1	G = 2	G = 4	G = 8	G = 16
10	2.62	20	20	20	19	18
25	6.55	19	19	19	18	18
30	7.86	19	19	18	18	17
50	13.1	17	17	17	17	16
60	15.7	17	17	17	16	16
100	26.2	15	15	15	15	15
250	65.5	12	12	12	12	12

TABLE III. Effective Resolution vs Data Rate and Gain Setting. (Turbo Mode Rate of 1 and a 1MHz clock.)

DEFINITION OF TERMS

An attempt has been made to be consistent with the terminology used in this data sheet. In that regard, the definition of each term is given as follows:

Analog Input Differential Voltage—For an analog signal that is fully differential, the voltage range can be compared to that of an instrumentation amplifier. For example, if both analog inputs of the ADS1212 are at 2.5V, then the differential voltage is 0V. If one is at 0V and the other at 5V, then the differential voltage magnitude is 5V. But, this is the case regardless of which input is at 0V and which is at 5V, while the digital output result is quite different.

The analog input differential voltage is given by the following equation: $A_{IN}P - A_{IN}N$. Thus, a positive digital output is produced whenever the analog input differential voltage is positive, while a negative digital output is produced whenever the differential is negative.

For example, when the converter is configured with a 2.5V reference and placed in a gain setting of 2, the positive full-scale output is produced when the analog input differential is 2.5V. The negative full-scale output is produced when the differential is –2.5V. In each case, the actual input voltages must remain within the AGND to AV_{DD} range (see Table I).

Actual Analog Input Voltage—The voltage at any one analog input relative to AGND.

Full-Scale Range (FSR)—As with most A/D converters, the full-scale range of the ADS1212/13 is defined as the "input" which produces the positive full-scale digital output minus the "input" which produces the negative full-scale digital output.

For example, when the converter is configured with a 2.5V reference and is placed in a gain setting of 2, the full-scale range is: [2.5V (positive full scale) minus –2.5V (negative full scale)] = 5V.

Typical Analog Input Voltage Range—This term describes the actual voltage range of the analog inputs which will cover the converter's full-scale range, assuming that each input has a common-mode voltage that is greater than REF_{IN}/PGA and smaller than ($AV_{DD} - REF_{IN}/PGA$).

For example, when the converter is configured with a 2.5V reference and placed in a gain setting of 2, the typical input voltage range is 1.25V to 3.75V (common-mode voltage = 2.5V). However, an input range of 0V to 2.5V (common-mode voltage = 1.25V) or 2.5V to 5V (common-mode voltage = 3.75V) would also cover the converter's full-scale range.

Voltage Span—This is simply the magnitude of the typical analog input voltage range. For example, when the converter is configured with a 2.5V reference and placed in a gain setting of 2, the input voltage span is 2.5V.

Least Significant Bit (LSB) Weight—This is the theoretical amount of voltage that the differential voltage at the analog input would have to change in order to observe a change in the output data of one least significant bit. It is computed as follows:

$$\text{LSB Weight} = \frac{\text{Full–Scale Range}}{2^N}$$

where N is the number of bits in the digital output.

Effective Resolution—The effective resolution of the ADS1212/13 in a particular configuration can be expressed in two different units: bits rms (referenced to output) and microvolts rms (referenced to input). Computed directly from the converter's output data, each is a statistical calculation based on a given number of results. Knowing one, the other can be computed as follows:

$$\text{ER in bits rms} = \frac{20 \bullet \log\left(\frac{\left(\frac{10\text{V}}{\text{PGA}}\right)}{\text{ER in Vrms}}\right) - 1.76}{6.02}$$

$$\text{ER in Vrms} = \frac{\left(\frac{10\text{V}}{\text{PGA}}\right)}{10^{\left(\frac{6.02 \bullet \text{ER in bits rms} + 1.76}{20}\right)}}$$

The 10V figure in each calculation represents the full-scale range of the ADS1212/13 in a gain setting of 1. This means that both units are absolute expressions of resolution—the performance in different configurations can be directly compared regardless of the units. Comparing the resolution of different gain settings expressed in bits rms requires accounting for the PGA setting.

Main Controller—A generic term for the external microcontroller, microprocessor, or digital signal processor which is controlling the operation of the ADS1212/13 and receiving the output data.

f_{XIN}—The frequency of the crystal oscillator or CMOS compatible input signal at the X_{IN} input of the ADS1212/13.

f_{MOD}—The frequency or speed at which the modulator of the ADS1212/13 is running, given by the following equation:

$$f_{MOD} = \frac{f_{XIN} \bullet \text{Turbo Mode}}{128}$$

f_{SAMP}—The frequency or switching speed of the input sampling capacitor. The value is given by the following equation:

$$f_{SAMP} = \frac{f_{XIN} \bullet \text{Turbo Mode} \bullet \text{Gain Setting}}{128}$$

f_{DATA}, t_{DATA}—The frequency of the digital output data produced by the ADS1212/13 or the inverse of this (the period), respectively, f_{DATA} is also referred to as the data rate.

$$f_{DATA} = \frac{f_{XIN} \bullet \text{Turbo Mode}}{128 \bullet (\text{Decimation Ratio} + 1)}, \quad t_{DATA} = \frac{1}{f_{DATA}}$$

Conversion Cycle—The term "conversion cycle" usually refers to a discrete A/D conversion operation, such as that performed by a successive approximation converter. As used here, a conversion cycle refers to the t_{DATA} time period. However, each digital output is actually based on the modulator results from the last three t_{DATA} time periods.

DIGITAL FILTER

The digital filter of the ADS1212/13 computes the output result based on the most recent results from the delta-sigma modulator. The number of modulator results that are used depend on the decimation ratio set in the Command Register. At the most basic level, the digital filter can be thought of as simply averaging the modulator results and presenting this average as the digital output.

While the decimation ratio determines the number of modulator results to use, the modulator runs faster at higher Turbo Modes. These two items, together with the ADS1212/13 clock frequency, determine the output data rate:

$$f_{DATA} = \frac{f_{XIN} \bullet \text{Turbo Mode}}{128 \bullet (\text{Decimation Ratio} + 1)}$$

Also, since the conversion result is essentially an average, the data rate determines where the resulting notches are in the digital filter. For example, if the output data rate is 1kHz, then a 1kHz input frequency will average to zero during the 1ms conversion cycle. Likewise, a 2kHz input frequency will average to zero, etc.

In this manner, the data rate can be used to set specific notch frequencies in the digital filter response (see Figure 1 for the normalized response of the digital filter). For example, if the rejection of power line frequencies is desired, then the data rate can simply be set to the power line frequency. Figures 2 and 3 show the digital filter response for a data rate of 50Hz and 60Hz, respectively.

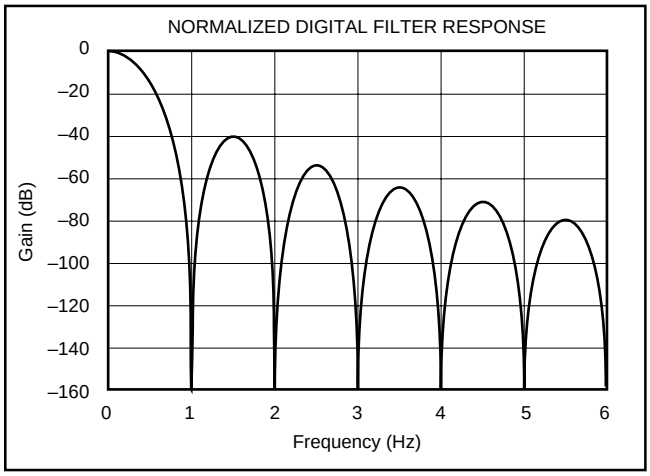


FIGURE 1. Normalized Digital Filter Response.

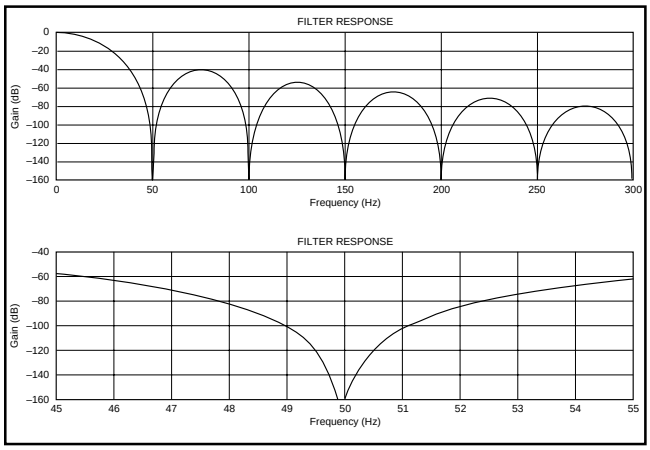


FIGURE 2. Digital Filter Response at a Data Rate of 50Hz.

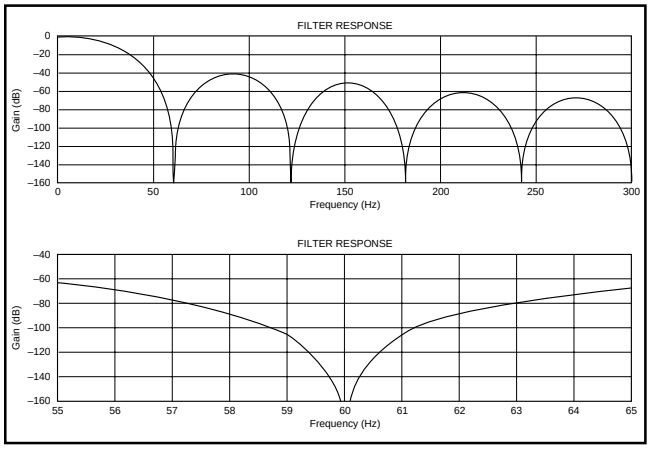


FIGURE 3. Digital Filter Response at a Data Rate of 60Hz.

If the effective resolution at a 50Hz or 60Hz data rate is not adequate for the particular application, then power line frequencies could still be rejected by operating the ADS1212/13 at 25/30Hz, 16.7/20Hz, 12.5/15Hz, etc. If a higher data rate is needed, then power line frequencies must either be rejected before conversion (with an analog notch filter) or after conversion (with a digital notch filter running on the main controller).

Filter Equation

The digital filter is described by the following transfer function:

$$|H(f)| = \left| \frac{\sin\left(\frac{\pi \bullet f \bullet N}{f_{MOD}}\right)}{N \bullet \sin\left(\frac{\pi \bullet f}{f_{MOD}}\right)} \right|^3$$

where N is the Decimation Ratio.

This filter has a $(\sin(x)/x)^3$ response and is referred to a $sinc^3$ filter. For the ADS1212/13, this type of filter allows the data rate to be changed over a very wide range (nearly four orders of magnitude). However, the –3dB point of the filter is 0.262 times the data rate. And, as can be seen in Figures 1 and 2, the rejection in the stopband (frequencies higher than the first notch frequency) may only be –40dB.

These factors must be considered in the overall system design. For example, with a 50Hz data rate, a significant signal at 75Hz may alias back into the passband at 25Hz. The analog front end can be designed to provide the needed attenuation to prevent aliasing, or the system may simply provide this inherently. Another possibility is increasing the data rate and then post filtering with a digital filter on the main controller.

Filter Settling

The number of modulator results used to compute each conversion result is three times the Decimation Ratio. This means that any step change (or any channel change for the ADS1213) will require at least three conversions to fully settle. However, if the change occurs asynchronously, then at least four conversions are required to ensure complete settling. For example, on the ADS1213, the fourth conversion result after a channel change will be valid (see Figure 4).

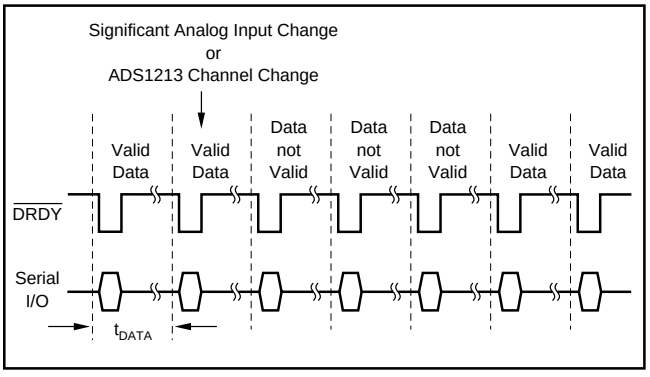


FIGURE 4. Asynchronous ADS1212/13 Analog Input Voltage Step or ADS1213 Channel Change to Fully Settled Output Data.

TURBO MODE

The ADS1212/13 offers a unique Turbo Mode feature which can be used to increase the modulator sampling rate by 2, 4, 8, or 16 times normal. With the increase of modulator sampling frequency, there can be a substantial increase in the effective resolution of the output data at a given data rate, but there is also an increase in power dissipation. For Turbo Mode Rates 2 and 4, the increase is slight. For rates 8 and 16, the increase is more substantial. See the Typical Performance Curves for more information.

In a Turbo Mode Rate of 16, the ADS1212/13 can offer 16 bits of effective resolution at a 1kHz data rate. A comparison of effective resolution versus Turbo Mode Rates and output data rates is shown in Table IV while Table V shows the corresponding noise level in μVrms.

DATA RATE (HZ)	EFFECTIVE RESOLUTION (BITS RMS)				
	TURBO MODE RATE 1	TURBO MODE RATE 2	TURBO MODE RATE 4	TURBO MODE RATE 8	TURBO MODE RATE 16
10	20	21	21		
20	19	20	21	21	
40	18	20	21	21	21
50	17	19	20	21	21
60	17	19	20	21	21
100	15	17	19	21	21
250	12	14	16	19	20
1000			12	14	16

TABLE IV. Effective Resolution vs Data Rate and Turbo Mode Rate. (Gain setting of 1 and 1MHz clock.)

DATA RATE (Hz)	NOISE LEVEL (μVrms)				
	TURBO MODE RATE 1	TURBO MODE RATE 2	TURBO MODE RATE 4	TURBO MODE RATE 8	TURBO MODE RATE 16
10	7.6	3.8	3.8		
20	15	7.6	3.8	3.8	
40	30	7.6	3.8	3.8	3.8
50	60	15	7.6	3.8	3.8
60	60	15	7.6	3.8	3.8
100	240	60	15	3.8	3.8
250	1900	480	120	15	7.6
1000			1900	480	120

TABLE V. Noise Level vs Data Rate and Turbo Mode Rate. (Gain setting of 1 and 1MHz clock.)

The Turbo Mode feature allows trade-offs to be made between the ADS1212/13 X_{IN} clock frequency, power dissipation, and effective resolution. If a 0.5MHz clock is available but a 1MHz clock is needed to achieve the desired performance, a Turbo Mode Rate of 2X will result in the same effective resolution. Table VI provides a comparison of effective resolution at various clock frequencies, data rates, and Turbo Mode Rates.

DATA RATE (Hz)	X_{IN} CLOCK FREQUENCY (MHz)	TURBO MODE RATE	EFFECTIVE RESOLUTION (Bits rms)
60	2	2	20
60	1	4	20
60	0.5	8	20
100	2	2	19
100	1	4	19
100	0.5	8	19

TABLE VI. Effective Resolution vs Data Rate, Clock Frequency, and Turbo Mode Rate. (Gain setting of 1.)

The Turbo Mode Rate (TMR) is programmed via the Sampling Frequency bits of the Command Register. Due to the increase in input capacitor sampling frequency, higher Turbo Mode settings result in lower analog input impedance;

$$A_{IN} \text{ Impedance } (\Omega) = (1MHz/f_{XIN}) \bullet 20E6/(G \bullet TMR)$$

where G is the gain setting. Because the modulator rate also changes in direct relation to the Turbo Mode setting, higher values result in a lower impedance for the REF_{IN} input:

$$REF_{IN} \text{ Impedance } (\Omega) = (1MHz/f_{XIN}) \bullet 5E6/TMR$$

The Turbo Mode Rate can be set to 1, 2, 4, 8, or 16. Consult the graphs shown in the Typical Performance Curves for full details on the performance of the ADS1212/13 operating in different Turbo Mode Rates. Keep in mind that higher Turbo Mode Rates result in fewer available gain settings as shown in Table II.

PROGRAMMABLE GAIN AMPLIFIER

The programmable gain amplifier gain setting is programmed via the PGA Gain bits of the Command Register. Changes in the gain setting (G) of the programmable gain amplifier results in an increase in the input capacitor sampling frequency. Thus, higher gain settings result in a lower analog input impedance:

$$A_{IN} \text{ Impedance } (\Omega) = (1MHz/f_{XIN}) \bullet 20E6/(G \bullet TMR)$$

where TMR is the Turbo Mode Rate. Because the modulator speed does not depend on the gain setting, the input impedance seen at REF_{IN} does not change.

The PGA can be set to gains of 1, 2, 4, 8, or 16. These gain settings with their resulting full-scale range and typical voltage range are shown in Table I. Keep in mind that higher Turbo Mode Rates result in fewer available gain settings as shown in Table II.

SOFTWARE GAIN

The excellent performance, flexibility, and low cost of the ADS1212/13 allow the converter to be considered for designs which would not normally need a 24-bit ADC. For example, many designs utilize a 12-bit converter and a high-gain INA or PGA for digitizing low amplitude signals. For some of these cases, the ADS1212/13 by itself may be a solution, even though the maximum gain is limited to 16.

To get around the gain limitation, the digital result can simply be shifted up by “n” bits in the main controller—resulting in a gain of “n” times G, where G is the gain setting. While this type of manipulation of the output data is obvious, it is easy to miss how much the gain can be increased in this manner on a 24-bit converter.

For example, shifting the result up by three bits when the ADS1212/13 is set to a gain of 16 results in an effective gain of 128. At lower data rates, the converter can easily provide more than 12 bits of resolution. Even higher gains are possible. The limitation is a combination of the needed data rate, desired noise performance, and desired linearity.

CALIBRATION

The ADS1212/13 offers several different types of calibration, and the particular calibration desired is programmed via the Command Register. In the case of Background Calibration, the calibration will repeat at regular intervals indefinitely. For all others, the calibration is performed once and then normal operation is resumed.

Each type of calibration is covered in detail in its respective section. In general, calibration is recommended immediately after power-on and whenever there is a “significant” change in the operating environment. The amount of change which should cause a re-calibration is dependent on the application, effective resolution, etc. Where high accuracy is important, re-calibration should be done on changes in temperature and power supply. In all cases, re-calibration should be done when the gain, Turbo Mode, or data rate is changed.

After a calibration has been accomplished, the Offset Calibration Register and the Full-Scale Calibration Register contain the results of the calibration. The data in these registers are accurate to the effective resolution of the ADS1212/13’s mode of operation during the calibration. Thus, these values will show a variation (or noise) equivalent to a regular conversion result.

For those cases where this error must be reduced, it is tempting to consider running the calibration at a slower data rate and then increasing the converter’s data rate after the calibration is complete. Unfortunately, this will not work as expected. The reason is that the results calculated at the slower data rate would not be valid for the higher data rate. Instead, the calibration should be done repeatedly. After each calibration, the results can be read and stored. After the desired number of calibrations, the main controller can compute an average and write this value into the calibration registers. The resulting error in the calibration values will be reduced by the square root of the number of calibrations which were averaged.

The calibration registers can also be used to provide system offset and gain corrections separate from those computed by the ADS1212/13. For example, these might be burned into E^2PROM during final product testing. On power-on, the main controller would load these values into the calibration registers. A further possibility is a look-up table based on the current temperature.

Note that the values in the calibration registers will vary from configuration to configuration and from part to part. There is no method of reliably computing what a particular calibration register should be to correct for a given amount of system error. It is possible to present the ADS1212/13 with a known amount of error, perform a calibration, read the desired calibration register, change the error value, perform another calibration, read the new value and use these values to interpolate an intermediate value.

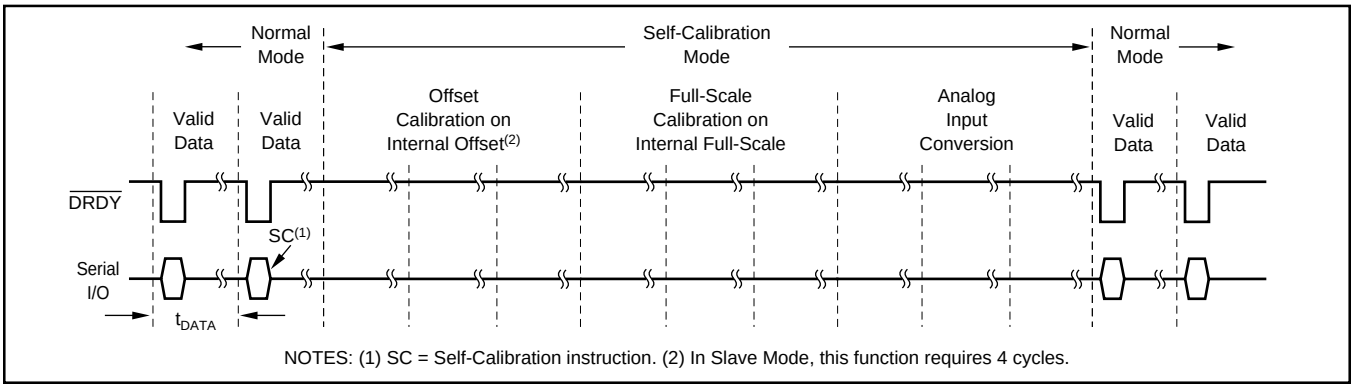


FIGURE 5. Self-Calibration Timing.

Self-Calibration

A self-calibration is performed after the bits 001 have been written to the Command Register Operation Mode bits (MD2 through MD0). This initiates the following sequence at the start of the next conversion cycle (see Figure 5). The $\overline{DRDY}$ signal will not go LOW but will remain HIGH and will continue to remain HIGH throughout the calibration sequence. The inputs to the sampling capacitor are disconnected from the converter's analog inputs and are shorted together. An offset calibration is performed over the next three conversion periods (four in Slave Mode). Then, the input to the sampling capacitor is connected across REF_{IN}, and a full-scale calibration is performed over the next three conversions.

After this, the Operation Mode bits are reset to 000 (Normal Mode) and the input capacitor is reconnected to the input. Conversions proceed as usual over the next three cycles in order to fill the digital filter. $\overline{DRDY}$ remains HIGH during this time. On the start of the fourth cycle , $\overline{DRDY}$ goes LOW indicating valid data and resumption of normal operation.

System Offset Calibration

A system offset calibration is performed after the bits 010 have been written to the Command Register Operation Mode bits (MD2 through MD0). This initiates the following sequence (see Figure 6). At the start of the next conversion cycle, the $\overline{DRDY}$ signal will not go LOW but will remain HIGH and will continue to remain HIGH throughout the calibration sequence. The offset calibration will be performed on the differential input voltage present at the converter's input over the next three conversion periods (four in Slave Mode). When this is done, the Operation Mode bits are reset to 000 (Normal Mode). A single conversion is done with $\overline{DRDY}$ HIGH. After this conversion, the $\overline{DRDY}$ signal goes LOW indicating resumption of normal operation.

Normal operation returns within a single conversion cycle because it is assumed that the input voltage at the converter's input is not removed immediately after the offset calibration is performed. In this case, the digital filter already contains a valid result.

For full system calibration, offset calibration must be performed first and then full-scale calibration. In addition, the offset calibration error will be the rms sum of the conversion error and the noise on the system offset voltage. See the System Calibration Limits section for information regarding the limits on the magnitude of the system offset voltage.

System Full-Scale Calibration

A system full-scale calibration is performed after the bits 011 have been written to the Command Register Operation Mode bits (MD2 through MD0). This initiates the following sequence (see Figure 7). At the start of the next conversion cycle, the $\overline{DRDY}$ signal will not go LOW but will remain HIGH and will continue to remain HIGH throughout the calibration sequence. The full-scale calibration will be performed on the differential input voltage ($2 \cdot REF_{IN}/G$) present at the converter's input over the next three conversion periods (four in Slave Mode). When this is done, the Operation Mode bits are reset to 000 (Normal Mode). A single conversion is done with $\overline{DRDY}$ HIGH. After this conversion, the $\overline{DRDY}$ signal goes LOW indicating resumption of normal operation.

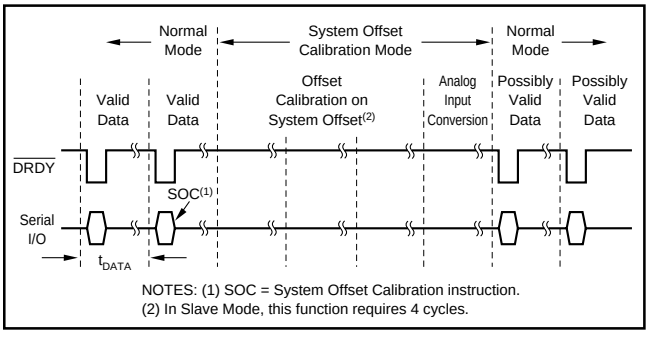


FIGURE 6. System Offset Calibration Timing.

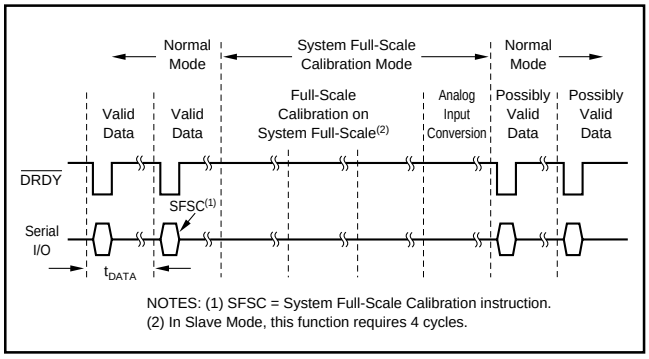


FIGURE 7. System Full-Scale Calibration Timing.

Normal operation returns within a single conversion cycle because it is assumed that the input voltage at the converter's input is not removed immediately after the full-scale calibration is performed. In this case, the digital filter already contains a valid result.

For full system calibration, offset calibration must be performed first and then full-scale calibration. The calibration error will be a sum of the rms noise on the conversion result and the input signal noise. See the System Calibration Limits section for information regarding the limits on the magnitude of the system full-scale voltage.

Pseudo System Calibration

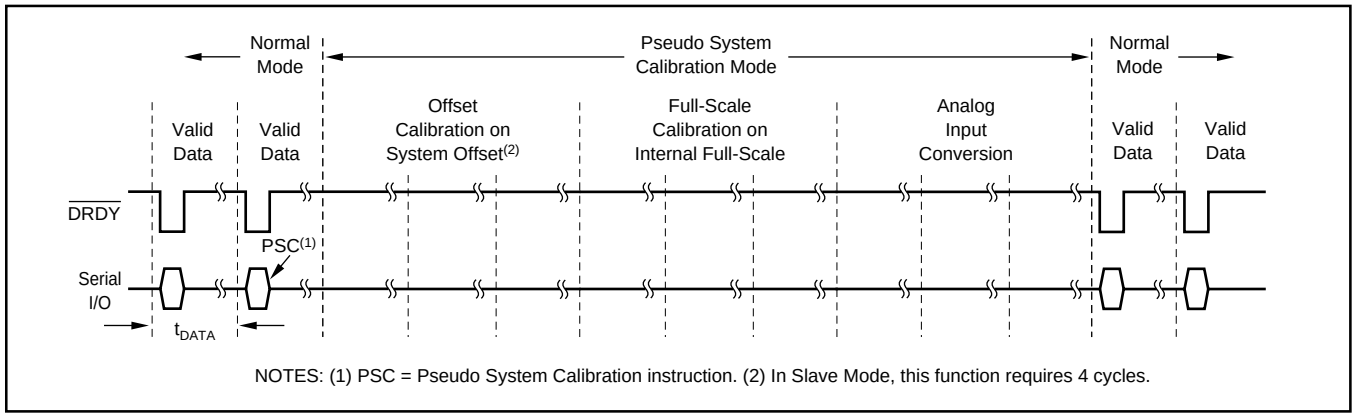
The Pseudo System Calibration is performed after the bits 100 have been written to the Command Register Operation Mode bits (MD2 through MD0). This initiates the following sequence (see Figure 8). At the start of the next conversion cycle, the $\overline{\text{DRDY}}$ signal will not go LOW but will remain HIGH and will continue to remain HIGH throughout the calibration sequence. The offset calibration will be performed on the differential input voltage present at the converter's input over the next three conversion periods (four in Slave Mode). Then, the input to the sampling capacitor is disconnected from the converter's analog input and connected across REF_{IN}. A gain calibration is performed over the next three conversions.

After this, the Operation Mode bits are reset to 000 (Normal Mode) and the input capacitor is then reconnected to the input. Conversions proceed as usual over the next three cycles in order to fill the digital filter. $\overline{\text{DRDY}}$ remains HIGH during this time. On the next cycle, the $\overline{\text{DRDY}}$ signal goes LOW indicating valid data and resumption of normal operation.

The system offset calibration range of the ADS1212/13 is limited and is listed in the Specifications Table. For more information on how to use these specifications, see the System Calibration Limits section. To calculate V_{OS}, use $2 \cdot REF_{IN}/GAIN$ for V_{FS}.

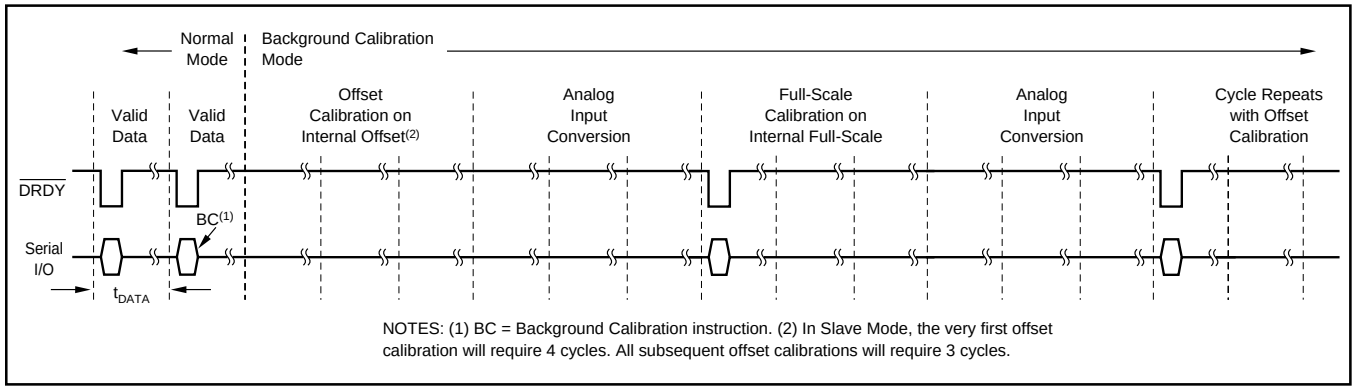
Background Calibration

The Background Calibration Mode is entered after the bits 101 have been written to the Command Register Operation Mode bits (MD2 through MD0). This initiates the following continuous sequence (see Figure 9). At the start of the next conversion cycle, the $\overline{\text{DRDY}}$ signal will not go LOW but will remain HIGH. The inputs to the sampling capacitor are disconnected from the converter's analog input and shorted together. An offset calibration is performed over the next three conversion periods (in Slave Mode, the very first offset calibration requires four periods, and all subsequent offset calibrations require three periods). Then, the input capacitor is reconnected to the input. Conversions proceed as usual over the next three cycles in order to fill the digital filter. $\overline{\text{DRDY}}$ remains HIGH during this time. On the next cycle, the $\overline{\text{DRDY}}$ signal goes LOW indicating valid data.



NOTES: (1) PSC = Pseudo System Calibration instruction. (2) In Slave Mode, this function requires 4 cycles.

FIGURE 8. Pseudo System Calibration Timing.



NOTES: (1) BC = Background Calibration instruction. (2) In Slave Mode, the very first offset calibration will require 4 cycles. All subsequent offset calibrations will require 3 cycles.

FIGURE 9. Background Calibration Timing.

Also, during this cycle, the sampling capacitor is disconnected from the converter's analog input and is connected across REF_{IN}. A gain calibration is initiated and proceeds over the next three conversions. After this, the input capacitor is once again connected to the analog input. Conversions proceed as usual over the next three cycles in order to fill the digital filter. $\overline{DRDY}$ remains HIGH during this time. On the next cycle, the $\overline{DRDY}$ signal goes LOW indicating valid data, the input to the sampling capacitor is shorted, and an offset calibration is initiated. At this point, the Background Calibration sequence repeats.

In essence, the Background Calibration Mode performs continuous self-calibration where the offset and gain calibrations are interleaved with regular conversions. Thus, the data rate is reduced by a factor of 6. The advantage is that the converter is continuously adjusting to environmental changes such as ambient or component temperature (due to airflow variations).

The ADS1212/13 will remain in the Background Calibration Mode indefinitely. To move to any other mode, the Command Register Operation Mode bits (MD2 through MD0) must be set to the appropriate values.

System Calibration Offset and Full-Scale Calibration Limits

The System Offset and Full-Scale Calibration range of the ADS1212/13 is limited and is listed in the Specifications Table. The range is specified as:

$$(V_{FS} - |V_{OS}|) < 1.3 \bullet (2 \bullet REF_{IN})/GAIN$$
$$(V_{FS} - |V_{OS}|) > 0.7 \bullet (2 \bullet REF_{IN})/GAIN$$

where V_{FS} is the system full-scale voltage and $|V_{OS}|$ is the absolute value of the system offset voltage. In the following discussion, keep in mind that these voltages are differential voltages.

For example, with the internal reference (2.5V) and a gain of two, the previous equations become (after some manipulation):

$$V_{FS} - 3.25 < V_{OS} < V_{FS} - 1.75$$

If V_{FS} is perfect at 2.5V (positive full-scale), then V_{OS} must be greater than –0.75V and less than 0.75V. Thus, when offset calibration is performed, the positive input can be no more than 0.75V below or above the negative input. If this range is exceeded, the ADS1212/13 may not calibrate properly.

This calculation method works for all gains other than one. For a gain of one and the internal reference (2.5V), the equation becomes:

$$V_{FS} - 6.5 < V_{OS} < V_{FS} - 3.5$$

With a 5V positive full-scale input, V_{OS} must be greater than –1.5V and less than 1.5V. Since the offset represents a common-mode voltage and the input voltage range in a gain of one is 0V to 5V, a common-mode voltage will cause the actual input voltage to possibly go below 0V or above 5V. The specifications also show that for the specifications to be valid, the input voltage must not go below AGND by more than 30mV or above AV_{DD} by more than 30mV.

This will be an important consideration in many systems which use a 2.5V or greater reference, as the input range is constrained by the expected power supply variations. In addition, the expected full-scale voltage will impact the allowable offset voltage (and vice-versa) as the combination of the two must remain within the power supply and ground potentials, regardless of the results obtained via the range calculation shown previously.

There are only two solutions to this constraint: either the system design must ensure that the full-scale and offset voltage variations will remain within the power supply and ground potentials, or the part must be used in a gain of 2 or greater.

SLEEP MODE

The Sleep Mode is entered after the bits 110 have been written to the Command Register Operation Mode bits (MD2 through MD0). This mode is exited by entering a new mode into the MD2-MD0 bits.

The Sleep Mode causes the analog section and a good deal of the digital section to power down. For full analog power down, the V_{BIAS} generator and the internal reference must also be powered down by setting the BIAS and REFO bits in the Command Register accordingly. The power dissipation shown in the Specifications Table is with the internal reference and the V_{BIAS} generator disabled.

To establish serial communication with the converter while it is in Sleep Mode, one of the following procedures must be used: If $\overline{CS}$ is being used, simply taking $\overline{CS}$ LOW will enable serial communication to proceed normally. If $\overline{CS}$ is not being used (tied LOW) and the ADS1212/13 is in the Master Mode, then a falling edge must be produced on the SDIO line. If SDIO is LOW, the SDIO line must be taken HIGH for $4 \bullet t_{XIN}$ periods (minimum) and then taken LOW. Alternatively, SDIO can be forced HIGH after putting the ADS1212/13 to "sleep" and then taken LOW when the Sleep Mode is to be exited. Finally, if $\overline{CS}$ is not being used (tied LOW) and the ADS1212/13 is in the Slave Mode, then simply sending a normal Instruction Register command will re-establish communication.

Once serial communication is resumed, the Sleep Mode is exited by changing the MD2-MD0 bits to any other mode. When a new mode (other than Sleep) has been entered, the ADS1212/13 will execute a very brief internal power-up sequence of the analog and digital circuitry. Once this has been done, one normal conversion cycle is performed before the new mode is actually entered. At the end of this conversion cycle, the new mode takes effect and the converter will respond accordingly. The $\overline{DRDY}$ signal will remain HIGH through the first conversion cycle. It will also remain HIGH through the second, even if the new mode is the Normal Mode.

If the V_{BIAS} generator and/or the internal reference have been disabled, then they must be manually re-enabled via the appropriate bits in the Command Register. In addition, the internal reference will have to charge the external bypass capacitor(s) and possibly other circuitry. There may also be

considerations associated with V_{BIAS} and the settling of external circuitry. All of these must be taken into account when determining the amount of time required to resume normal operation. The timing diagram shown in Figure 10 does not take into account the settling of external circuitry.

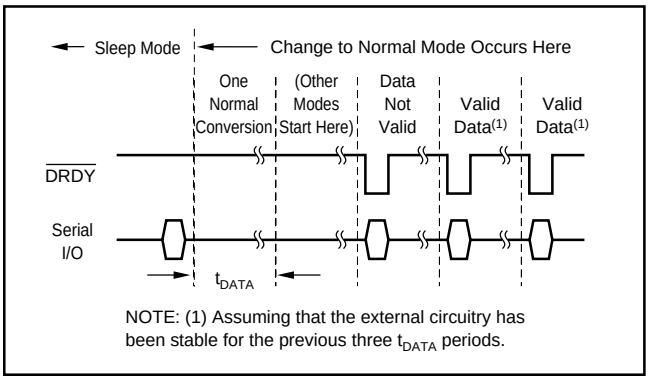


FIGURE 10. Sleep Mode to Normal Mode Timing.

ANALOG OPERATION

ANALOG INPUT

The input impedance of the analog input changes with ADS1212/13 clock frequency (f_{XIN}), gain (G), and Turbo Mode Rate (TMR). The relationship is:

$$A_{IN} \text{ Impedance } (\Omega) = (1MHz/f_{XIN}) \bullet 20E6/(G \bullet TMR)$$

Figure 11 shows the basic input structure of the ADS1212. The ADS1213 includes an input multiplexer, but this has little impact on the analysis of the input structure. The impedance is directly related to the sampling frequency of the input capacitor. The X_{IN} clock rate sets the basic sampling rate in a gain of 1 and Turbo Mode Rate of 1. Higher gains and higher Turbo Mode Rates result in an increase of the sampling rate, while slower clock (X_{IN}) frequencies result in a decrease.

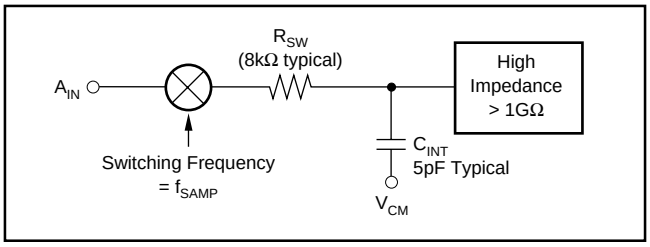


FIGURE 11. Analog Input Structure.

This input impedance can become a major point of consideration in some designs. If the source impedance of the input signal is significant or if there is passive filtering prior to the ADS1212/13, then a significant portion of the signal can be lost across this external impedance. How significant this effect is depends on the desired system performance.

There are two restrictions on the analog input signal to the ADS1212/13. Under no conditions should the current into or out of the analog inputs exceed 10mA. In addition, while the analog signal must reside within this range, the linearity of the ADS1212/13 is only ensured when the actual analog input voltage resides within a range defined by AGND – 30mV and AV_{DD} +30mV. This is due to leakage paths which occur within the part when AGND and AV_{DD} are exceeded.

For this reason, the 0V to 5V input range (gain of 1 with a 2.5V reference) must be used with caution. Should AV_{DD} be 4.75V, the analog input signal would swing outside of the tested specifications of the device. Designs utilizing this mode of operation should consider limiting the span to a slightly smaller range. Common-mode voltages are also a significant concern in this mode and must be carefully analyzed.

An input voltage range of 0.75V to 4.25V is the smallest span that is allowed if a full system calibration will be performed (see the Calibration section for more details). This also assumes an offset error of zero. A better choice would be 0.5V to 4.5V (a full-scale range of 9V). This span would allow some offset error, gain error, power supply drift, and common-mode voltage while still providing full system calibration over reasonable variation in each of these parameters.

The actual input voltage exceeding AGND or AV_{DD} should not be a concern in higher gain settings as the input voltage range will reside well within 0V to 5V. This is true unless the common-mode voltage is large enough to place positive full-scale or negative full-scale outside of the AGND to AV_{DD} range.

REFERENCE INPUT

The input impedance of the REF_{IN} input changes with clock frequency (f_{XIN}) and Turbo Mode Rate (TMR). The relationship is:

$$REF_{IN} \text{ Impedance } (\Omega) = (1MHz/f_{XIN}) \bullet 5E6/TMR$$

Unlike the analog input, the reference input impedance has a negligible dependency on the PGA gain setting.

The reference input voltage can vary between 2V and 3V. A nominal voltage of 2.5V appears at REF_{OUT}, and this can be directly connected to REF_{IN}. Higher reference voltages will cause the full-scale range to increase while the internal circuit noise of the converter remains approximately the same. This will increase the LSB weight but not the internal noise, resulting in increased signal-to-noise ratio and effective resolution. Likewise, lower reference voltages will decrease the signal-to-noise ratio and effective resolution.

REFERENCE OUTPUT

The ADS1212/13 contains an internal +2.5V reference. Tolerances, drift, noise, and other specifications for this reference are given in the Specification Table. Note that it is not designed to sink or to source more than 1mA of current. In addition, loading the reference with a dynamic or variable load is not recommended. This can result in small changes in reference voltage as the load changes. Finally, for designs approaching or exceeding 20 bits of effective resolution, a low-noise external reference is recommended as the internal reference may not have adequate performance.

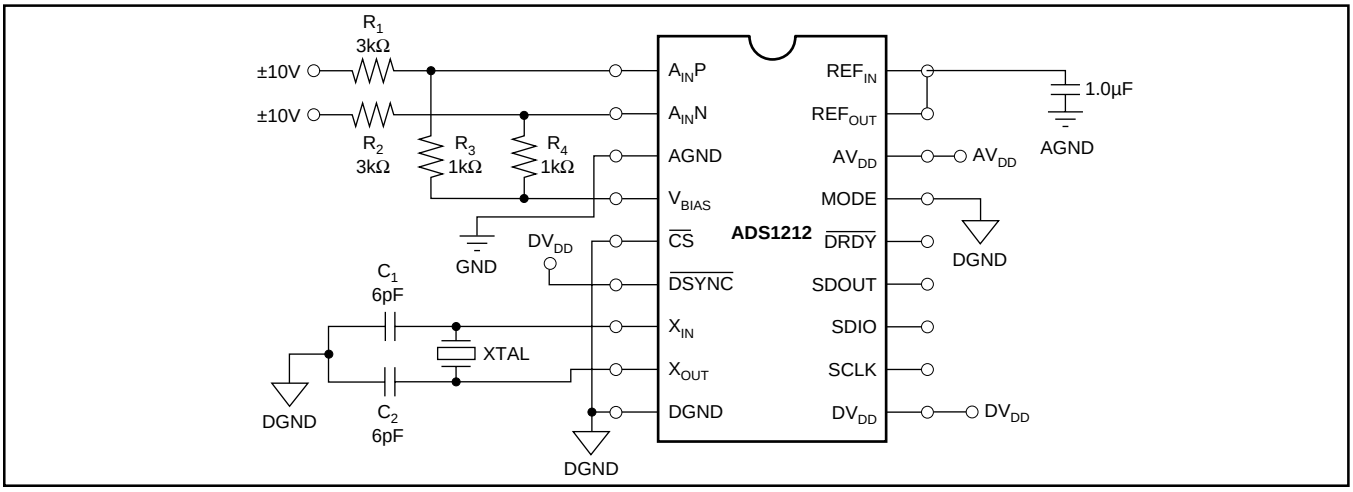


FIGURE 12. ±10V Input Configuration Using V_{BIAS}.

The circuitry which generates the +2.5V reference can be disabled via the Command Register and will result in a lower power dissipation. The reference circuitry consumes a little over 1.6mA of current with no external load. When the ADS1212/13 is in its default state, the internal reference is enabled.

V_{BIAS}

The V_{BIAS} output voltage is dependent on the reference input (REF_{IN}) voltage and is approximately 1.33 times as great. This output is used to bias input signals such that bipolar signals with spans of greater than 5V can be scaled to match the input range of the ADS1212/13. Figure 12 shows a connection diagram which will allow the ADS1212/13 to accept a ±10V input signal (40V full-scale range).

This method of scaling and offsetting the ±20V differential input signal will be a concern for those requiring minimum power dissipation. V_{BIAS} will supply 1.68mA for every channel connected as shown. For the ADS1213, the current draw is within the specifications for V_{BIAS}, but, at 12mW, the power dissipation is significant. If this is a concern, resistors R_1 and R_2 can be set to 9kΩ and R_3 and R_4 to 3kΩ. This will reduce power dissipation by one-third. In addition, these resistors can also be set to values which will provide any arbitrary input range. In all cases, the maximum current into or out of V_{BIAS} should not exceed its specification of 10mA.

Note that the connection diagram shown in Figure 12 causes a constant amount of current to be sourced by V_{BIAS}. This will be very important in higher resolution designs as the voltage at V_{BIAS} will not change with loading, as the load is constant. However, if the input signal is single-ended and one side of the input is grounded, the load will not be constant and V_{BIAS} will change slightly with the input signal. Also, in all cases, note that noise on V_{BIAS} introduces a common-mode error signal which is rejected by the converter.

The circuitry to generate V_{BIAS} is disabled when the ADS1212/13 is in its default state, and it must be enabled, via the Command Register, in order for the V_{BIAS} voltage to be present. When enabled, the V_{BIAS} circuitry consumes approximately 1mA with no external load.

On power-up, external signals may be present before V_{BIAS} is enabled. This can create a situation in which a negative voltage is applied to the analog inputs (–2.5V for the circuit shown in Figure 12), reverse biasing the negative input protection diode. This situation should not be a problem as long as the resistors R_1 and R_2 limit the current being sourced by each analog input to under 10mA (a potential of 0V at the analog input pin should be used in the calculation).

DIGITAL OPERATION

SYSTEM CONFIGURATION

The Micro Controller (MC) consists of an ALU and a register bank. The MC has two states: power-on reset and convert. In the power-on reset state, the MC resets all the registers to their default state, sets up the modulator to a stable state, and performs self-calibration at a 340Hz data rate. After this, it enters the Convert Mode, which is the normal mode of operation for the ADS1212/13.

The ADS1212/13 has 5 internal registers, as shown in Table VII. Two of these, the Instruction Register and the Command Register, control the operation of the converter. The Data Output Register (DOR) contains the result from the most recent conversion. The Offset and Full-Scale Calibration Registers (OCR and FCR) contain data used for correcting the internal conversion result before it is placed into the DOR. The data in these two registers may be the result of a calibration routine, or they may be values which have been written directly via the serial interface.

INSR	Instruction Register	8 Bits
DOR	Data Output Register	24 Bits
CMR	Command Register	32 Bits
OCR	Offset Calibration Register	24 Bits
FCR	Full-Scale Calibration Register	24 Bits

TABLE VII. ADS1212/13 Registers.

Communication with the ADS1212/13 is controlled via the Instruction Register (INSR). Under normal operation, the INSR is written as the first part of each serial communication. The instruction that is sent determines what type of communication will occur next. It is not possible to read the INSR.

The Command Register (CMR) controls all of the ADS1212/13's options and operating modes. These include the PGA gain setting, the Turbo Mode Rate, the output data rate (decimation ratio), etc. The CMR is the only 32-bit register within the ADS1212/13. It, and all the remaining registers, may be read from or written to.

Instruction Register (INSR)

The INSR is an 8-bit register which commands the serial interface either to read or to write "n" bytes beginning at the specified register location. Table VIII shows the format for the INSR.

MSB							LSB
R/$\overline{W}$	MB1	MB0	0	A3	A2	A1	A0

TABLE VIII. Instruction Register.

R/$\overline{W}$ (Read/$\overline{Write}$) Bit—For a write operation to occur, this bit of the INSR must be 0. For a read, this bit must be 1, as follows:

R/$\overline{W}$	
0	Write
1	Read

MB1, MB0 (Multiple Bytes) Bits—These two bits are used to control the word length (number of bytes) of the read or write operation, as follows:

MB1	MB0	
0	0	1 Byte
0	1	2 Bytes
1	0	3 Bytes
1	1	4 Bytes

A3-A0 (Address) Bits—These four bits select the beginning register location which will be read from or written to, as shown in Table IX. Each subsequent byte will be read from or written to the next higher location. (If the BD bit in the Command Register is set, each subsequent byte will be read from the next lower location. This bit does not affect the write operation.) If the next location is not defined in Table IX, then the results are unknown. Reading or writing continues until the number of bytes specified by MB1 and MB0 have been transferred.

A3	A2	A1	A0	REGISTER BYTE
0	0	0	0	Data Output Register Byte 2 (MSB)
0	0	0	1	Data Output Register Byte 1
0	0	1	0	Data Output Register Byte 0 (LSB)
0	1	0	0	Command Register Byte 3 (MSB)
0	1	0	1	Command Register Byte 2
0	1	1	0	Command Register Byte 1
0	1	1	1	Command Register Byte 0 (LSB)
1	0	0	0	Offset Cal Register Byte 2 (MSB)
1	0	0	1	Offset Cal Register Byte 1
1	0	1	0	Offset Cal Register Byte 0 (LSB)
1	1	0	0	Full-Scale Cal Register Byte 2 (MSB)
1	1	0	1	Full-Scale Cal Register Byte 1
1	1	1	0	Full-Scale Cal Register Byte 0 (LSB)
Note: MSB = Most Significant Byte, LSB = Least Significant Byte				

TABLE IX. A3-A0 Addressing.

Each serial communication starts with the 8-bits of the INSR being sent to the ADS1212/13. This directs the remainder of the communication cycle, which consists of n bytes being read from or written to the ADS1212/13. The read/write bit, the number of bytes n, and the starting register address are defined, as shown in Table VIII. When the n bytes have been transferred, the INSR is complete. A new communication cycle is initiated by sending a new INSR (under restrictions outlined in the Interfacing section).

Command Register (CMR)

The CMR controls all of the functionality of the ADS1212/13. The new configuration takes effect on the negative transition of SCLK for the last bit in each byte of data being written to the command register. The organization of the CMR is shown in Table X.

Most Significant Bit — **Byte 3**

BIAS	REFO	DF	U/$\overline{B}$	BD	MSB	SDL	DSYNC[1] / $\overline{DRDY}$	
0 Off	1 On	0 Two's	0 Biplr	0 MSByte	0 MSB	0 SDIO	0	Defaults

NOTE: (1) DSYNC is Write only, $\overline{DRDY}$ is Read only.

Byte 2

MD2 MD1 MD0	G2 G1 G0	CH1 CH0	
000 Normal Mode	000 Gain 1	00 Channel 1	Defaults

Byte 1

SF2 SF1 SF0	DR12 DR11 DR10 DR9 DR8	
000 Turbo Mode Rate of 1	00000	Defaults

Byte 0 Least Significant Bit

DR7 DR6 DR5 DR4 DR3 DR2 DR1 DR0	
(00000) 0001 0111 (23) Data Rate of 326Hz	Defaults

TABLE X. Organization of the Command Register and Default Status.

BIAS (Bias Voltage) Bit—The BIAS bit controls the V_{BIAS} output state—either on (1.33 • REF_{IN}) or off (disabled), as follows:

BIAS	V_{BIAS} GENERATOR	V_{BIAS} STATUS	
0	Off	Disabled	Default
1	On	1.33•REF_{IN}	

The V_{BIAS} circuitry consumes approximately 1mA of steady state current with no external load. See the V_{BIAS} section for full details. When the internal reference (REF_{OUT}) is connected to the reference input (REF_{IN}), V_{BIAS} is 3.3V, nominal.

REFO (Reference Output) Bit—The REFO bit controls the internal reference (REF_{OUT}) state, either on (2.5V) or off (disabled), as follows:

REFO	INTERNAL REFERENCE	REF_{OUT} STATUS	
0	Off	High Impedance	
1	On	2.5V	Default

The internal reference circuitry consumes approximately 1.6mA of steady state current with no external load. See the Reference Output section for full details on the internal reference.

DF (Data Format) Bit—The DF bit controls the format of the output data, either Two's Complement or Offset Binary, as follows:

DF	FORMAT	ANALOG INPUT	DIGITAL OUTPUT	
0	Two's Complement	+Full-Scale Zero –Full-Scale	$7FFFFF_H$ 000000_H 800000_H	Default
1	Offset Binary	+Full-Scale Zero –Full-scale	$FFFFFF_H$ 800000_H 000000_H	

These two formats are the same for all bits except the most significant, which is simply inverted in one format vs the other. This bit only applies to the Data Output Register—it has no effect on the other registers.

U/$\overline{B}$ (Unipolar) Bit—The U/$\overline{B}$ bit controls the limits imposed on the output data, as follows:

U/$\overline{B}$	MODE	LIMITS	
0	Bipolar	None	Default
1	Unipolar	Zero to +Full-Scale only	

The particular mode has no effect on the actual full-scale range of the ADS1212/13, data format, or data format vs input voltage. In the bipolar mode, the ADS1212/13 operates normally. In the unipolar mode, the conversion result is limited to positive values only (zero included).

This bit only controls what is placed in the Data Output Register. It has no effect on internal data. When cleared, the very next conversion will produce a valid bipolar result.

BD (Byte Order) Bit—The BD bit controls the order in which bytes of data are read, either most significant byte first or least significant byte, as follows:

BD	BYTE ACCESS ORDER	
0	Most Significant to Least Significant Byte	Default
1	Least Significant to Most Significant Byte	

Note that when BD is clear and a multi-byte read is initiated, A3-A0 of the Instruction Register is the address of the most significant byte and subsequent bytes reside at higher addresses. If BD is set, then A3-A0 is the address of the least significant byte and subsequent bytes reside at lower addresses. The BD bit only affects read operations; it has no effect on write operations.

MSB (Bit Order) Bit—The MSB bit controls the order in which bits within a byte of data are read, either most significant bit first or least significant bit, as follows:

MSB	BIT ORDER	
0	Most Significant Bit First	Default
1	Least Significant Bit First	

The MSB bit only effects read operations; it has no affect on write operations.

SDL (Serial Data Line) Bit—The SDL bit controls which pin on the ADS1212/13 will be used as the serial data output pin, either SDIO or SDOUT, as follows:

SDL	SERIAL DATA OUTPUT PIN	
0	SDIO	Default
1	SDOUT	

If SDL is LOW, then SDIO will be used for both input and output of serial data—see the Timing section for more details on how the SDIO pin transitions between these two states. In addition, SDOUT will remain in a tri-state condition at all times.

Important Note: Since the default condition is SDL LOW, SDIO has the potential of becoming an output once every data output cycle if the ADS1212/13 is in the Master Mode. This will occur until the Command Register can be written and the SDL bit set HIGH. See the Interfacing section for more information.

$\overline{DRDY}$ (Data Ready) Bit—The $\overline{DRDY}$ bit is a read-only bit which reflects the state of the ADS1212/13's $\overline{DRDY}$ output pin, as follows:

$\overline{DRDY}$	MEANING
0	Data Ready
1	Data Not Ready

DSYNC (Data Synchronization) Bit—The DSYNC bit is a write-only bit which occupies the same location as $\overline{DRDY}$. When a 'one' is written to this location, the effect on the ADS1212/13 is the same as if the $\overline{DSYNC}$ input pin had been taken LOW and returned HIGH. That is, the modulator count for the current conversion cycle will be reset to zero.

DSYNC	MEANING
0	No Change in Modulator Count
1	Modulator Count Reset to Zero

The DSYNC bit is provided in order to reduce the number of interface signals that are needed between the ADS1212/13 and the main controller. Consult "Making Use of $\overline{DSYNC}$" in the Serial Interface section for more information.

MD2-MD0 (Operating Mode) Bits—The MD2-MD0 bits initiate or enable the various calibration sequences, as follows:

MD2	MD1	MD0	OPERATING MODE
0	0	0	Normal Mode
0	0	1	Self-Calibration
0	1	0	System Offset Calibration
0	1	1	System Full-Scale Calibration
1	0	0	Pseudo System Calibration
1	0	1	Background Calibration
1	1	0	Sleep
1	1	1	Reserved

The Normal Mode, Background Calibration Mode, and Sleep Mode are permanent modes and the ADS1212/13 will remain in these modes indefinitely. All other modes are temporary and will revert to Normal Mode once the appropriate actions are complete. See the Calibration and Sleep Mode sections for more information.

DATA RATE (HZ)	DECI-MATION RATIO	DR12	DR11	DR10	DR9	DR8	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0
391	19	0	0	0	0	0	0	0	0	1	0	0	1	1
250	30	0	0	0	0	0	0	0	0	1	1	1	1	0
100	77	0	0	0	0	0	0	1	0	0	1	1	0	1
60	129	0	0	0	0	0	1	0	0	0	0	0	0	1
50	155	0	0	0	0	0	1	0	0	1	1	0	1	1
20	390	0	0	0	0	1	1	0	0	0	0	1	1	0
10	780	0	0	0	1	1	0	0	0	0	1	1	0	0
0.96	8000	1	1	1	1	1	0	1	0	0	0	0	0	0

Table XI. Decimation Ratios for Various Data Rates (Turbo Mode Rate of 1 and 1MHz clock).

G2-G0 (PGA Control) Bits—The G2-G0 bits control the gain setting of the PGA, as follows:

G2	G1	G0	GAIN SETTING	AVAILABLE TURBO MODE RATES	
0	0	0	1	1, 2, 4, 8, 16	Default
0	0	1	2	1, 2, 4, 8	
0	1	0	4	1, 2, 4	
0	1	1	8	1, 2	
1	0	0	16	1	

The gain is partially implemented by increasing the input capacitor sampling frequency, which is given by the following equation:

$$f_{SAMP} = G \bullet TMR \bullet f_{XIN}/128$$

where G is the gain setting and TMR is the Turbo Mode Rate. The product of G and TMR cannot exceed 16. The sampling frequency of the input capacitor directly relates to the analog input impedance. See the Programmable Gain Amplifier and Analog Input sections for more details.

CH1-CH0 (Channel Selection) Bits—The CH1 and CH0 bits control the input multiplexer on the ADS1213, as follows:

CH1	CH0	ACTIVE INPUT	
0	0	Channel 1	Default
0	1	Channel 2	
1	0	Channel 3	
1	1	Channel 4	

(For the ADS1212, CH1 and CH0 must always be zero.) The channel change takes effect when the last bit of byte 2 has been written to the Command Register. Output data will not be valid for the next three conversions despite the $\overline{DRDY}$ signal indicating that data is ready. On the fourth time that $\overline{DRDY}$ goes LOW after a channel change has been written to the Command Register, valid data will be present in the Data Output Register (see Figure 4).

SF2-SF0 (Turbo Mode Rate) Bits—The SF2-SF0 bits control the input capacitor sampling frequency and modulator rate, as follows:

SF2	SF1	SF0	TURBO MODE RATE	AVAILABLE PGA SETTINGS	
0	0	0	1	1, 2, 4, 8, 16	Default
0	0	1	2	1, 2, 4, 8	
0	1	0	4	1, 2, 4	
0	1	1	8	1, 2	
1	0	0	16	1	

The input capacitor sampling frequency and modulator rate can be calculated from the following equations:

$$f_{SAMP} = G \bullet TMR \bullet f_{XIN}/128$$

$$f_{MOD} = TMR \bullet f_{XIN}/128$$

where G is the gain setting and TMR is the Turbo Mode Rate. The sampling frequency of the input capacitor directly relates to the analog input impedance. The modulator rate relates to the power consumption of the ADS1212/13 and the output data rate. See the Turbo Mode, Analog Input, and Reference Input sections for more details.

DR12-DR0 (Decimation Ratio) Bits—The DR12-DR0 bits control the decimation ratio of the ADS1212/13. In essence, these bits set the number of modulator results which are used in the digital filter to compute each individual conversion result. Since the modulator rate depends on both the ADS1212/13 clock frequency and the Turbo Mode Rate, the actual output data rate is given by the following equation:

$$f_{DATA} = f_{XIN} \bullet TMR/(128 \bullet (\text{Decimation Ratio} + 1))$$

where TMR is the Turbo Mode Rate. Table XI shows various data rates and corresponding decimation ratios (with a 1MHz clock). Valid decimation ratios are from 19 to 8000. Outside of this range, the digital filter will compute results incorrectly due to inadequate or too much data.

Data Output Register (DOR)

The DOR is a 24-bit register which contains the most recent conversion result (see Table XII). This register is updated with a new result just prior to $\overline{DRDY}$ going LOW. If the contents of the DOR are not read within a period of time defined by $1/f_{DATA} - 24 \bullet (1/f_{XIN})$, then a new conversion result will overwrite the old. ($\overline{DRDY}$ is forced HIGH prior to the DOR update, unless a read is in progress).

Most Significant Bit			Byte 2				
DOR23	DOR22	DOR21	DOR20	DOR19	DOR18	DOR17	DOR16
Byte 1							
DOR15	DOR14	DOR13	DOR12	DOR11	DOR10	DOR9	DOR8
Byte 0						Least Significant Bit	
DOR7	DOR6	DOR5	DOR4	DOR3	DOR2	DOR1	DOR0

TABLE XII. Data Output Register.

The contents of the DOR can be in Two's Complement or Offset Binary format. This is controlled by the DF bit of the Command Register. In addition, the contents can be limited to unipolar data only with the U/$\overline{B}$ bit of the Command Register.

Offset Calibration Register (OCR)

The OCR is a 24-bit register which contains the offset correction factor that is applied to the conversion result before it is placed in the Data Output Register (see Table XIII). In most applications, the contents of this register will be the result of either a self-calibration or a system calibration.

The OCR is both readable and writeable via the serial interface. For applications requiring a more accurate offset calibration, multiple calibrations can be performed, each resulting OCR value read, the results averaged, and a more precise offset calibration value written back to the OCR.

The actual OCR value will change from part-to-part and with configuration, temperature, and power supply. Thus, the actual OCR value for any arbitrary situation cannot be accurately predicted. That is, a given system offset could not be corrected simply by measuring the error externally, computing a correction factor, and writing that value to the OCR. In addition, be aware that the contents of the OCR are not used to directly correct the conversion result. Rather, the correction is a function of the OCR value. This function is linear and two known points can be used as a basis for interpolating intermediate values for the OCR. Consult the Calibration section for more details.

Most Significant Bit			**Byte 2**				
OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	OCR17	OCR16
			Byte 1				
OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	OCR9	OCR8
			Byte 0			Least Significant Bit	
OCR7	OCR6	OCR5	OCR4	OCR3	OCR2	OCR1	OCR0

TABLE XIII. Offset Calibration Register.

The contents of the OCR are in Two's Complement format. This is not affected by the DF bit in the Command Register.

Full-Scale Calibration Register (FCR)

The FCR is a 24-bit register which contains the full-scale correction factor that is applied to the conversion result before it is placed in the Data Output Register (see Table XIV). In most applications, the contents of this register will be the result of either a self-calibration or a system calibration.

Most Significant Bit			**Byte 2**				
FSR23	FSR22	FSR21	FSR20	FSR19	FSR18	FSR17	FSR16
			Byte 1				
FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR9	FSR8
			Byte 0			Least Significant Bit	
FSR7	FSR6	FSR5	FSR4	FSR3	FSR2	FSR1	FSR0

TABLE XIV. Full-Scale Calibration Register.

The FCR is both readable and writable via the serial interface. For applications requiring a more accurate full-scale calibration, multiple calibrations can be performed, each resulting FCR value read, the results averaged, and a more precise calibration value written back to the FCR.

The actual FCR value will change from part-to-part and with configuration, temperature, and power supply. Thus, the actual FCR value for any arbitrary situation cannot be accurately predicted. That is, a given system full-scale error cannot be corrected simply by measuring the error externally, computing a correction factor, and writing that value to the FCR. In addition, be aware that the contents of the FCR are not used to directly correct the conversion result. Rather, the correction is a function of the FCR value. This function is linear and two known points can be used as a basis for interpolating intermediate values for the FCR. Consult the Calibration section for more details. The contents of the FCR are in unsigned binary format. This is not affected by the DF bit in the Command Register.

TIMING

Table XV and Figures 13 through 21 define the basic digital timing characteristics of the ADS1212/13. Figure 13 and the associated timing symbols apply to the X_{IN} input signal. Figures 14 through 20 and associated timing symbols apply to the serial interface signals (SCLK, SDIO, SDOUT, and $\overline{CS}$) and their relationship to $\overline{DRDY}$. The serial interface is discussed in detail in the Serial Interface section. Figure 21 and the associated timing symbols apply to the maximum $\overline{DRDY}$ rise and fall times.

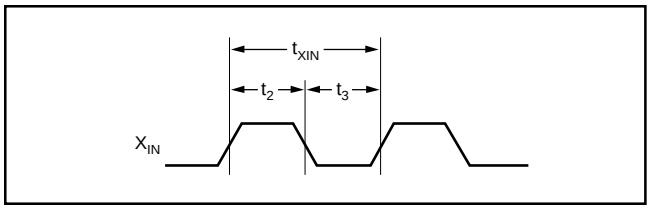


FIGURE 13. X_{IN} Clock Timing.

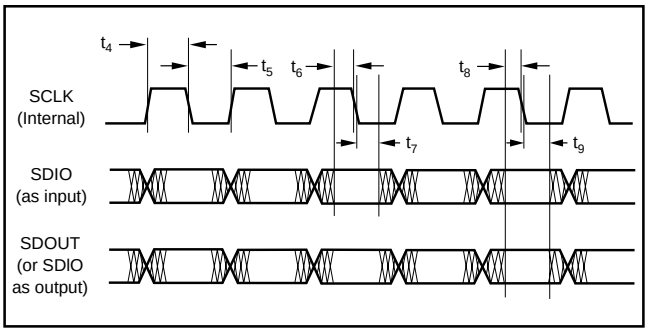


FIGURE 14. Serial Input/Output Timing, Master Mode.

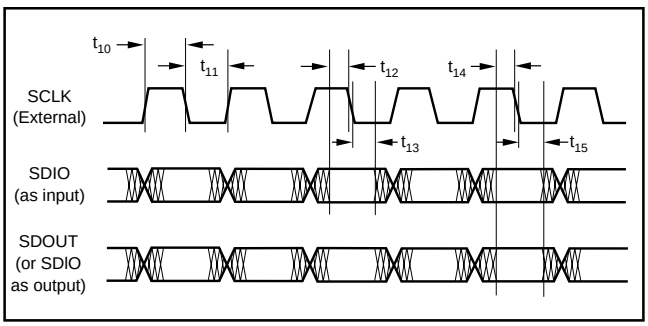


FIGURE 15. Serial Input/Output Timing, Slave Mode.

SYMBOL	DESCRIPTION	MIN	NOM	MAX	UNITS
f_{XIN}	X_{IN} Clock Frequency	0.5	1	2.5	MHz
t_{XIN}	X_{IN} Clock Period	400		2000	ns
t_2	X_{IN} Clock High	0.4 • t_{XIN}			ns
t_3	X_{IN} Clock LOW	0.4 • t_{XIN}			ns
t_4	Internal Serial Clock HIGH		2 • t_{XIN}		ns
t_5	Internal Serial Clock LOW		2 • t_{XIN}		ns
t_6	Data In Valid to Internal SCLK Falling Edge (Setup)	40			ns
t_7	Internal SCLK Falling Edge to Data In Not Valid (Hold)	20			ns
t_8	Data Out Valid to Internal SCLK Falling Edge (Setup)	2 • t_{XIN} –25			ns
t_9	Internal SCLK Falling Edge to Data Out Not Valid (Hold)	2 • t_{XIN}			ns
t_{10}	External Serial Clock HIGH	5 • t_{XIN}			ns
t_{11}	External Serial Clock LOW	5 • t_{XIN}			ns
t_{12}	Data In Valid to External SCLK Falling Edge (Setup)	40			ns
t_{13}	External SCLK Falling Edge to Data In Not Valid (Hold)	20			ns
t_{14}	Data Out Valid to External SCLK Falling Edge (Setup)	t_{XIN} –40			ns
t_{15}	External SCLK Falling Edge to Data Out Not Valid (Hold)	4 • t_{XIN}			ns
t_{16}	Falling Edge of $\overline{DRDY}$ to First SCLK Rising Edge (Mode, $\overline{CS}$ Tied LOW)		12 • t_{XIN}		ns
t_{17}	Falling Edge of Last SCLK for INSR to Rising Edge of First SCLK for Register Data (Master Mode)		10 • t_{XIN}		ns
t_{18}	Falling Edge of Last SCLK for Register Data to Rising Edge of $\overline{DRDY}$ (Master Mode)		6 • t_{XIN}		ns
t_{19}	Falling Edge of Last SCLK for INSR to Rising Edge of First SCLK for Register Data (Slave Mode)	13 • t_{XIN}			ns ns
t_{20}	Falling Edge of Last SCLK for Register Data to Rising Edge of $\overline{DRDY}$ (Slave Mode)	8 • t_{XIN}		10 • t_{XIN}	ns
t_{21}	Falling Edge of $\overline{DRDY}$ to Falling Edge of $\overline{CS}$ (Master and Slave Mode)	3 • t_{XIN}			ns
t_{22}	Falling Edge of $\overline{CS}$ to Rising Edge of SCLK (Master Mode)	10 • t_{XIN}		12 • t_{XIN}	ns
t_{23}	Rising Edge of $\overline{DRDY}$ to Rising Edge of $\overline{CS}$ (Master and Slave Mode)	2 • t_{XIN}			ns
t_{24}	Falling Edge of $\overline{CS}$ to Rising Edge of SCLK (Slave Mode)	11 • t_{XIN}			ns
t_{25}	Falling Edge of Last SCLK for INSR to SDIO Tri-state (Master Mode)		4 • t_{XIN}		ns
t_{26}	SDIO as Output to Rising Edge of First SCLK for Register Data (Master and Slave Modes)		4 • t_{XIN}		ns
t_{27}	Falling Edge of Last SCLK for INSR to SDIO Tri-state (Slave Mode)	6 • t_{XIN}		8 • t_{XIN}	ns
t_{28}	SDIO Tri-state Time (Master and Slave Modes)		2 • t_{XIN}		ns
t_{29}	Falling Edge of Last SCLK for Register Data to SDIO Tri-State (Master Mode)		2 • t_{XIN}		ns
t_{30}	Falling Edge of Last SCLK for Register Data to SDIO Tri-state (Slave Mode)	4 • t_{XIN}		6 • t_{XIN}	ns
t_{31}	$\overline{DRDY}$ Fall Time			30	ns
t_{32}	$\overline{DRDY}$ Rise Time			30	ns
t_{33}	Minimum $\overline{DSYNC}$ LOW Time	21 • t_{XIN}			ns
t_{34}	$\overline{DSYNC}$ Valid HIGH to Falling Edge of X_{IN} (for Exact Synchronization of Multiple Converters Only)	10			ns
t_{35}	Falling Edge of X_{IN} to $\overline{DSYNC}$ Not Valid LOW (for Exact Synchronization of Multiple Converters Only)	10			ns
t_{36}	Falling Edge of Last SCLK for Register Data to Rising Edge of First SCLK of next INSR (Slave Mode, $\overline{CS}$ Tied LOW)	41 • t_{XIN}			ns
t_{37}	Rising Edge of $\overline{CS}$ to Falling Edge of $\overline{CS}$ (Slave Mode, Using $\overline{CS}$)	22 • t_{XIN}			ns
t_{38}	Falling Edge of $\overline{DRDY}$ to First SCLK Rising Edge (Slave Mode, $\overline{CS}$ Tied LOW)	11 • t_{XIN}			ns

TABLE XV. Digital Timing Characteristics.

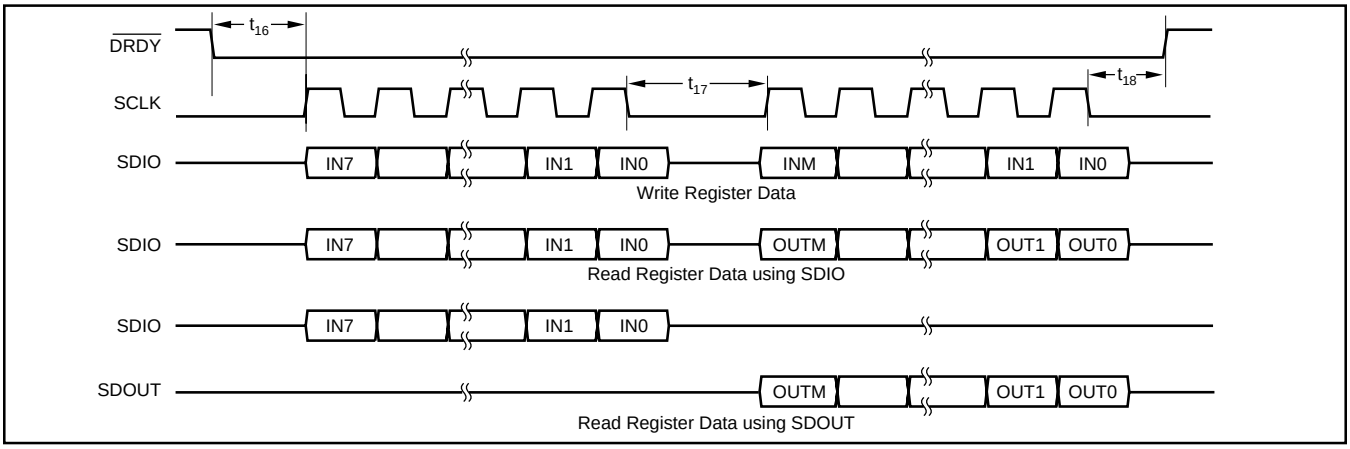


FIGURE 16. Serial Interface Timing ($\overline{CS}$ LOW), Master Mode.

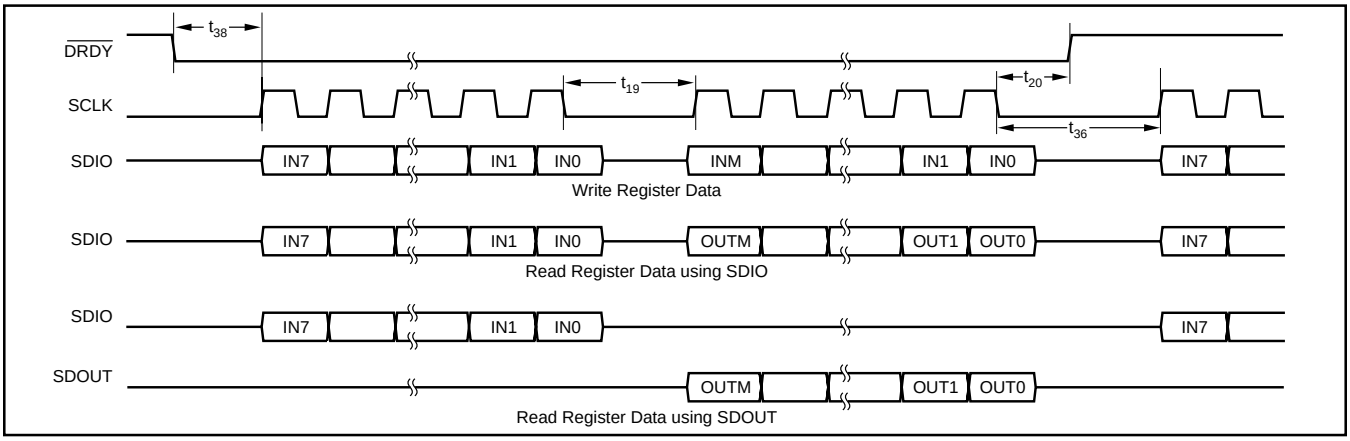


FIGURE 17. Serial Interface Timing ($\overline{CS}$ LOW), Slave Mode.

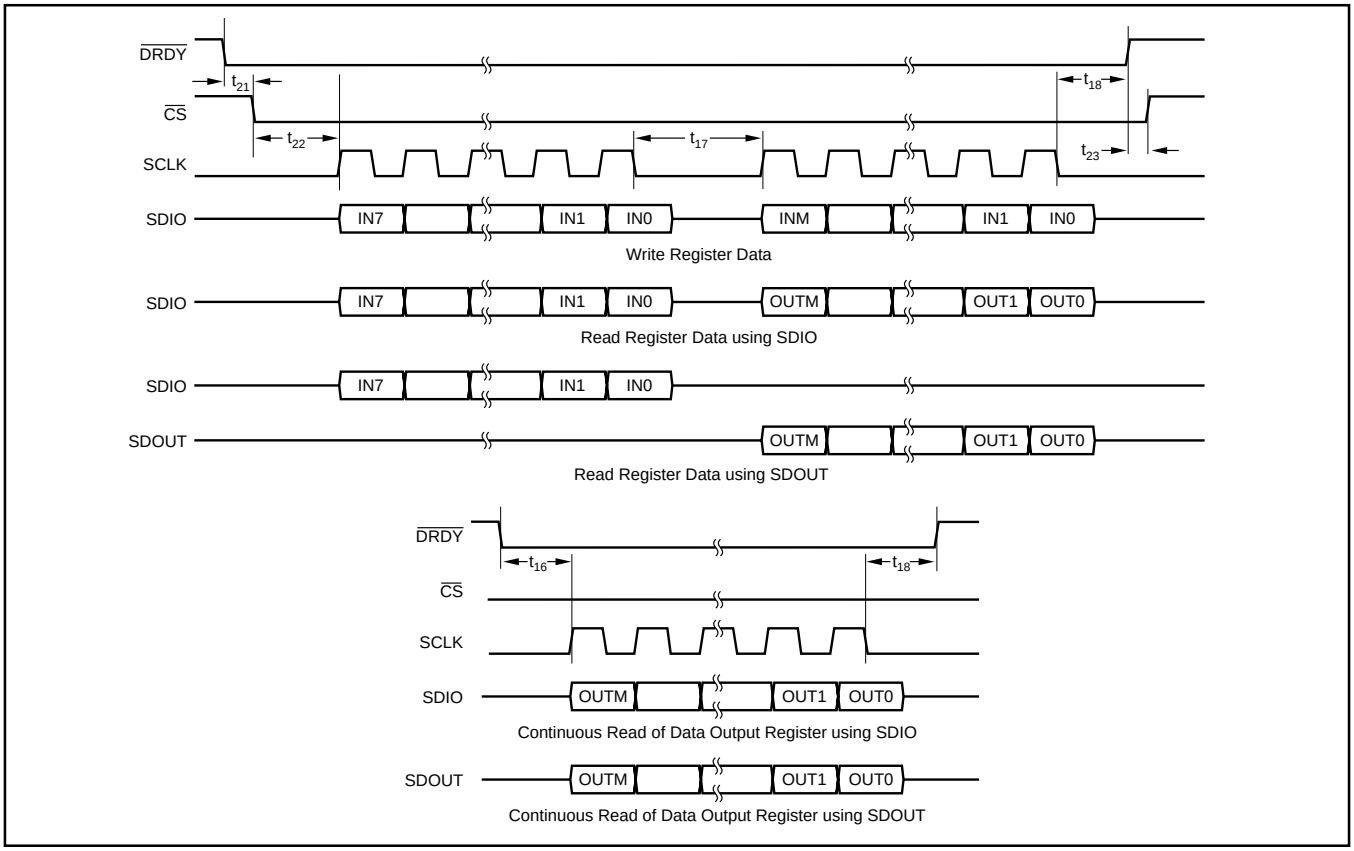


FIGURE 18. Serial Interface Timing (Using $\overline{CS}$), Master Mode.

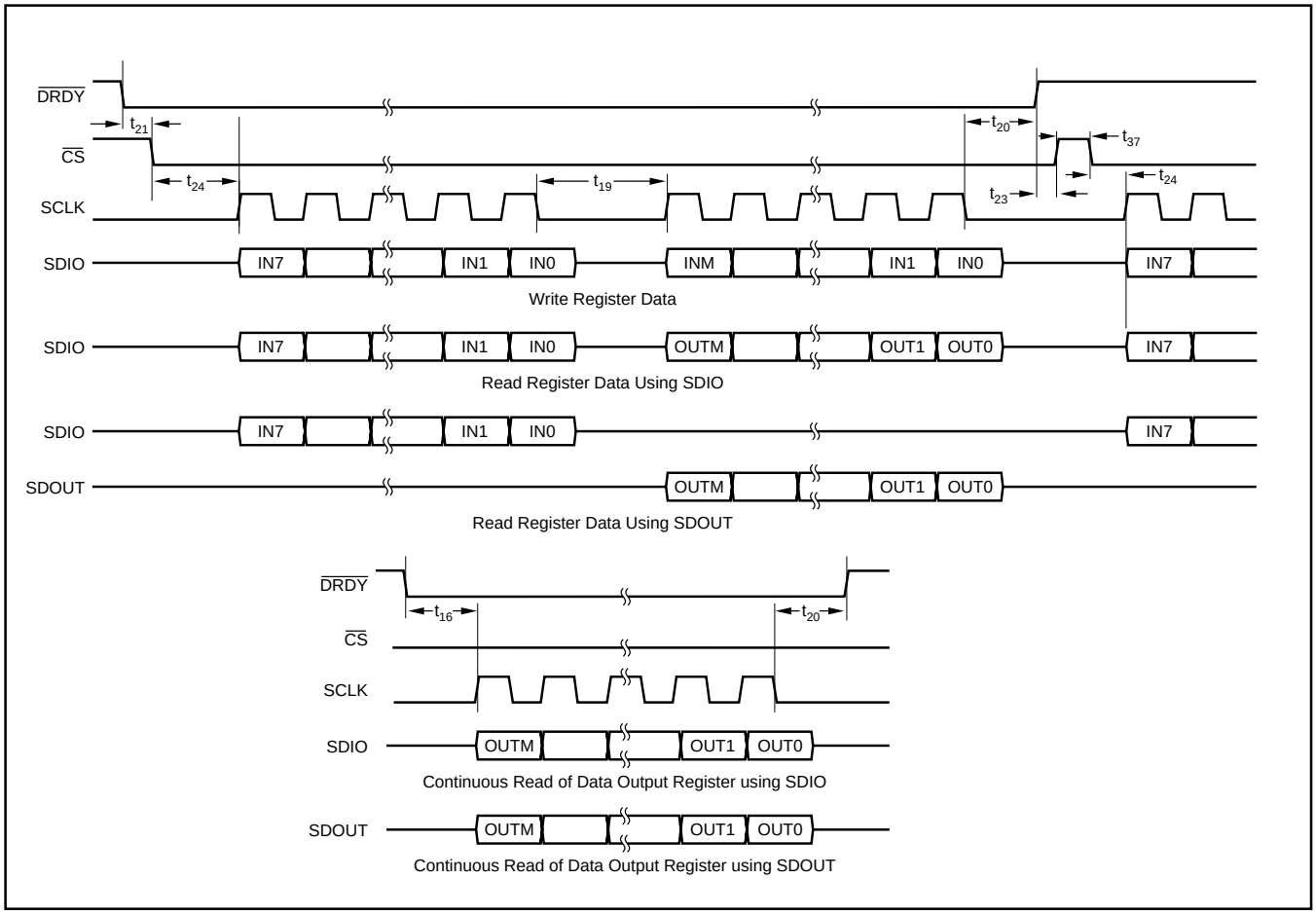


FIGURE 19. Serial Interface Timing (Using $\overline{CS}$), Slave Mode.

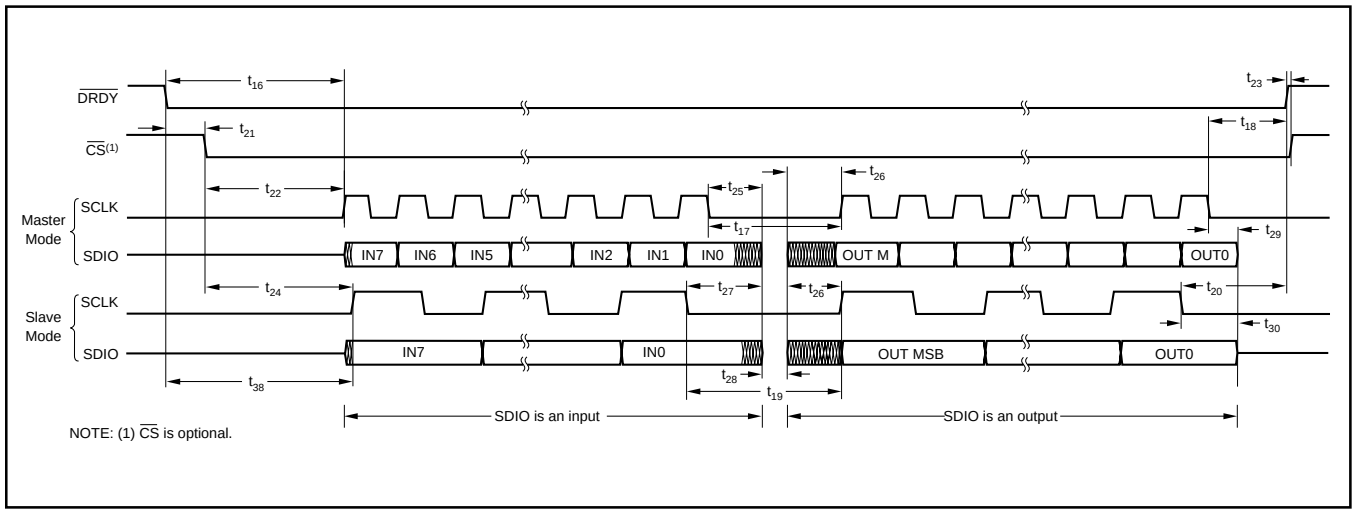


FIGURE 20. SDIO Input to Output Transition Timing.

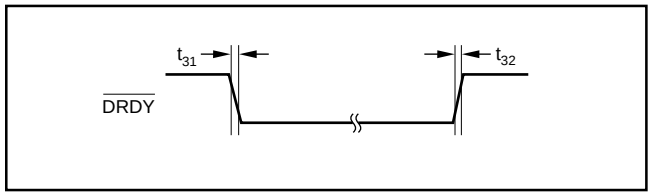


FIGURE 21. $\overline{DRDY}$ Rise and Fall Time.

Synchronizing Multiple Converters

A negative going pulse on $\overline{DSYNC}$ can be used to synchronize multiple ADS1212/13s. This assumes that each ADS1212/13 is driven from the same master clock and is set to the same Decimation Ratio and Turbo Mode Rate. The affect that this signal has on data output timing in general is discussed in the Serial Interface section.

The concern here is what happens if the $\overline{DSYNC}$ input is completely asynchronous to this master clock. If the $\overline{DSYNC}$ input rises at a critical point in relation to the master clock input, then some ADS1212/13s may start-up one X_{IN} clock cycle before the others. Thus, the output data will be synchronized, but only to within one X_{IN} clock cycle.

For many applications, this will be more than adequate. In these cases, the timing symbols which relate the $\overline{DSYNC}$ signal to the X_{IN} signal can be ignored. For other multiple-converter applications, this one X_{IN} clock cycle difference could be a problem. These types of applications would include using the $\overline{DRDY}$ and/or the SCLK output from one ADS1212/13 as the "master" signal for all converters.

To ensure exact synchronization to the same X_{IN} edge, the timing relationship between the $\overline{DSYNC}$ and X_{IN} signals, as shown in Figure 22, must be observed. Figure 23 shows a simple circuit which can be used to clock multiple ADS1212/13s from one ADS1212/13, as well as to ensure that an asynchronous $\overline{DSYNC}$ signal will exactly synchronize all the converters.

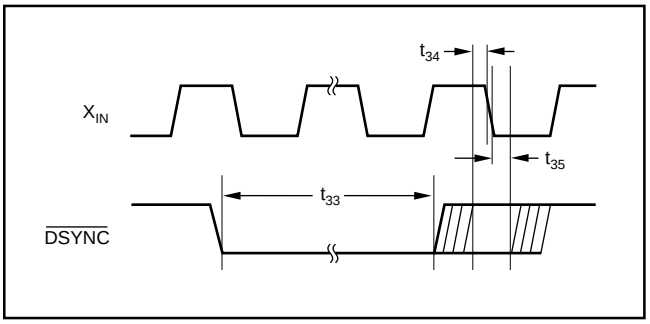


FIGURE 22. $\overline{DSYNC}$ to X_{IN} Timing for Synchronizing Mutliple ADS1212/13s.

SERIAL INTERFACE

The ADS1212/13 includes a flexible serial interface which can be connected to microcontrollers and digital signal processors in a variety of ways. Along with this flexibility, there is also a good deal of complexity. This section describes the trade-offs between the different types of interfacing methods in a top-down approach—starting with the overall flow and control of serial data, moving to specific interface examples, and then providing information on various issues related to the serial interface.

Multiple Instructions

The general timing diagrams which appear throughout this data sheet show serial communication to and from the ADS1212/13 occurring during the $\overline{DRDY}$ LOW period (see Figures 4 through 10 and Figure 36). This communication represents one instruction that is executed by the ADS1212/13, resulting in a single read or write of register data.

However, more than one instruction can be executed by the ADS1212/13 during any given conversion period (see Figure 24). Note that $\overline{DRDY}$ remains HIGH during the subsequent instructions. There are several important restrictions on how and when multiple instructions can be issued during any one conversion period.

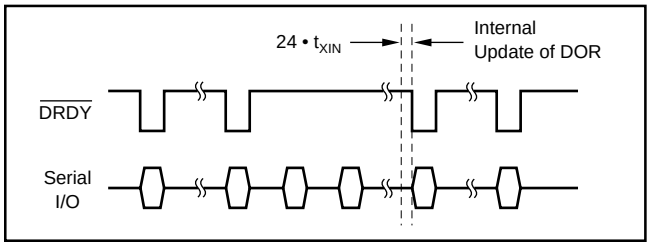


FIGURE 24. Timing of Data Output Register Update.

The first restriction is that the converter must be in the Slave Mode. There is no provision for multiple instructions when the ADS1212/13 is operating in the Master Mode. The second is that some instructions will produce invalid results if started at the end of one conversion period and carried into the start of the next conversion period.

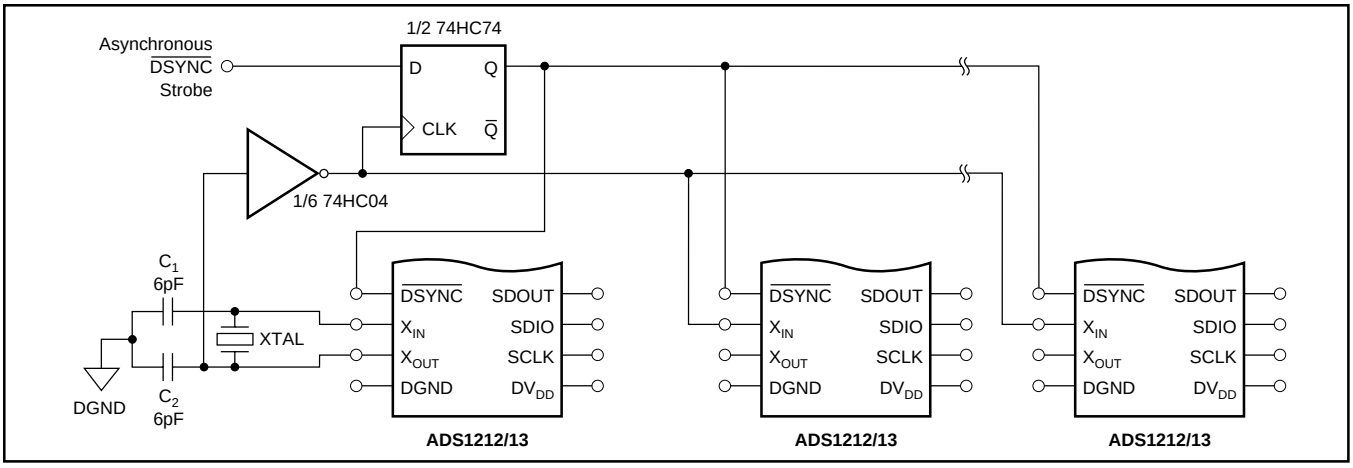


FIGURE 23. Exactly Synchronizing Multiple ADS1212/13s to an Asynchronous $\overline{DSYNC}$ Signal.

For example, Figure 24 shows that just prior to the $\overline{DRDY}$ signal going LOW, the internal Data Output Register (DOR) is updated. This update involves the Offset Calibration Register (OCR) and the Full-Scale Register (FSR). If the OCR or FSR are being written, their final value may not be correct, and the result placed into the DOR will certainly not be valid. Problems can also arise if certain bits of the Command Register are being changed.

Note that reading the Data Output Register is an exception. If the DOR is being read when the internal update is initiated, the update is blocked. The old output data will remain in the DOR and the new data will be lost. The old data will remain valid until the read operation has completed. In general, multiple instructions may be issued, but the last one in any conversion period should be complete within 24 • X_{IN} clock periods of the next $\overline{DRDY}$ LOW time. In this usage, "complete" refers to the point where $\overline{DRDY}$ rises in Figures 17 and 19 (in the Timing Section). Consult Figures 25 and 26 for the flow of serial data during any one conversion period.

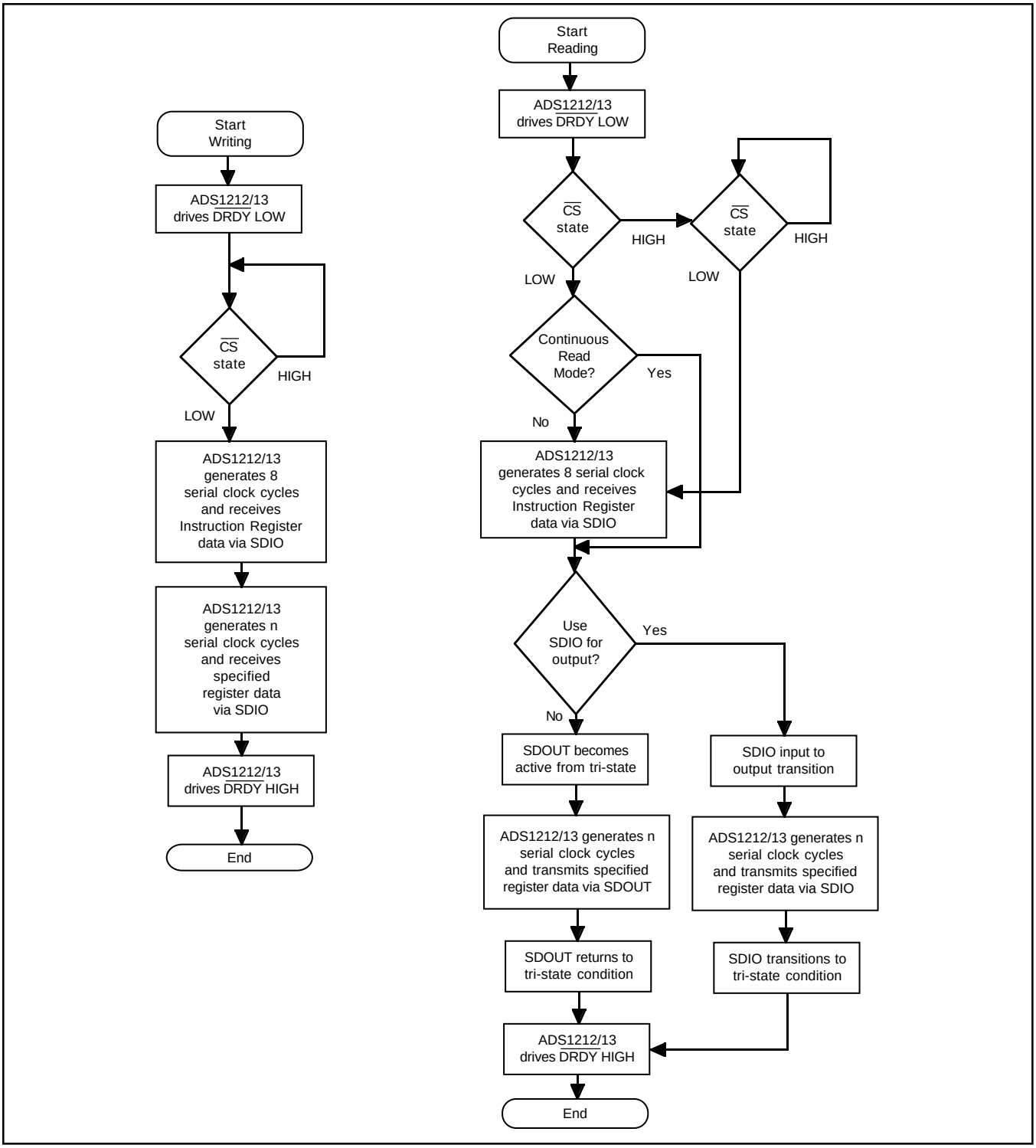


FIGURE 25. Flowchart for Writing and Reading Register Data, Master Mode.

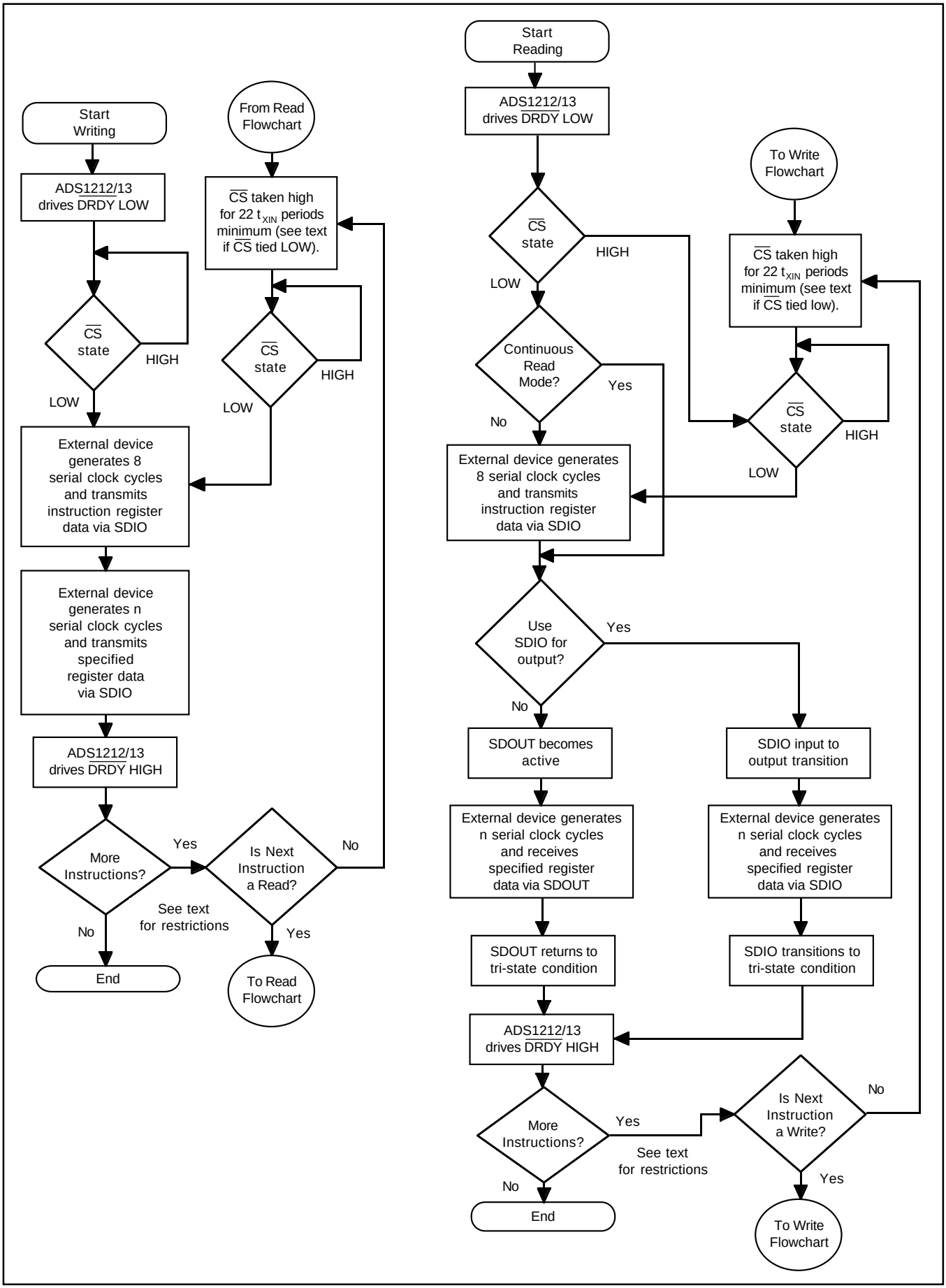


FIGURE 26. Flowchart for Writing and Reading Register Data, Slave Mode.

Using $\overline{CS}$ and Continuous Read Mode

The serial interface may make use of the $\overline{CS}$ signal, or this input may simply be tied LOW. There are several issues associated with choosing to do one or the other.

The $\overline{CS}$ signal does not directly control the tri-state condition of the SDOUT or SDIO output. These signals are normally in the tri-state condition. They only become active when serial data is being transmitted from the ADS1212/13. If the ADS1212/13 is in the middle of a serial transfer and SDOUT or SDIO is an output, taking $\overline{CS}$ HIGH will not tri-state the output signal.

If there are multiple serial peripherals utilizing the same serial I/O lines and communication may occur with any peripheral at any time, then the $\overline{CS}$ signal must be used. The ADS1212/13 may be in the Master Mode or the Slave Mode. In the Master Mode, the $\overline{CS}$ signal is used to hold-off serial communication with a "ready" ($\overline{DRDY}$ LOW) ADS1212/13 until the main controller can accommodate the communication. In the Slave Mode, the $\overline{CS}$ signal is used to enable communication with the ADS1212/13.

The $\overline{CS}$ input has another use. If the $\overline{CS}$ state is left LOW after a read of the Data Output Register has been performed, then the next time that $\overline{DRDY}$ goes LOW, the ADS1212/13 Instruction Register will not be entered. Instead, the Instruction Register contents will be re-used, and the new contents of the Data Output Register, or some part thereof, will be transmitted. This will occur as long as $\overline{CS}$ is LOW and not toggled.

This mode of operation is called the Continuous Read Mode and is shown in the read flowcharts of Figures 25 and 26. It is also shown in the Timing Diagrams of Figures 18 and 19 in the Timing section. Note that once $\overline{CS}$ has been taken HIGH, the Continuous Read Mode will be enabled (but not entered) and can never be disabled. The mode is actually entered and exited as described above.

Power-On Conditions for SDIO

Even if the SDIO connection will be used only for input, there is one important item to consider regarding SDIO. This only applies when the ADS1212/13 is in the Master Mode and $\overline{CS}$ will be tied LOW. At power-up, the serial I/O lines of most microcontrollers and digital signal processors will be in a tri-state condition, or they will be configured as inputs. When power is applied to the ADS1212/13, it will begin operating as defined by the default condition of the Command Register (see Table X in the System Configuration section). This condition defines SDIO as the data output pin.

Since the ADS1212/13 is in the Master Mode and $\overline{CS}$ is tied LOW, the serial clock will run whenever $\overline{DRDY}$ is LOW and an instruction will be entered and executed. If the SDIO line is HIGH, as it might be with an active pull-up, then the instruction is a read operation and SDIO will become an output every $\overline{DRDY}$ LOW period—for 32 serial clock cycles. When the serial port on the main controller is enabled, signal contention could result.

The recommended solution to this problem is to actively pull SDIO LOW. If SDIO is LOW when the ADS1212/13 enters the instruction byte, then the resulting instruction is a write of one byte of data to the Data Output Register, which results in no internal operation.

If the SDIO signal cannot be actively pulled LOW, then another possibility is to time the initialization of the controller's serial port such that it becomes active between adjacent $\overline{DRDY}$ LOW periods. The default configuration for the ADS1212/13 produces a data rate of 326Hz—a conversion period of 2.9ms. This time should be more than adequate for most microcontrollers and DSPs to monitor $\overline{DRDY}$ and initialize the serial port at the appropriate time.

Master Mode

The Master Mode is active when the MODE input is HIGH. All serial clock cycles will be produced by the ADS1212/13 in this mode, and the SCLK pin is configured as an output. The frequency of the serial clock will be one-quarter of the X_{IN} frequency. Multiple instructions cannot be issued during a single conversion period in this mode—only one instruction per conversion cycle is possible.

The Master Mode will be difficult for some microcontrollers, particularly when the X_{IN} input frequency is greater than 2MHz, as the serial clock may exceed the microcontroller's maximum serial clock frequency. For the majority of digital signal processors, this will be much less of a concern. In addition, if SDIO is being used as an input and an output, then the transition time from input to output may be a concern. This will be true for both microcontrollers and DSPs. See Figure 20 in the Timing section.

Note that if $\overline{CS}$ is tied LOW, there are special considerations regarding SDIO as outlined previously in this section. Also note that if $\overline{CS}$ is being used to control the flow of data from the ADS1212/13 and it remains HIGH for one or more conversion periods, the ADS1212/13 will operate properly. However, the result in the Data Output Register will be lost when it is overwritten by each new result. Just prior to this update, $\overline{DRDY}$ will be forced HIGH and will return LOW after the update.

Slave Mode

Most systems will use the ADS1212/13 in the Slave Mode. This mode allows multiple instructions to be issued per conversion period as well as allowing the main controller to set the serial clock frequency and pace the serial data transfer. The ADS1212/13 is in the Slave Mode when the MODE input is LOW.

There are several important items regarding the serial clock for this mode of operation. The maximum serial clock frequency cannot exceed the ADS1212/13 X_{IN} frequency divided by 10 (see Figure 15 in the Timing section).

As with the Master Mode of operation, when using SDIO as edge of the last serial clock cycle of the instruction byte, the SDIO pin will begin its transition from input to output. Between six and eight X_{IN} cycles after this falling edge, the SDIO pin will become an output. This transition may be too fast for some microcontrollers and digital signal processors.

If a serial communication does not occur during any conversion period, the ADS1212/13 will continue to operate properly. However, the results in the Data Output Register will be lost when they are overwritten by the new result at the start of the next conversion period. Just prior to this update, $\overline{\text{DRDY}}$ will be forced HIGH and will return LOW after the update.

Making Use of $\overline{\text{DSYNC}}$

The $\overline{\text{DSYNC}}$ input pin and the DSYNC write bit in the Command Register reset the current modulator count to zero. This causes the current conversion cycle to proceed as normal, but all modulator outputs from the last data output to the point where DSYNC is asserted are discarded. Note that the previous two data outputs are still present in the ADS1212/13 internal memory. Both will be used to compute the next conversion result, and the most recent one will be used to compute the result two conversions later. DSYNC does not reset the internal data to zero.

There are two main uses of DSYNC. In the first case, DSYNC allows for synchronization of multiple converters. In regards to the $\overline{\text{DSYNC}}$ input pin, this case was discussed under "Synchronizing Multiple Converters" in the Timing section. In regards to the DSYNC bit, it will be difficult to set all of the converter's DSYNC bits at the same time unless all of the converters are in the Slave Mode and the same instruction can be sent to all of the converters at the same time.

The second use of DSYNC is to reset the modulator count to zero in order to obtain valid data as quickly as possible. For example, if the input channel is changed on the ADS1213, the current conversion cycle will be a mix of the old channel and the new channels. Thus, four conversions are needed in order to ensure valid data. However, if the channel is changed and then DSYNC is used to reset the modulator count, the modulator data at the end of the current conversion cycle will be entirely from the new channel. After two additional conversion cycles, the output data will be completely valid. Note that the conversion cycle in which DSYNC is used will be slightly longer than normal. Its length will depend on when DSYNC was set.

Reset, Power-On Reset and Brown-Out

The ADS1212/13 contains an internal power-on reset circuit. If the power supply ramp rate is greater than 50mV/ms, this circuit will be adequate to ensure the device powers up correctly. (Due to oscillator settling considerations, communication to and from the ADS1212/13 should not occur for at least 25ms after power is stable).

If this requirement cannot be met or if the circuit has brown-out considerations, the timing diagram of Figure 27 can be used to reset the ADS1212/13. This timing applies only when the ADS1212/13 is in the Slave Mode and accomplishes the reset by controlling the duty cycle of the SCLK input. In general, reset is required after power-up, after a brown-out has been detected, or when a watchdog timer event has occured.

If the ADS1212/13 is in the Master Mode, a reset of the device is not possible. If the power supply does not meet the minimum ramp rate requirement or brown-out is of concern, low on-resistance MOSFETs or equivalent should be used to control power to the ADS1212/13. When powered down, the device should be left unpowered for at least 300ms before power is reapplied. An alternate method would be to control the MODE pin and temporarily place the ADS1212/13 in the Slave Mode while a reset is initiated as shown in Figure 27.

Two-Wire Interface

For a two-wire interface, the Master Mode of operation may be preferable. In this mode, serial communication occurs only when data is ready, informing the main controller as to the status of the ADS1212/13. The disadvantages are that the ADS1212/13 must have a dedicated serial port on the main controller and only one instruction can be issued per data ready period.

In the Slave Mode, the main controller must read and write to the ADS1212/13 "blindly." Writes to the internal registers, such as the Command Register or Offset Calibration Register, might occur during an update of the Data Output Register. This can result in invalid data in the DOR. A two-wire interface can be used if the main controller can read and/or write to the converter either much slower or much faster than the data rate. For example, if much faster, the main controller can use the $\overline{\text{DRDY}}$ bit to determine when data is becoming valid (polling it multiple times during one conversion cycle). Thus, the controller obtains some idea of when to write to the internal registers. If much slower, then reads of the DOR might always return valid data (mulitple conversions have occurred since the last read of the DOR or since any write of the internal registers).

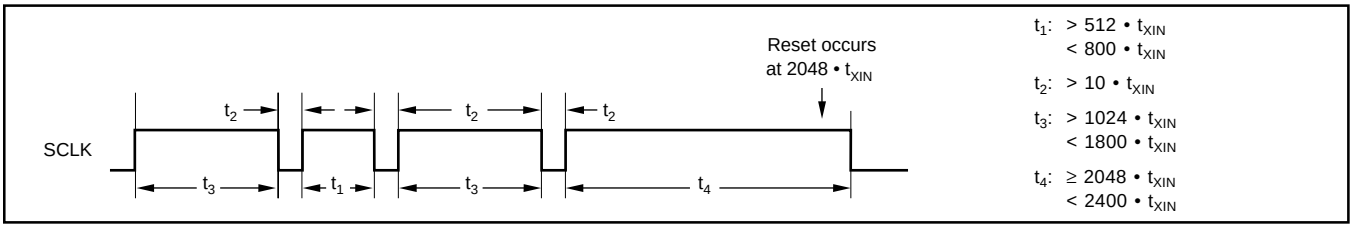


FIGURE 27. Resetting the ADS1212/13 (Slave Mode only).

Three-Wire Interface

Figure 28 shows a three-wire interface with a 8xC32 microprocessor. Note that the Slave Mode is selected and the SDIO pin is being used for input and output.

Figure 29 shows a different type of three-wire interface with an 8xC51 microprocessor. Here, the Master Mode is used. The interface signals consist of SDOUT, SDIO, and SCLK.

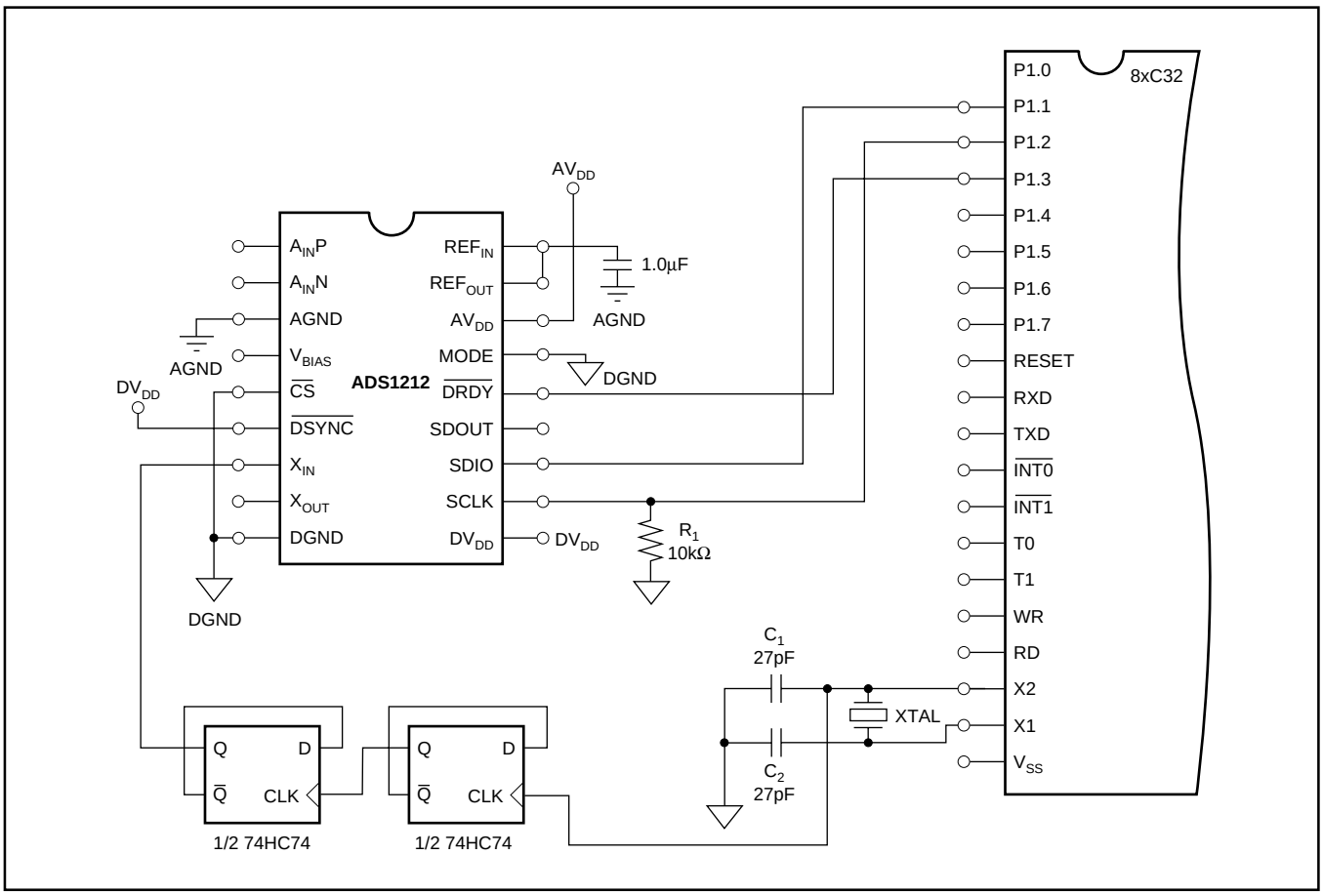


FIGURE 28. Three-Wire Interface with a 8xC32 Microprocessor.

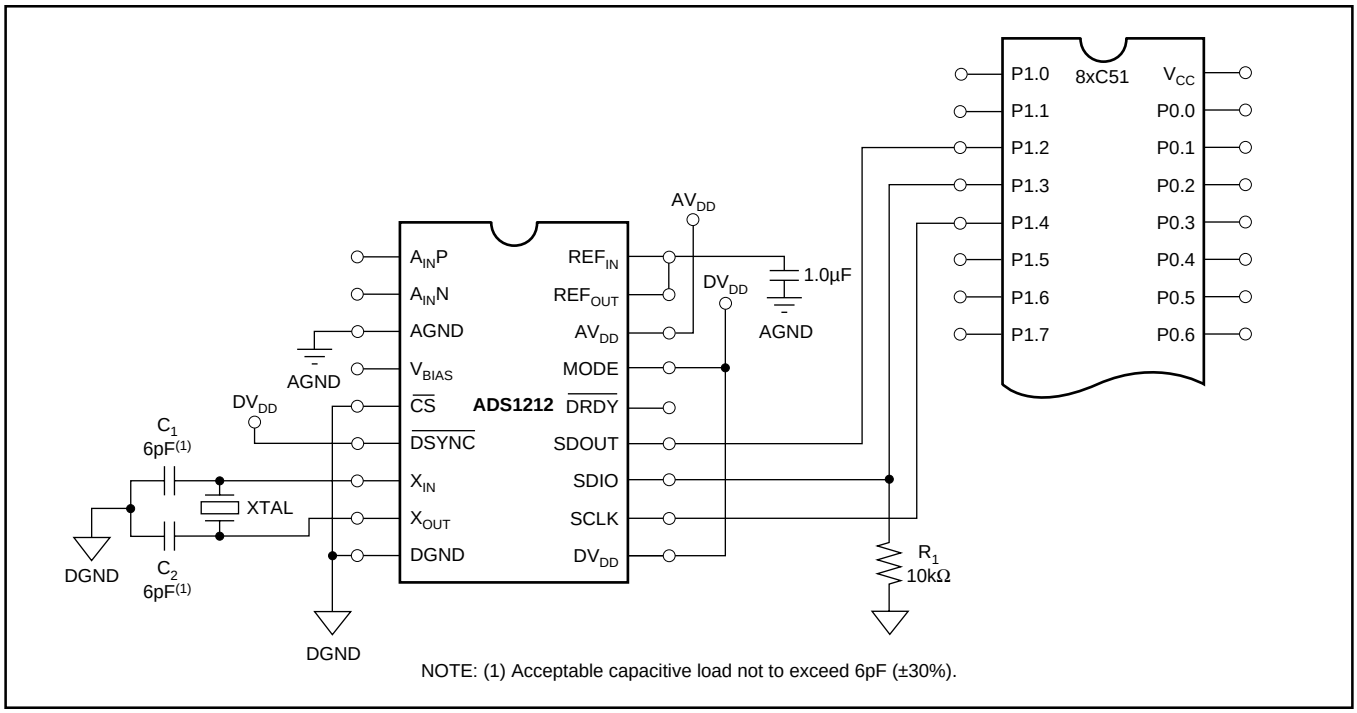


FIGURE 29. Three-Wire Interface with a 8xC51 Microprocessor.

Four-Wire Interface

Figure 30 shows a four-wire interface with a 8xC32 microprocessor. Again, the Slave Mode is being used.

Multi-Wire Interface

Figures 31 and 32 show multi-wire interfaces with a 8xC51 or 68HC11 microprocessor. In these interfaces, the mode of the ADS1212/13 is actually controlled dynamically. This could be extremely useful when the ADS1212/13 is to be used in a wide variety of ways. For example, it might be desirable to have the ADS1212/13 produce data at a steady rate and to have the converter operating in the Continuous Read Mode. But for system calibration, the Slave Mode might be preferred because multiple instructions can be issued per conversion period.

Note that the MODE input should not be changed in the middle of a serial transfer. This could result in misoperation of the device. A Master/Slave Mode change will not affect the output data.

Note that the X_{IN} input can also be controlled. It is possible with some microcontrollers and digital signal processors to produce a continuous serial clock, which could be connected to the X_{IN} input. The frequency of the clock is often settable over some range. Thus, the power dissipation of the ADS1212/13 could be dynamically varied by changing both the Turbo Mode and X_{IN} input, trading off conversion speed and resolution for power consumption.

I/O Recovery

If serial communication stops during an instruction or data transfer for longer than $4 \cdot t_{DATA}$, the ADS1212/13 will reset its serial interface. This will not affect the internal registers. The main controller must not continue the transfer after this event, but must restart the transfer from the beginning.

This feature is very useful if the main controller can be reset at any point. After reset, simply wait $8 \cdot t_{DATA}$ before starting serial communication.

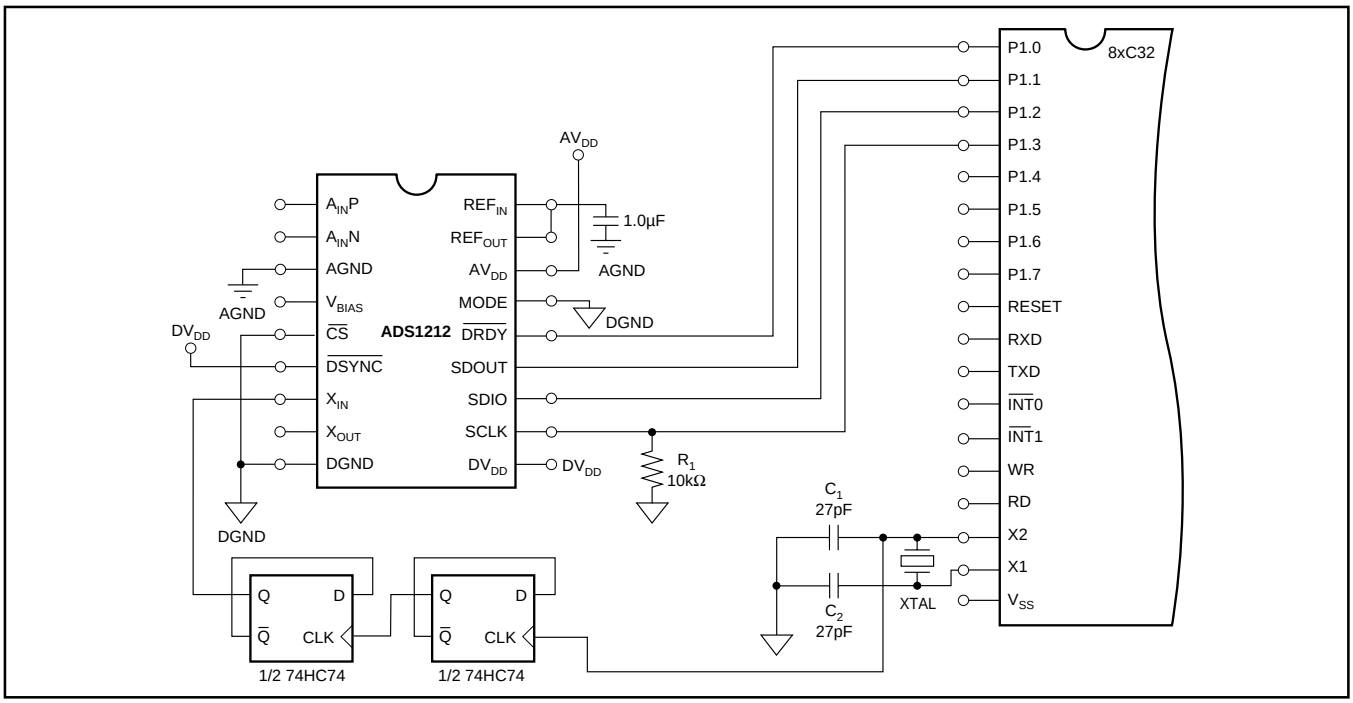


FIGURE 30. Four-Wire Interface with a 8xC32 Microprocessor.

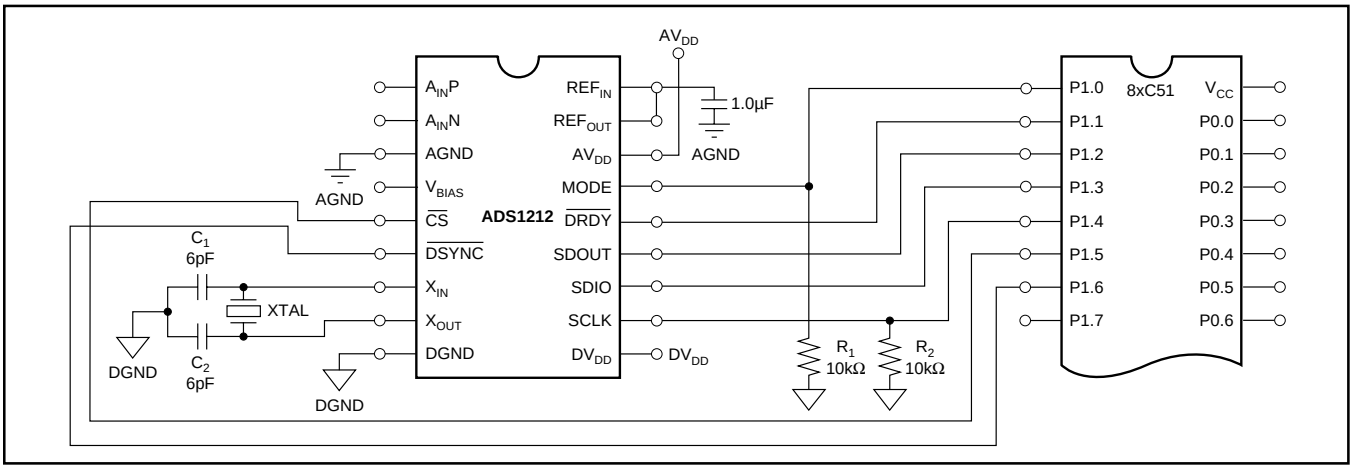


FIGURE 31. Full Interface with a 8xC51 Microprocessor.

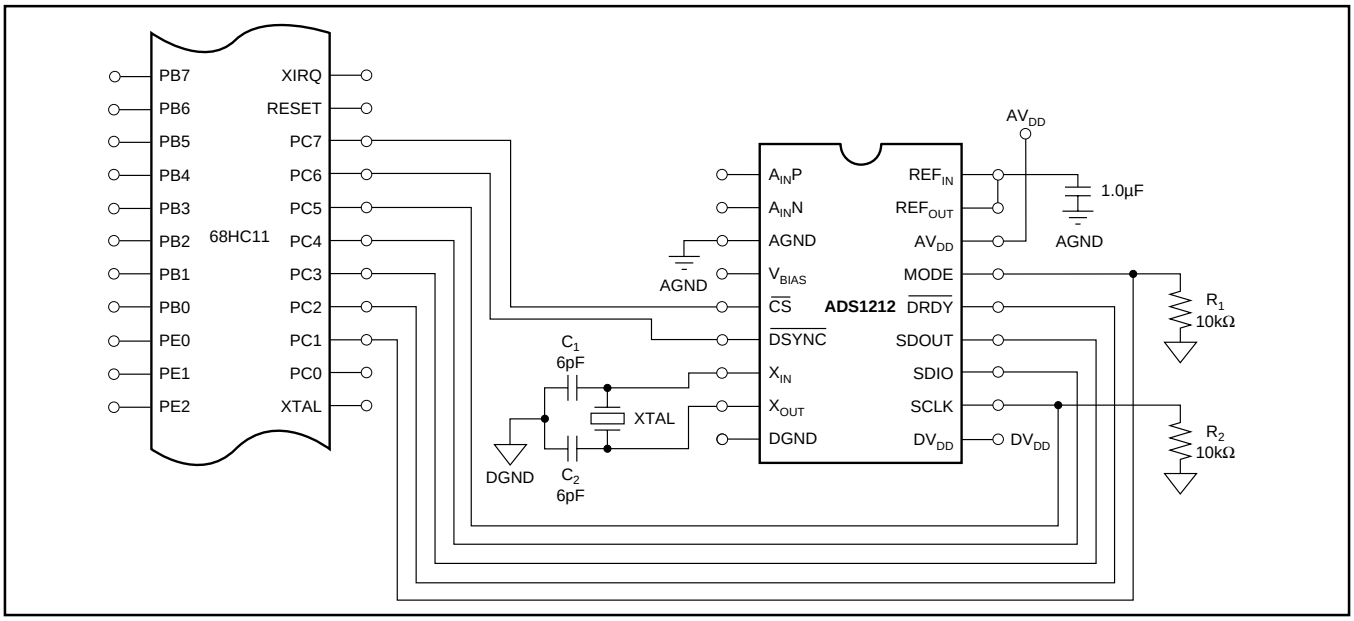


FIGURE 32. Full Interface with a 68HC11 Microprocessor.

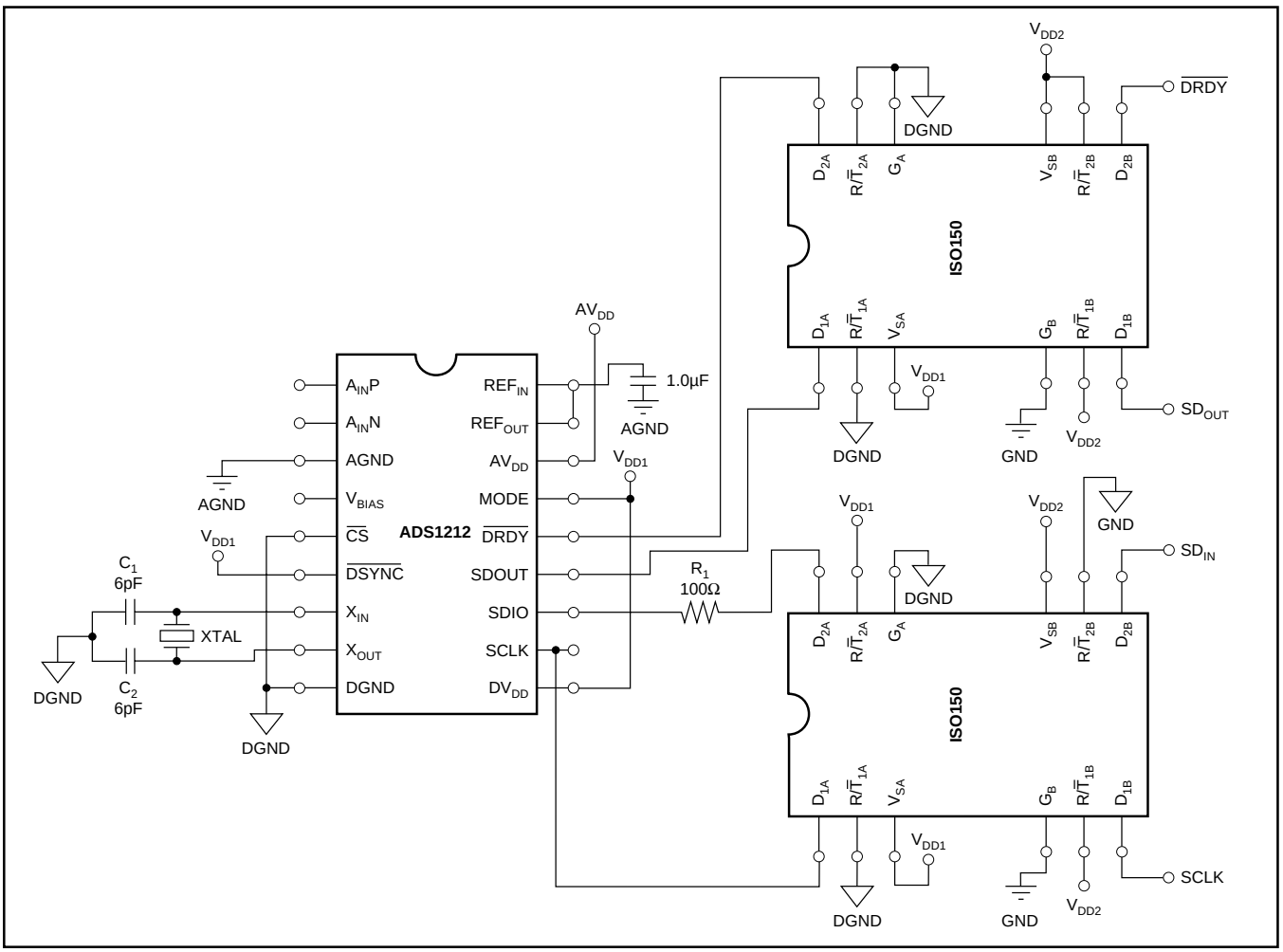


FIGURE 33. Isolated Four-Wire Interface.

Isolation

The serial interface of the ADS1212/13 provides for simple isolation methods. An example of an isolated four-wire interface is shown in Figure 33. The ISO150 is used to transmit the digital signals over the isolation barrier.

In addition, the digital outputs of the ADS1212/13 can, in some cases, drive opto-isolators directly. Figures 34 and 35 show the voltage of the SDOUT pin versus source or sink current under worst-case conditions. Worst-case conditions for source current occur when the analog input differential

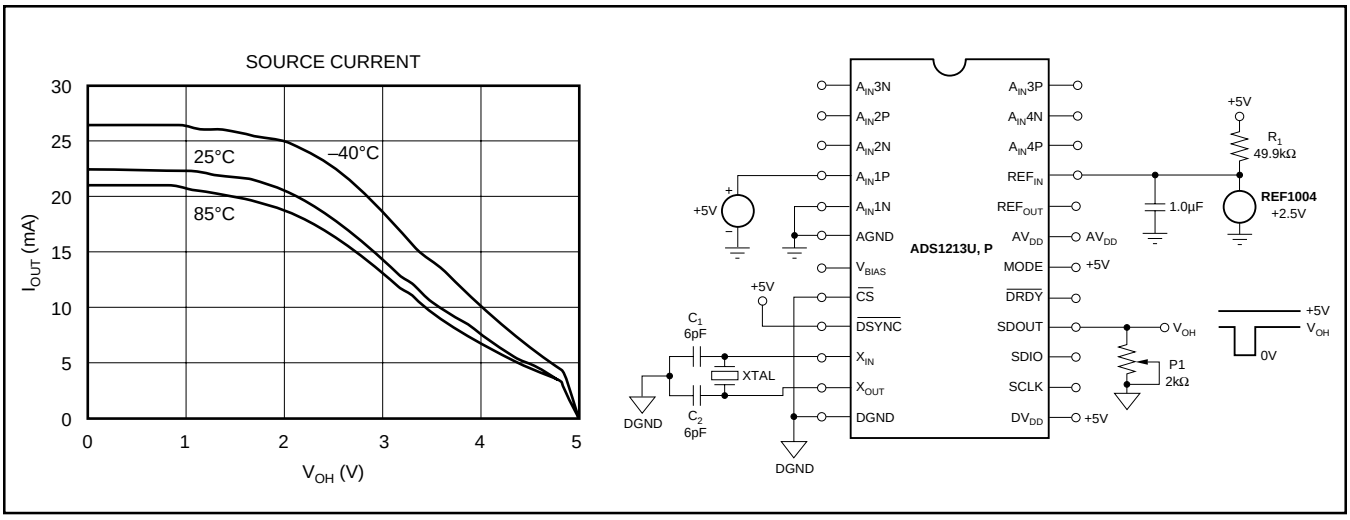


FIGURE 34. Source Current vs V_{OH} for SDOUT Under Worst-Case Conditions.

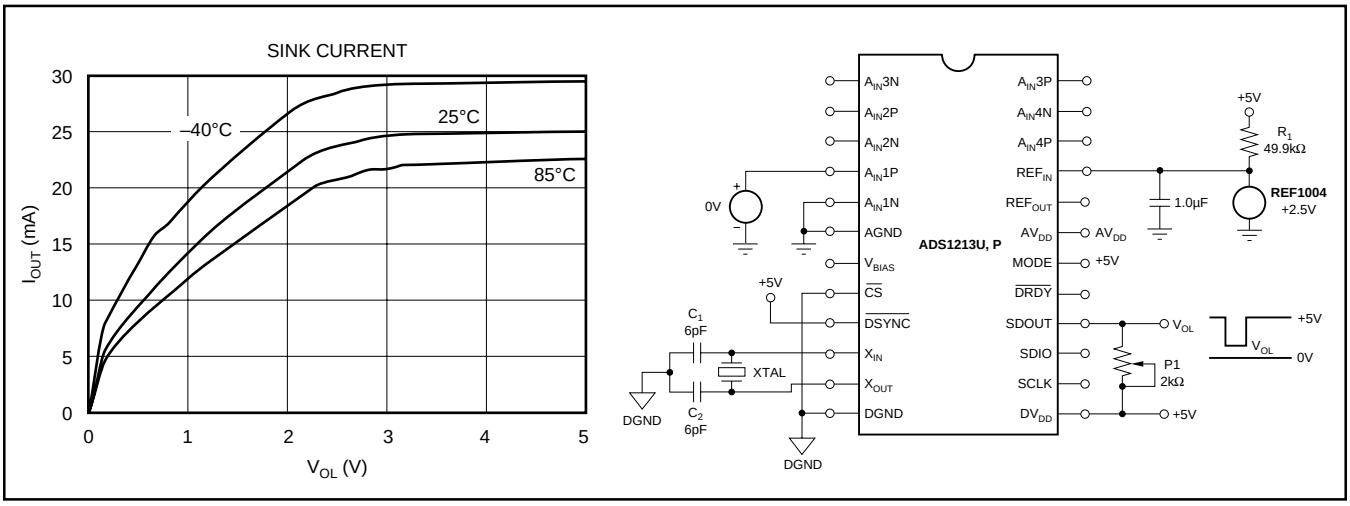


FIGURE 35. Sink Current vs V_{OL} for SDOUT Under Worst-Case Conditions.

voltage is 5V and the output format is Offset Binary ($FFFFFF_H$). For sink current, the worst-case condition occurs when the analog input differential voltage is 0V and the output format is Two's Complement (000000_H).

Note that SDOUT is tri-stated for the majority of the conversion period and the opto-isolator connection must take this into account.

Synchronization of Multiple Converters

The $\overline{DSYNC}$ input is used to synchronize the output data of multiple ADS1212/13s. Synchronization involves configuring each ADS1212/13 to the same Decimation Ratio and Turbo Mode setting, and providing a common signal to the X_{IN} inputs. Then, the $\overline{DSYNC}$ signal is pulsed LOW (see Figure 22 in the Timing section). This results in an internal reset of the modulator count for the current conversion. Thus, all the converters start counting from zero at the same time, producing a $\overline{DRDY}$ LOW signal at approximately the same point (see Figure 36).

Note that an asynchronous $\overline{DSYNC}$ input may cause multiple converters to be different from one another by one X_{IN} clock cycle. This should not be a concern for most applications. However, the Timing section contains information on exactly synchronizing multiple converters to the same X_{IN} clock cycle.

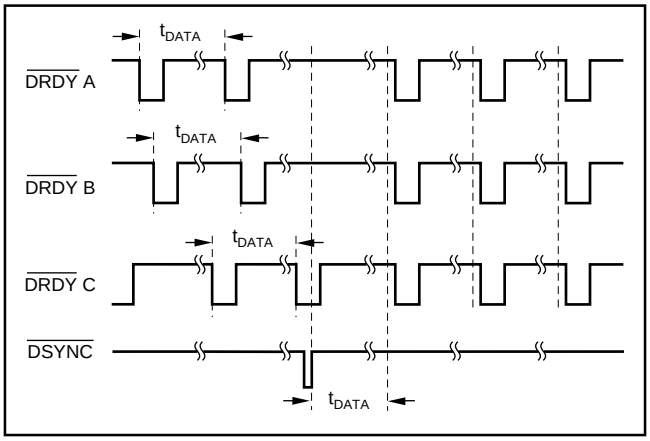


FIGURE 36. Effect of Synchronization on Output Data Timing.

LAYOUT

POWER SUPPLIES

The ADS1212/13 requires the digital supply (DV_{DD}) to be no greater than the analog supply (AV_{DD}) +0.3V. In the majority of systems, this means that the analog supply must come up first, followed by the digital supply. Failure to observe this condition could cause permanent damage to the ADS1212/13.

Inputs to the ADS1212/13, such as SDIO, A_{IN}, or REF_{IN}, should not be present before the analog and digital supplies are on. Violating this condition could cause latch-up. If these signals are present before the supplies are on, series resistors should be used to limit the input current (see the Analog Input and V_{BIAS} sections of this data sheet for more details concerning these inputs).

The best scheme is to power the analog section of the design and AV_{DD} of the ADS1212/13 from one +5V supply and the digital section (and DV_{DD}) from a separate +5V supply. The analog supply should come up first. This will ensure that A_{IN} and REF_{IN} do not exceed AV_{DD} and that the digital inputs are present only after AV_{DD} has been established, and that they do not exceed DV_{DD}.

The requirements for the digital supply are not as strict. However, high frequency noise on DV_{DD} can capacitively couple into the analog portion of the ADS1212/13. This noise can originate from switching power supplies, very fast microprocessors or digital signal processors.

For either supply, high frequency noise will generally be rejected by the digital filter except at interger multiplies of f_{MOD}. Just below and above these frequencies, noise will alias back into the passband of the digital filter, affecting the conversion result.

If one supply must be used to power the ADS1212/13, the AV_{DD} supply should be used to power DV_{DD}. This connection can be made via a 10Ω resistor which, along with the decoupling capacitors, will provide some filtering between DV_{DD} and AV_{DD}. In some systems, a direct connection can be made. Experimentation may be the best way to determine the approprate connection between AV_{DD} and DV_{DD}.

GROUNDING

The analog and digital sections of the design should be carefully and cleanly partitioned. Each section should have its own ground plane with no overlap between them. AGND should be connected to the analog ground plane as well as all other analog grounds. DGND should be connected to the digital ground plane and all digital signals referenced to this plane.

For a single converter system, AGND and DGND of the ADS1212/13 should be connected together, underneath the converter. Do not join the ground planes, but connect the two with a moderate signal trace. For multiple converters, connect the two ground planes at one location as central to all of the converters as possible. In some cases, experimentation may be required to find the best point to connect the two planes together. The printed circuit board can be designed to provide different analog/digital ground connections via short jumpers. The initial prototype can be used to establish which connection works best.

DECOUPLING

Good decoupling practices should be used for the ADS1212/13 and for all components in the design. All decoupling capacitors, but specifically the 0.1µF ceramic capacitors, should be placed as close as possible to the pin being decoupled. A 1µF to 10µF capacitor, in series with a 0.1µF ceramic capacitor, should be used to decouple AV_{DD} to AGND. At a minimum, a 0.1µF ceramic capacitor should be used to decouple DV_{DD} to DGND, as well as for the digital supply on each digital component.

SYSTEM CONSIDERATIONS

The recommendations for power supplies and grounding will change depending on the requirements and specific design of the overall system. Achieving 20 bits or more of effective resolution is a great deal more difficult than achieving 12 bits. In general, a system can be broken up into four different stages:

Analog Processing

Analog Portion of the ADS1212/13

Digital Portion of the ADS1212/13

Digital Processing

For the simplest system consisting of minimal analog signal processing (basic filtering and gain), a self-contained microcontroller, and one clock source, high-resolution could be achieved by powering all components by a common power supply. In addition, all components could share a common ground plane. Thus, there would be no distinctions between “analog” and “digital” power and ground. The layout should still include a power plane, a ground plane, and careful decoupling.

In a more extreme case, the design could include: multiple ADS1212/13s; extensive analog signal processing; one or more microcontrollers, digital signal processors, or microprocessors; many different clock sources; and interconnections to various other systems. High resolution will be very difficult to achieve for this design. The approach would be to break the system into a many different parts as possible. For example, each ADS1212/13 may have its own analog processing front end, its own “analog” power and ground (possibly shared with the analog front end), and its own “digital” power and ground. The converter’s “digital” power and ground would be separate from the power and ground for the system’s processors, RAM, ROM, and “glue” logic.

APPLICATIONS

The ADS1212/13 can be used in a broad range of data acquisition tasks. The following application diagrams show the ADS1212 and/or ADS1213 being used for bridge transducer measurements, temperature measurement, and 4-20mA receiver applications.

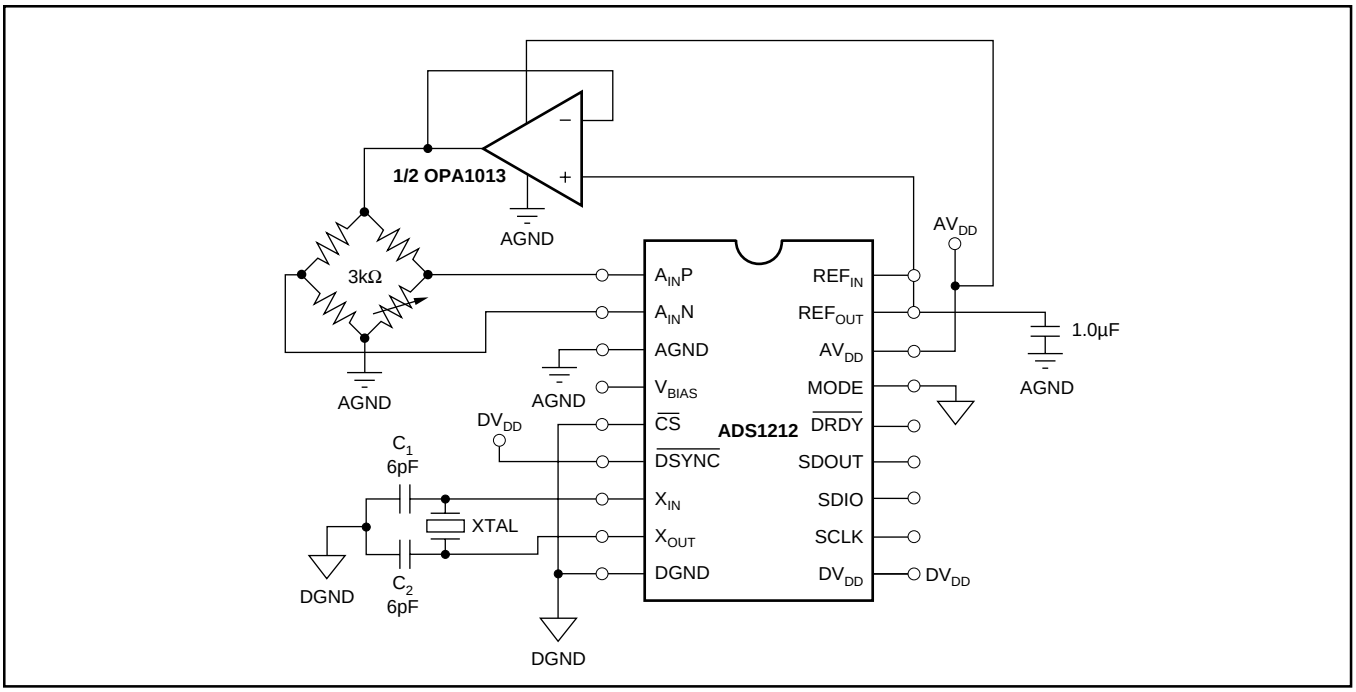


FIGURE 37. Bridge Transducer Interface with Voltage Excitation.

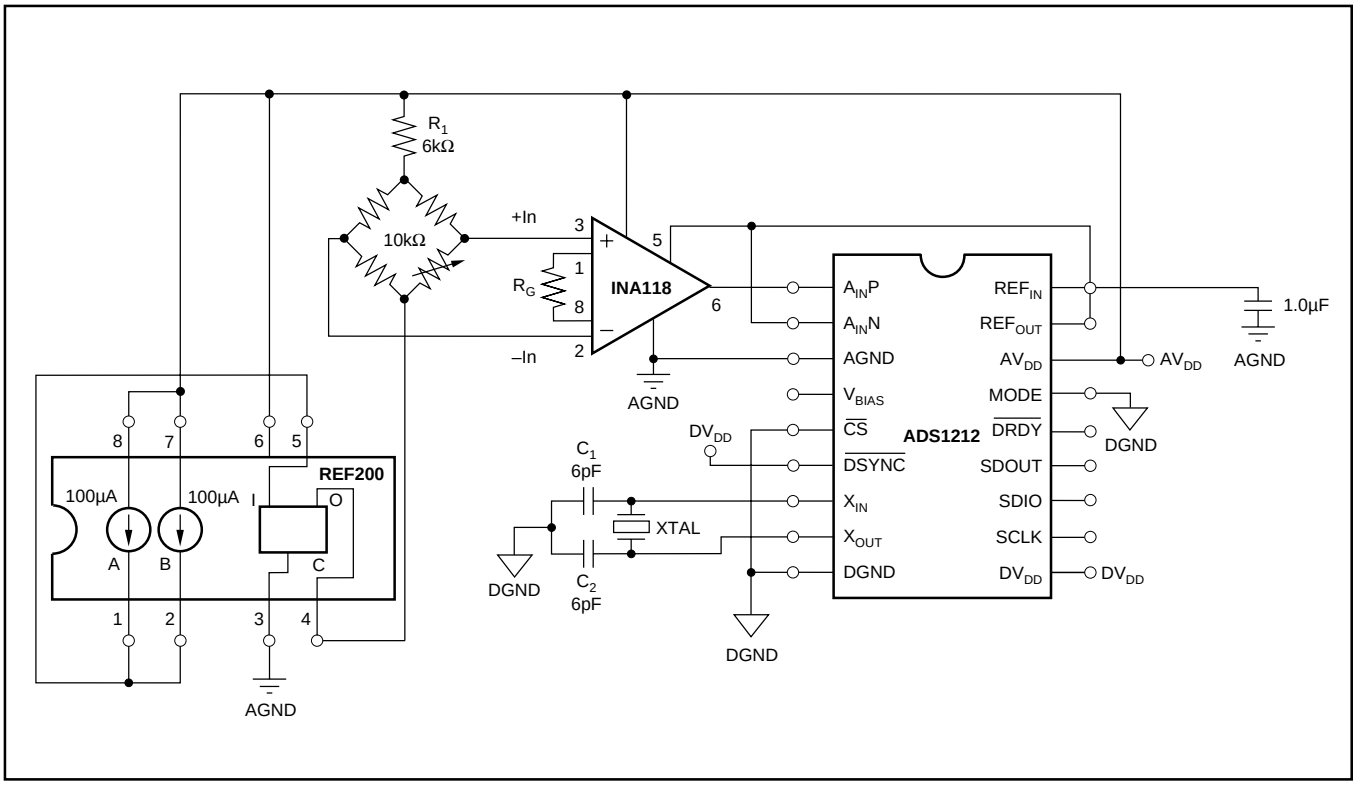


FIGURE 38. Bridge Transducer Interface with Current Excitation.

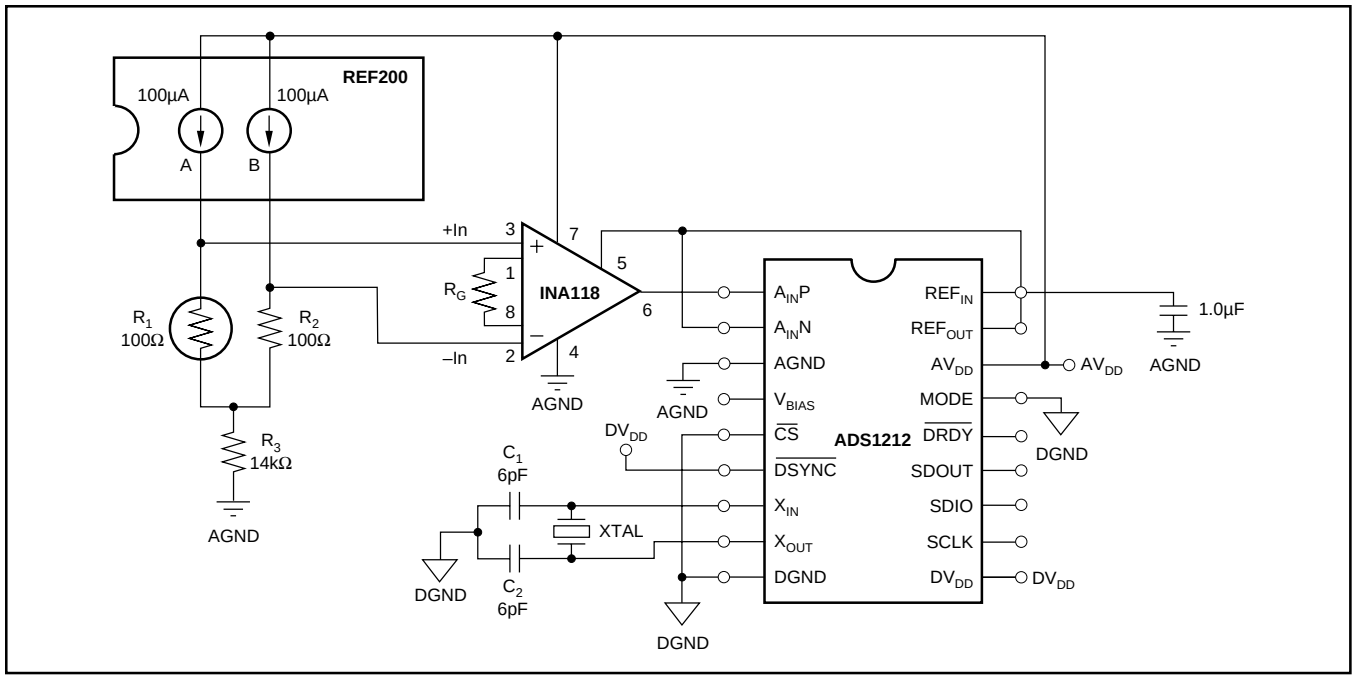


FIGURE 39. PT100 Interface.

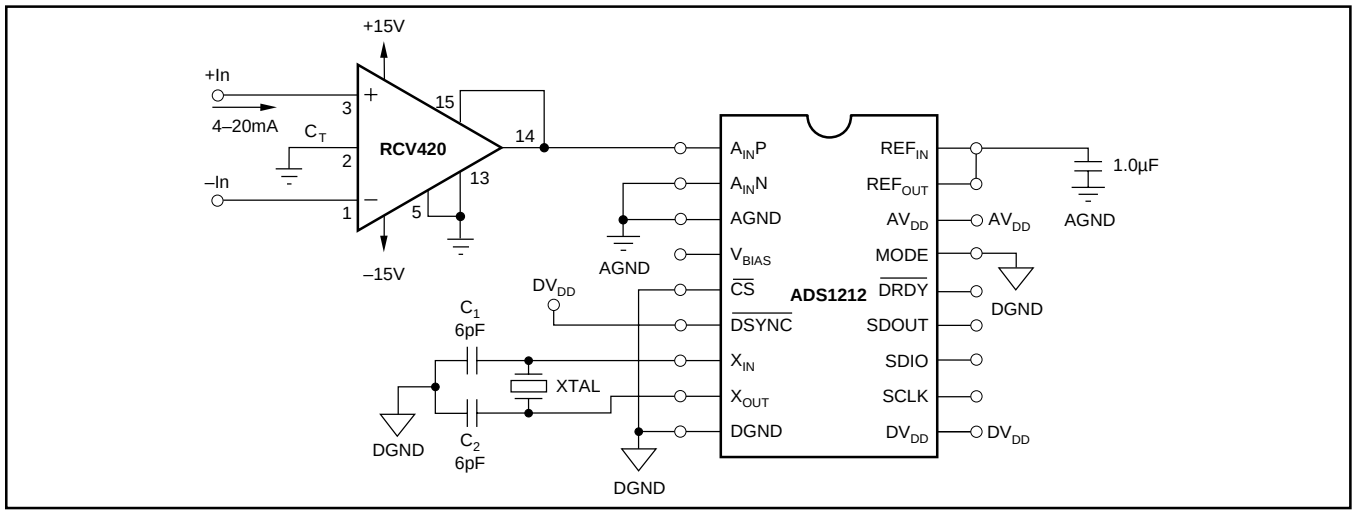


FIGURE 40. Complete 4-20mA Receiver.

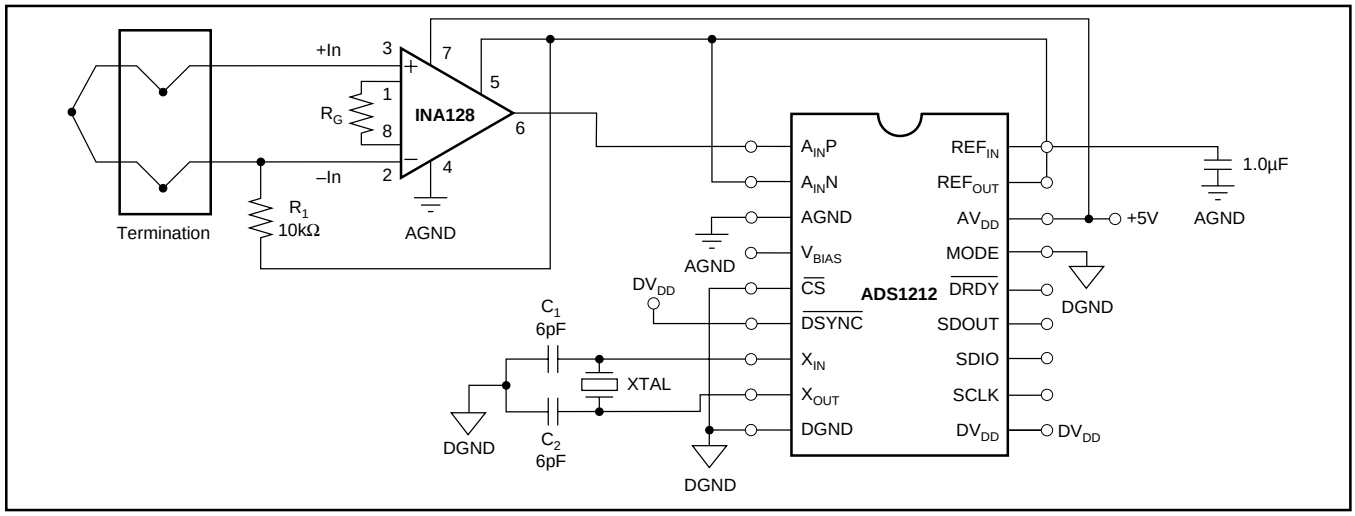


FIGURE 41. Single Supply, High-Accuracy Thermocouple.

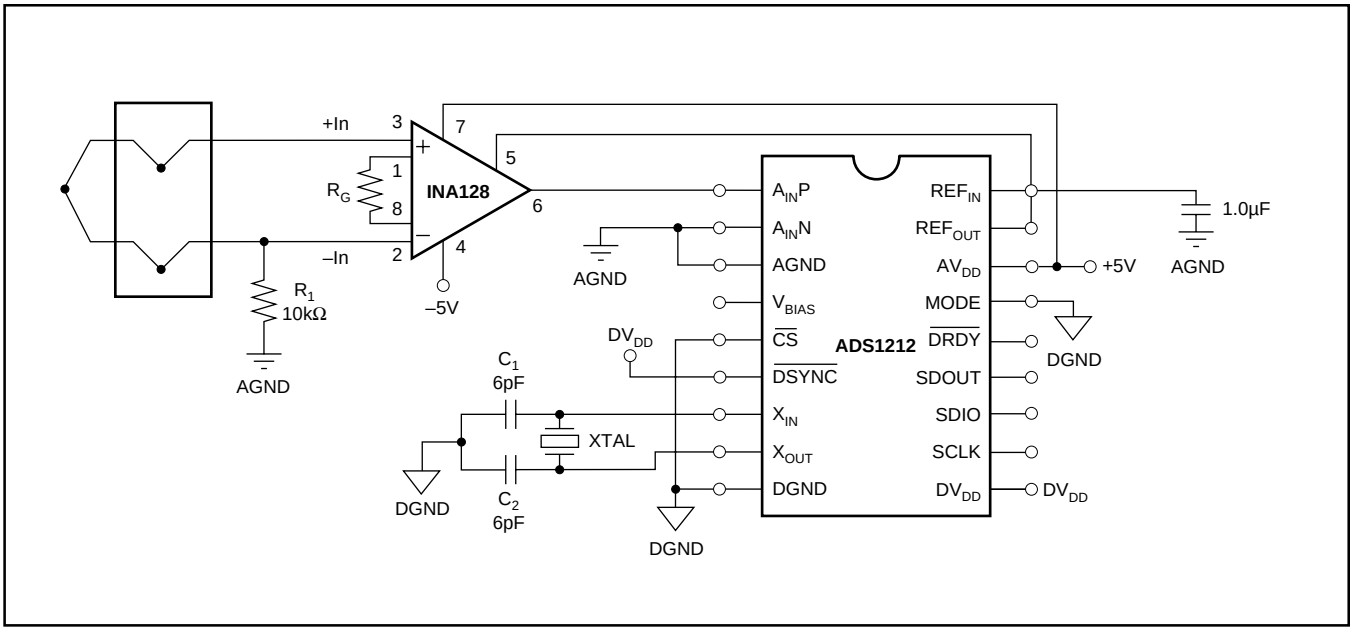


FIGURE 42. Dual Supply, High-Accuracy Thermocouple.

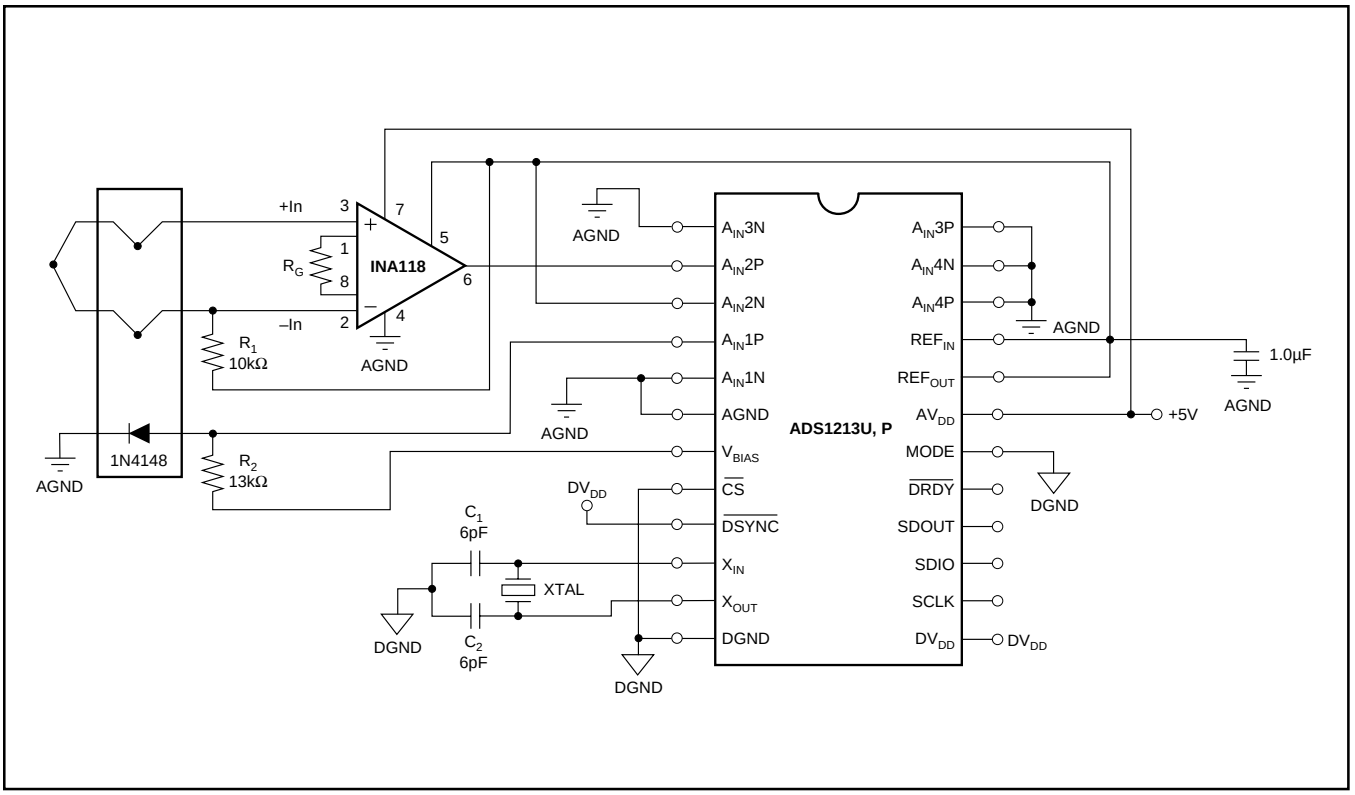


FIGURE 43. Single Supply, High-Accuracy Thermocouple Interface with Cold Junction Compensation.

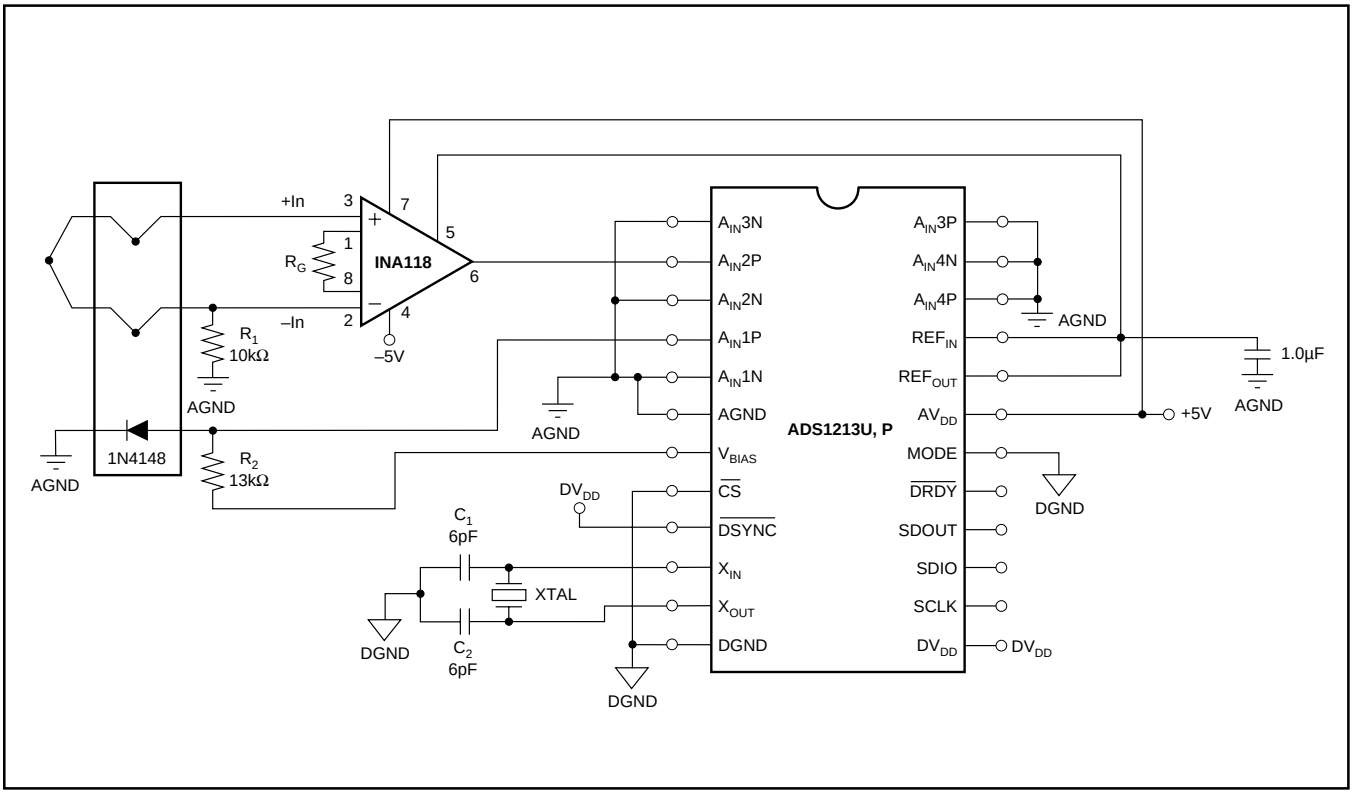


FIGURE 44. Dual Supply, High-Accuracy Thermocouple Interface with Cold Junction Compensation.

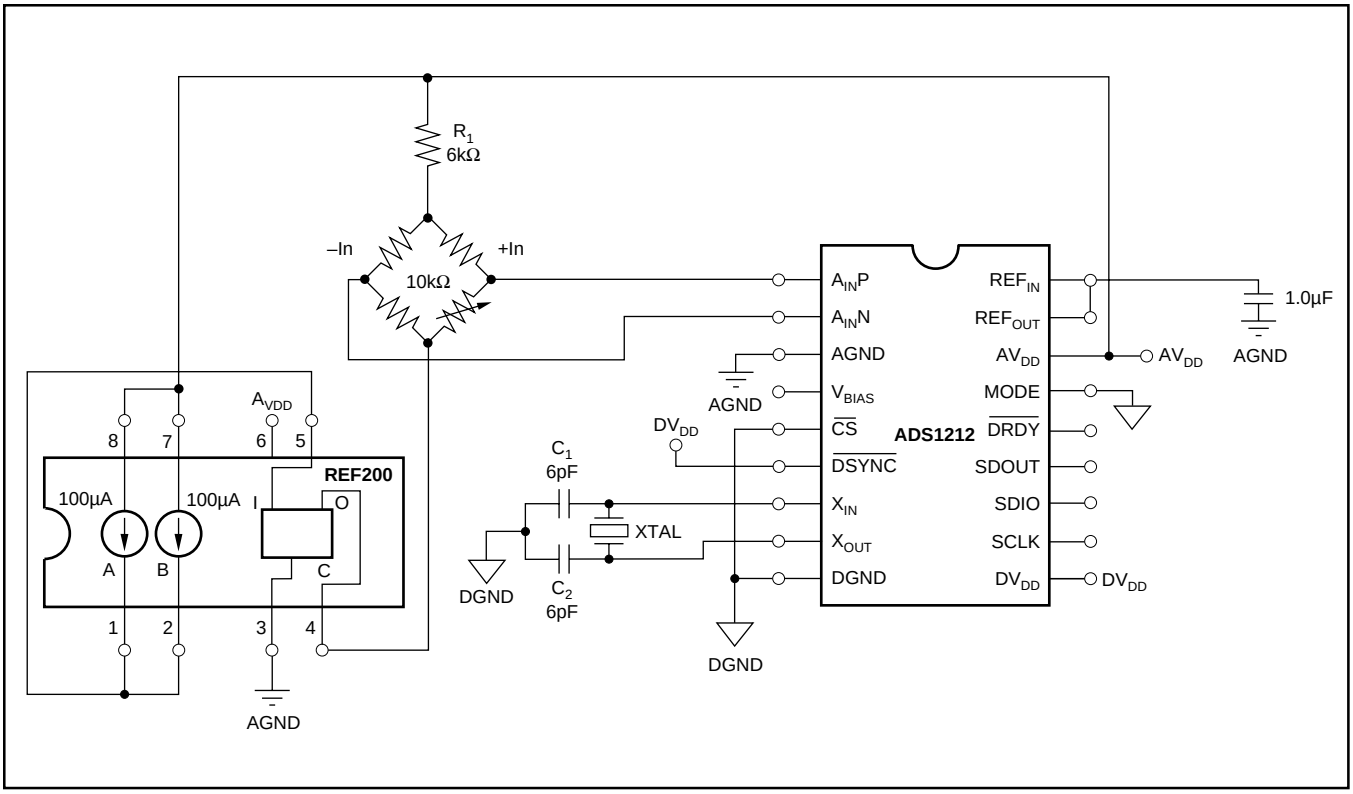


FIGURE 45. Low-Cost Bridge Transducer Interface with Current Excitation.

TOPIC INDEX

FIGURE INDEX

TABLE INDEX

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ADS1212P	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	Call TI	N / A for Pkg Type
ADS1212PG4	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	Call TI	N / A for Pkg Type
ADS1212U	ACTIVE	SOP	DTC	18	43	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS1212U/1K	ACTIVE	SOP	DTC	18	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS1212U/1KG4	ACTIVE	SOP	DTC	18	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS1212UG4	ACTIVE	SOP	DTC	18	43	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS1213E	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ADS1213E/1K	ACTIVE	SSOP	DB	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ADS1213E/1KG4	ACTIVE	SSOP	DB	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ADS1213EG4	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ADS1213P	ACTIVE	PDIP	NT	24	15	Green (RoHS & no Sb/Br)	Cu NiPdAu	N / A for Pkg Type
ADS1213PG4	ACTIVE	PDIP	NT	24	15	Green (RoHS & no Sb/Br)	Cu NiPdAu	N / A for Pkg Type
ADS1213U	ACTIVE	SOIC	DW	24	33	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS1213U/1K	ACTIVE	SOIC	DW	24	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS1213U/1KG4	ACTIVE	SOIC	DW	24	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS1213UG4	ACTIVE	SOIC	DW	24	33	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

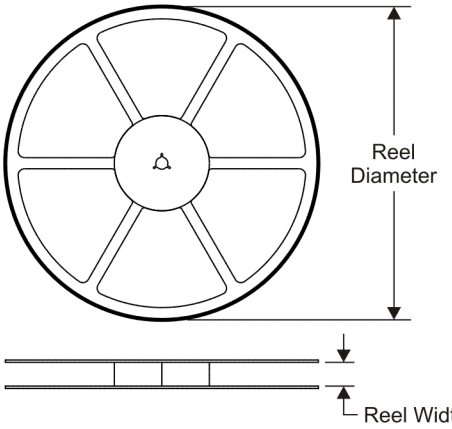
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

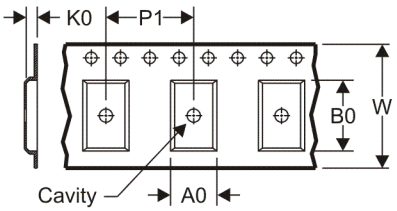
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

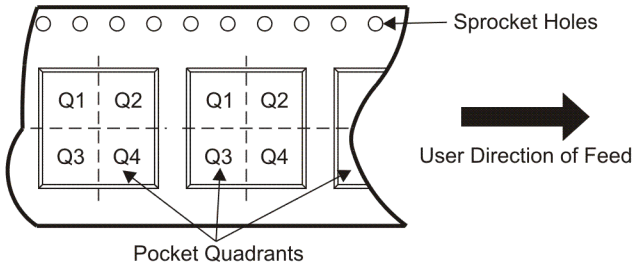


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

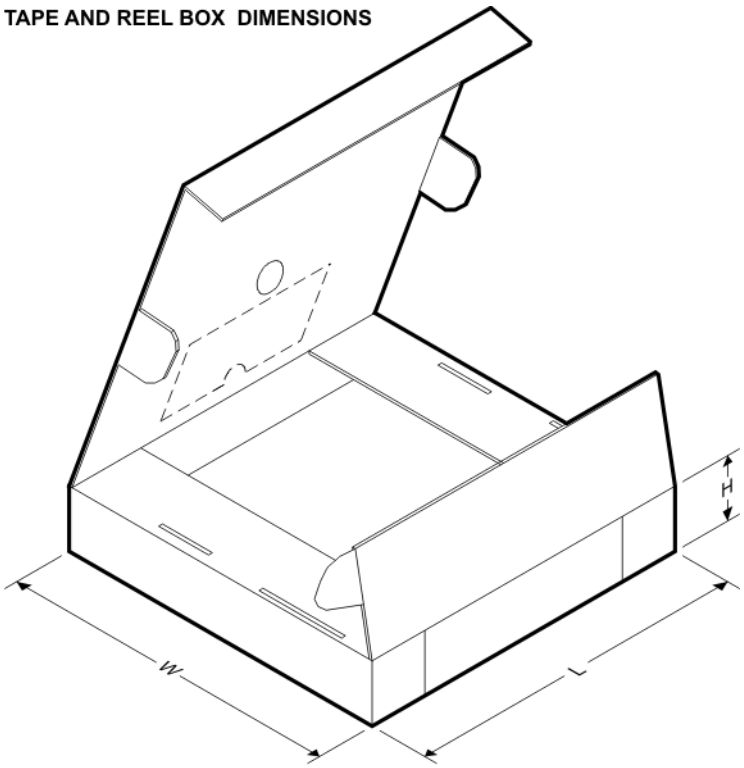
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1212U/1K	SOP	DTC	18	1000	330.0	24.4	10.9	12.0	2.7	12.0	24.0	Q1
ADS1213E/1K	SSOP	DB	28	1000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
ADS1213U/1K	SOIC	DW	24	1000	330.0	24.4	10.85	15.8	2.7	12.0	24.0	Q1

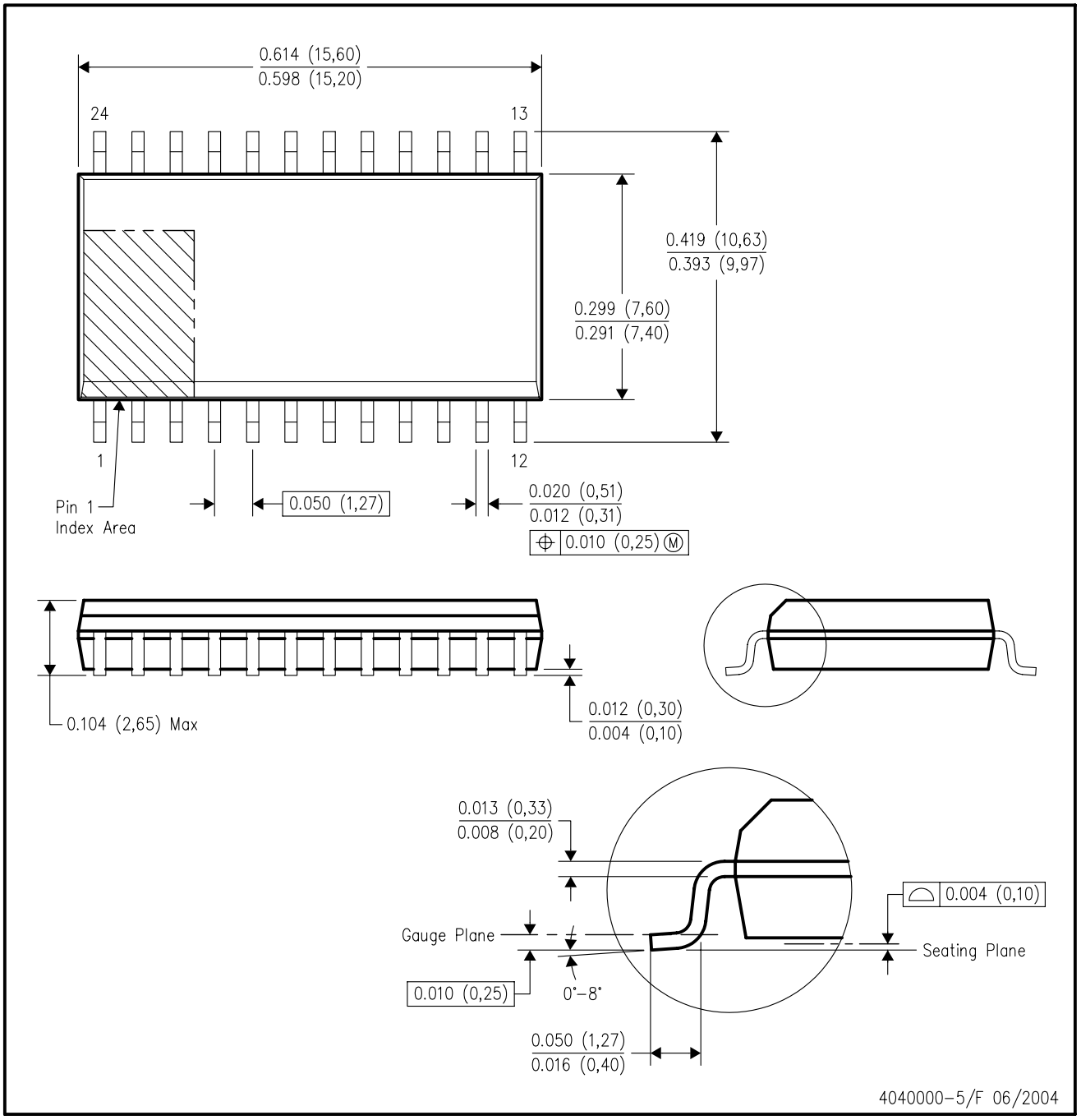
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1212U/1K	SOP	DTC	18	1000	346.0	346.0	41.0
ADS1213E/1K	SSOP	DB	28	1000	346.0	346.0	33.0
ADS1213U/1K	SOIC	DW	24	1000	346.0	346.0	41.0

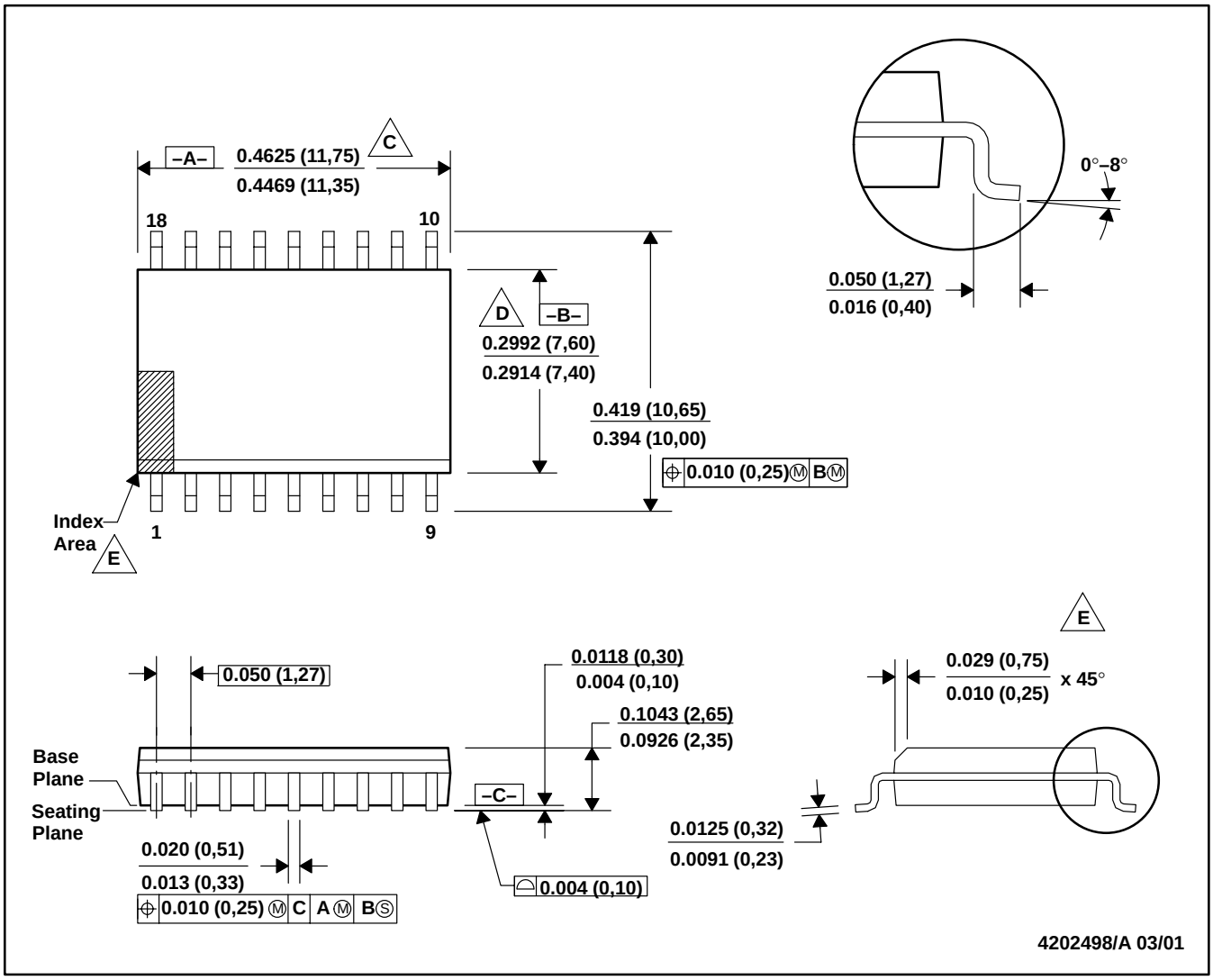
DW (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

MPDS095 – APRIL 2001

DTC (R-PDSO-G18) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs shall not exceed 0.006 (0,15) per side.
D. Body width dimension does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 0.010 (0,25) per side.
E. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
F. Falls within JEDEC MS-013-AB.

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