FEMTOCLOCKS™ CRYSTAL-TO-LVCMOS/LVTTL FREQUENCY SYNTHESIZER

ICS840001I-34

General Description

The ICS840001I-34 is a two output LVCMOS/LVTTL Synthesizer and a member of the HiPerClocks™ family of high performance devices from IDT. One output is the LVCMOS/LVTTL main synthesized clock output (Q) and one output is a three-state LVCMOS/LVTTL reference clock (REF_OUT) output at the frequency of the crystal oscillator. The device can accept crystals from 15.3125MHz to 42.67MHz and can synthesize outputs from 81.67MHz to 213.33MHz. The ICS840001I-34 is packaged in a 3mm x 3mm 16-pin VFQFN, making it ideal for use on space constrained boards.

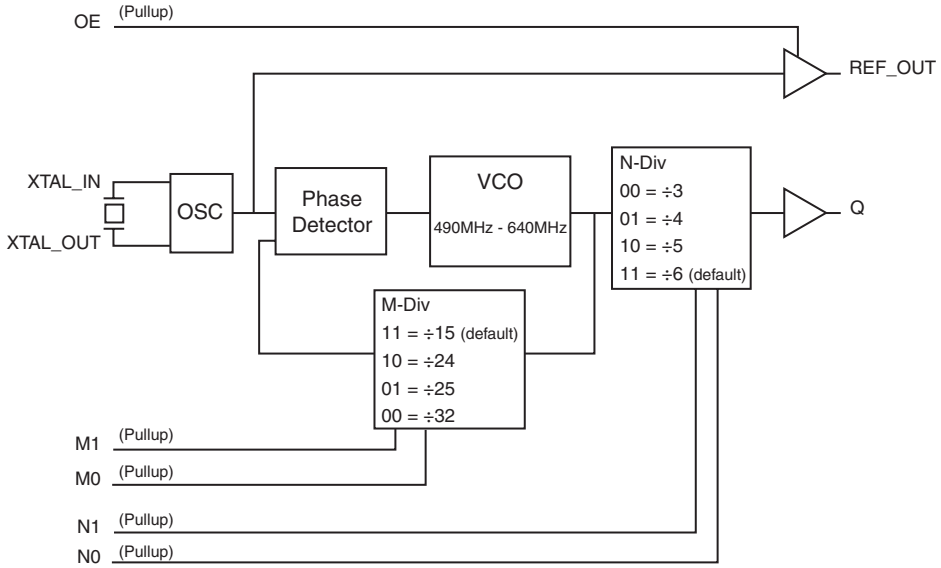
Features

- Two LVCMOS/LVTTL outputs, 22Ω typical output impedance
  One main clock output (Q)
  One three-state reference clock output (REF_OUT)
- Crystal oscillator interface can accept crystals from 15.3125MHz to 42.67MHz, 18pF parallel resonant crystal
- Q output frequency range: 81.67MHz to 213.33MHz
- RMS phase jitter @106.25, (637kHz – 10MHz): 0.38ps (typical)
- VCO range: 490MHz to 640MHz
- Full 3.3V and 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

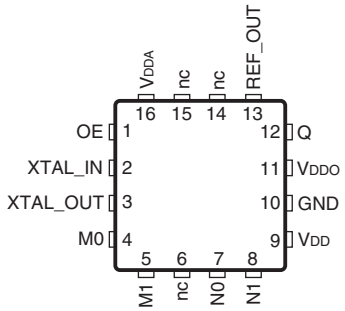
Common Application Configuration Table

Inputs				Output Frequency (MHz)	Application
Crystal (MHz)	M Divider	VCO (MHz)	N Divider		
40	15	600	6	100 (default)	Serial Attached (SCSI), PCI Express, Processor Clock
26.5625	24	637.5	6	106.25	Fibre Channel
40	15	600	4	150	Serial ATA (SATA), Processor Clock
26.5625	24	637.5	3	212.5	Fibre Channel 2
25	25	625	5	125	Ethernet
25	25	625	4	156.25	10 Gigabit Ethernet
22.5	25	562.5	3	187.5	12 Gigabit Ethernet
19.44	32	622.08	4	155.52	SONET

Block Diagram



Pin Assignment



ICS840001-34
16 Lead VFQFN
3mm x 3mm x 0.925 package body
K Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	OE	Input	Pullup	Output enable pin. When HIGH, REF_OUT output is enabled. When LOW, forces REF_OUT to Hi-Z state. See Table 3A. LVCMOS/LVTTL interface levels.
2, 3	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
4, 5	M0, M1	Input	Pullup	M divider inputs. LVCMOS/LVTTL interface levels. See Table 3B.
6, 14, 15	nc	Unused		No connect.
7, 8	No, N1	Input	Pullup	Determines output divider value as defined in Table 3C. LVCMOS/LVTTL interface levels.
9	V_{DD}	Power		Core supply pin.
10	GND	Power		Power supply ground.
11	V_{DDO}	Power		Output supply pin.
12	Q	Output		Single-ended clock output. 22Ω typical output impedance. LVCMOS/LVTTL interface levels.
13	REF_OUT	Output		Single-ended three-state reference clock output. 22Ω typical output impedance. LVCMOS/LVTTL interface levels.
16	V_{DDA}	Power		Analog supply pin.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance	V_{DD}, V_{DDO} = 3.465V		8		pF
		V_{DD}, V_{DDO} = 2.625V		6		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
R_{OUT}	Output Impedance	V_{DD}, V_{DDO} = 3.3V±5%	14	22	30	Ω
		V_{DD}, V_{DDO} = 2.5V±5%	16	26	36	Ω

Table 3A. Control Input Function Table

Control Input	Output
OE	REF_OUT
0	Hi-Z
1	Active (default)

Table 3B. M Divider Function Table

Control Inputs		
M1	M0	Feedback Divider Ratio
0	0	÷32
0	1	÷25
1	0	÷24
1	1	÷15 (default)

Table 3C. N Divider Function Table

Control Inputs		
N1	N0	Output Divider Ratio
0	0	÷3
0	1	÷4
1	0	÷5
1	1	÷6 (default)

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	76.1°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.12	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				100	mA
I_{DDA}	Analog Supply Current				12	mA
I_{DDO}	Output Supply Current				35	mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.12	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				90	mA
I_{DDA}	Analog Supply Current				12	mA
I_{DDO}	Output Supply Current				25	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		$V_{DD} = 3.3V$	2		$V_{DD} + 0.3$	V
			$V_{DD} = 2.5V$	1.7		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		$V_{DD} = 3.3V$	-0.3		0.8	V
			$V_{DD} = 2.5V$	-0.3		0.7	V
I_{IH}	Input High Current	OE, M0, M1, N0, N1	$V_{DD} = V_{IN} = 3.465V$ or 2.625V			5	µA
I_{IL}	Input Low Current	OE, M0, M1, N0, N1	$V_{DD} = V_{IN} = 3.465V$ or 2.625V	-150			µA
V_{OH}	Output High Voltage; NOTE 1		$V_{DDO} = 3.3V \pm 5\%$	2.6			V
			$V_{DDO} = 2.5V \pm 5\%$	1.8			V
V_{OL}	Output Low Voltage; NOTE 1		$V_{DDO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$			0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement Information, *Output Load Test Circuit diagrams.*

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		15.3125		42.67	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

AC Electrical Characteristics

Table 6A. AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40°C$ to $85°$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		81.67		213.33	MHz
$t_{jit}(Ø)$	RMS Phase Jitter, Random; NOTE 1	100MHz, Integration Range: 637kHz – 10MHz		0.54		ps
		106.25MHz, Integration Range: 637kHz – 10MHz		0.38		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle	Q, N = 3	40		60	%
		Q, N ≠ 3	48		52	%
		REF_OUT	48		52	%

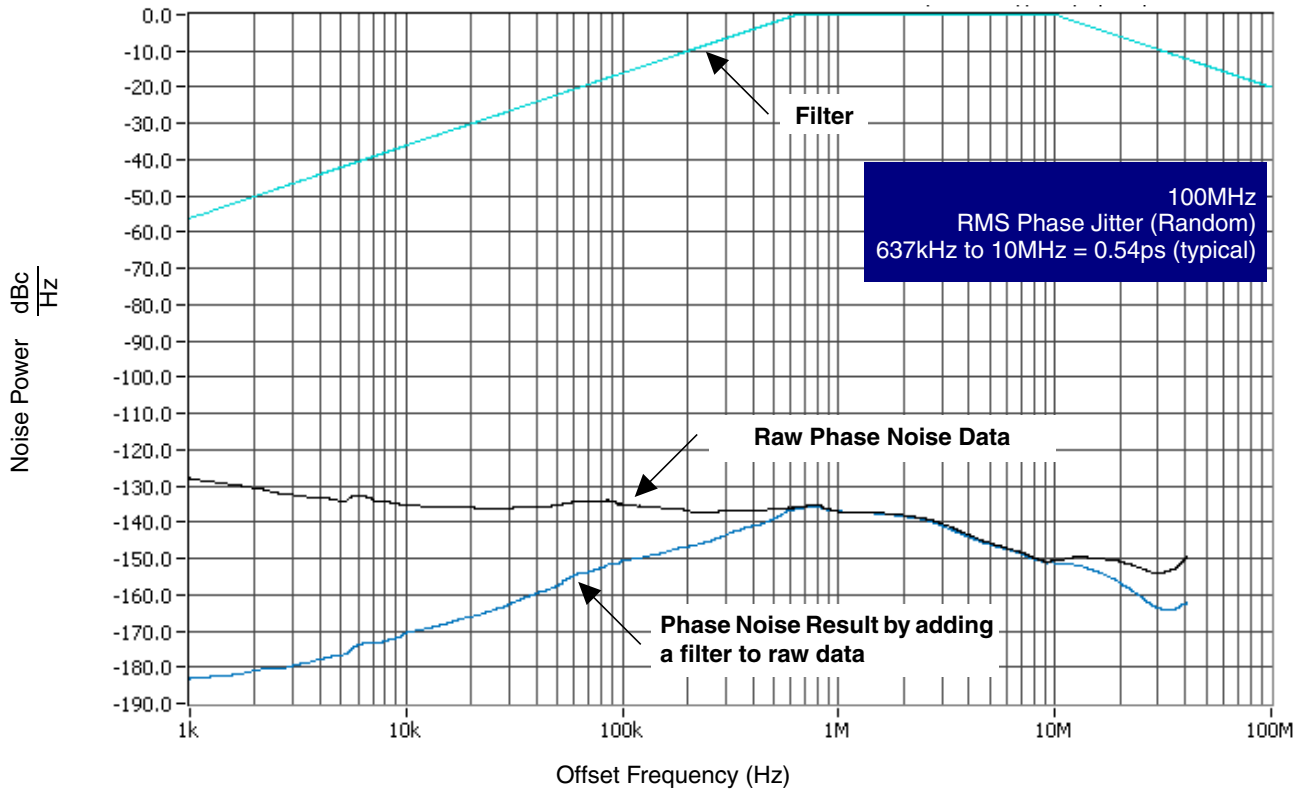
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. Device will meet specifications after thermal equilibrium has been reached under these conditions
NOTE 1: Please refer to Phase Noise Plot.

Table 6B. AC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C to 85°

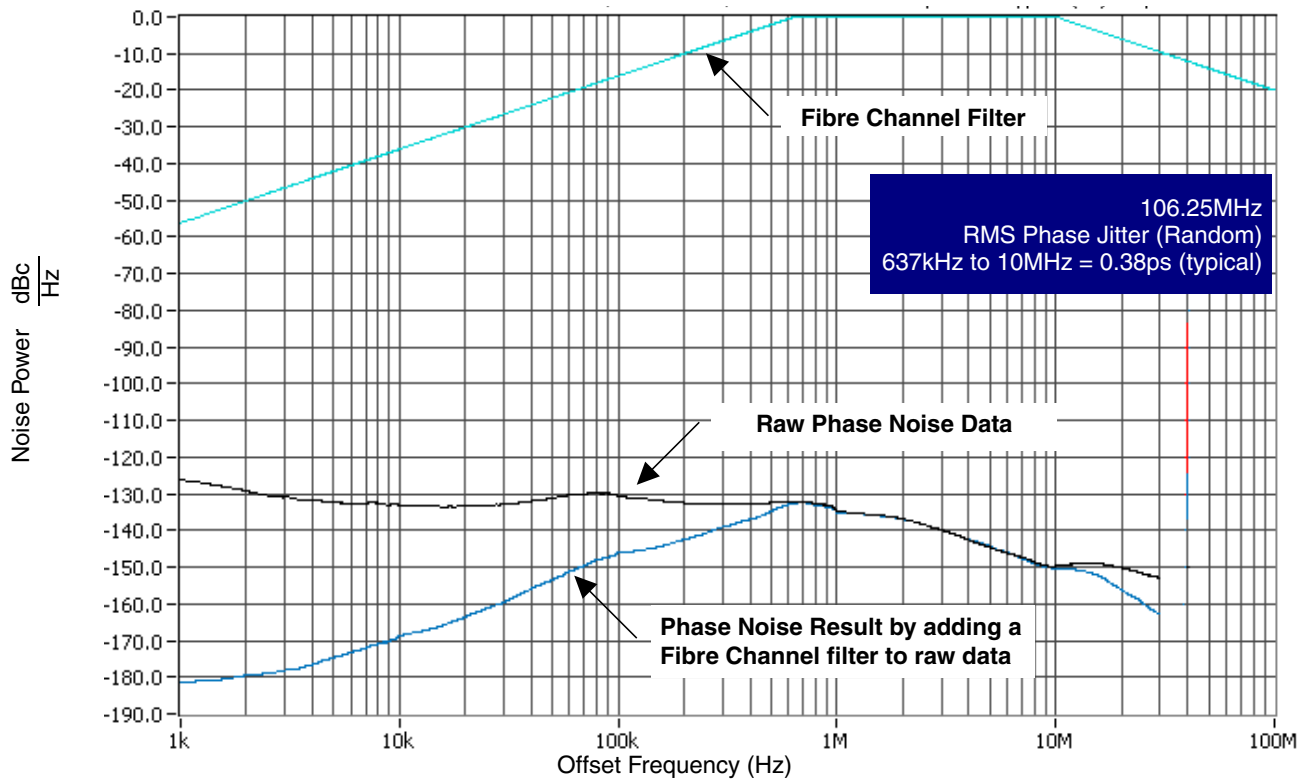
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		81.67		213.33	MHz
$t_{jit}(\emptyset)$	RMS Phase Jitter, Random; NOTE 1	100MHz, Integration Range: 637kHz – 10MHz		0.54		ps
		106.25MHz, Integration Range: 637kHz – 10MHz		0.38		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	300		800	ps
odc	Output Duty Cycle	Q, N = 3	35		65	%
		Q, N ≠ 3	40		60	%
		REF_OUT	45		55	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. Device will meet specifications after thermal equilibrium has been reached under these conditions
NOTE 1: Please refer to Phase Noise Plot.

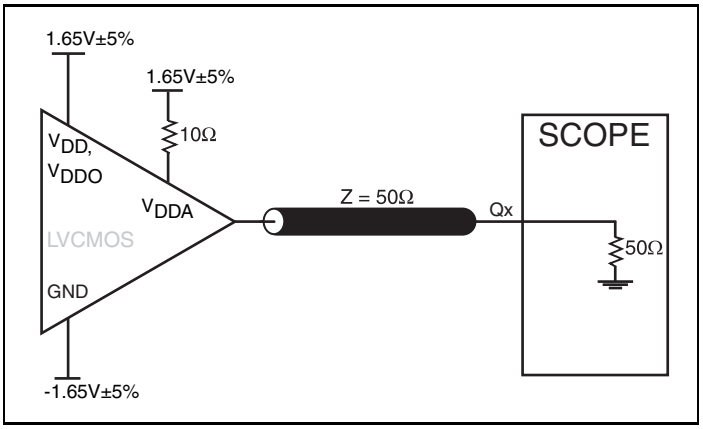
Typical Phase Noise at 100MHz (3.3V)



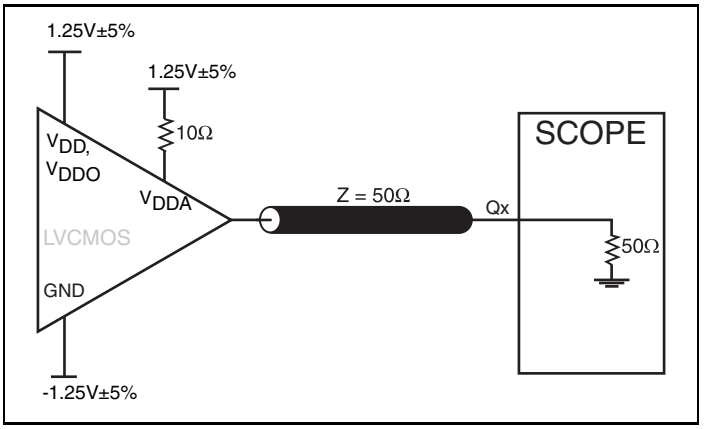
Typical Phase Noise at 106.25MHz (3.3V)



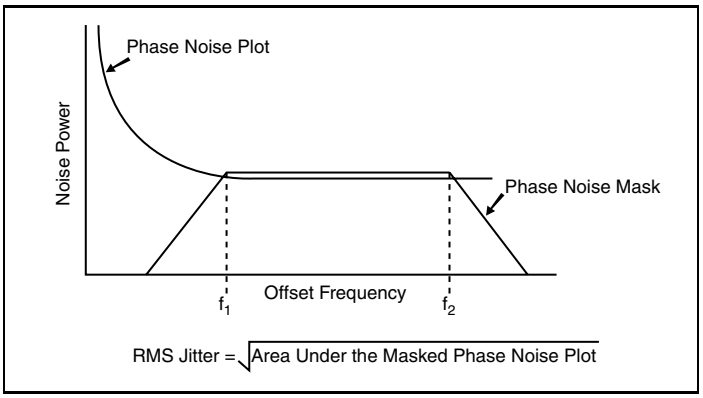
Parameter Measurement Information



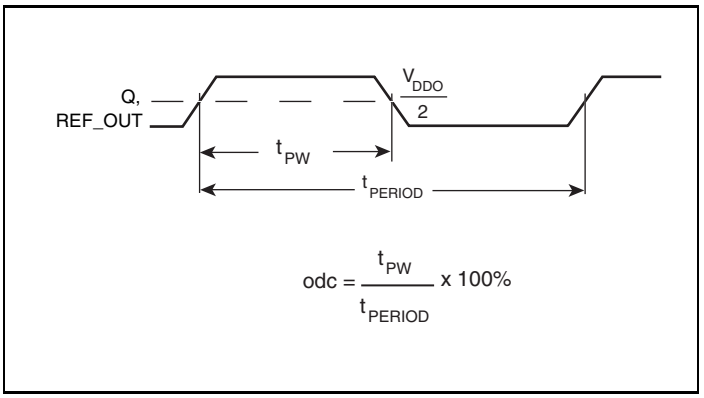
3.3V LVCMOS Output Load AC Test Circuit



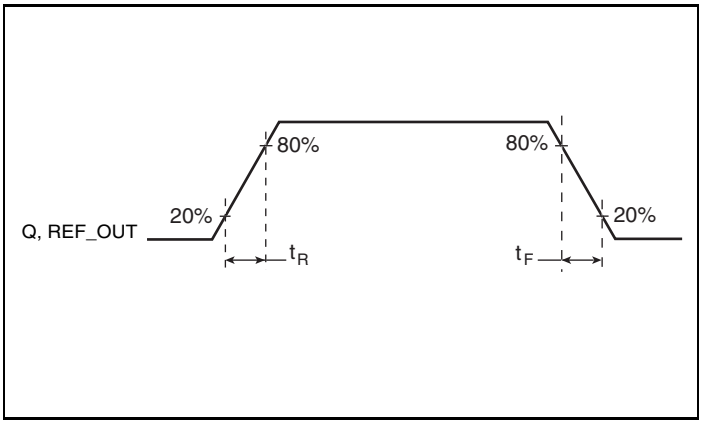
2.5V LVCMOS Output Load AC Test Circuit



RMS Phase Jitter



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Application Information

Power Supply Filtering Technique

To achieve optimum jitter performance, power supply isolation is required. The ICS40001I-34 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. $V_{DD,}$ $V_{DDA,}$ and V_{DDO} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

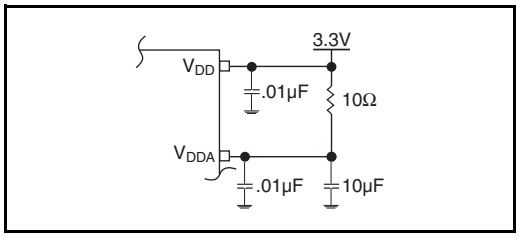


Figure 1. Power Supply Filtering

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Output

All unused LVCMOS output can be left floating. There should be no trace attached.

Crystal Input Interface

The ICS840001I-34 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 26.5625MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

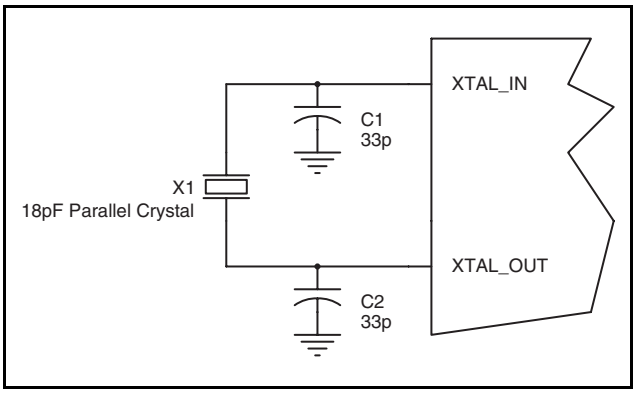


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

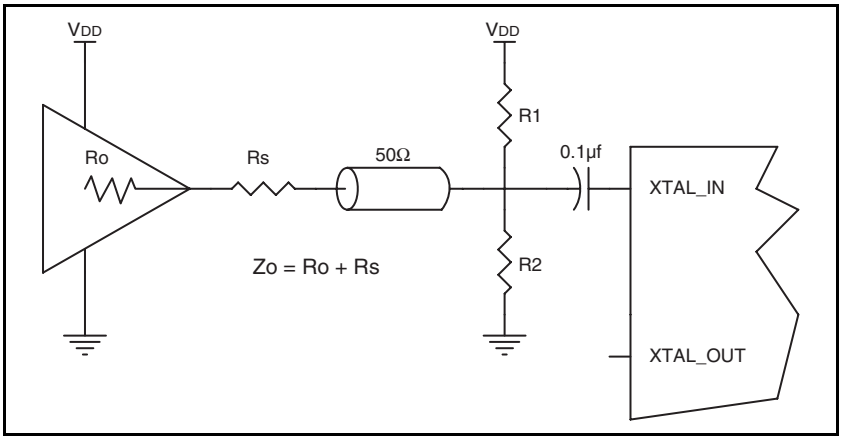


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

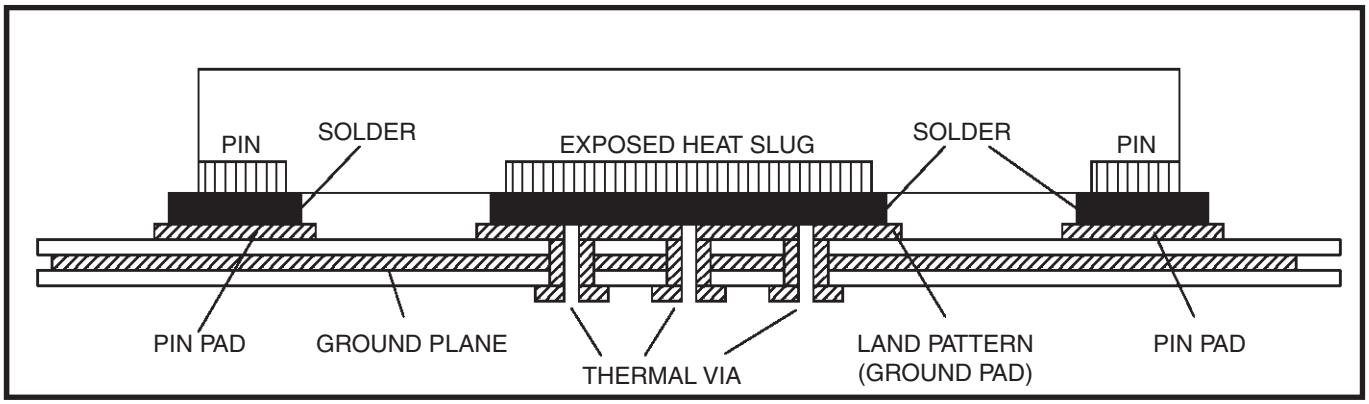


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 16 Lead VFQFN

θ_{JA} at 0 Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	76.1°C/W	66.5	59.7

Transistor Count

The transistor count for ICS840001I-34 is: 2805

Package Outline and Package Dimensions

Package Outline - K Suffix for 16 Lead VFQFN

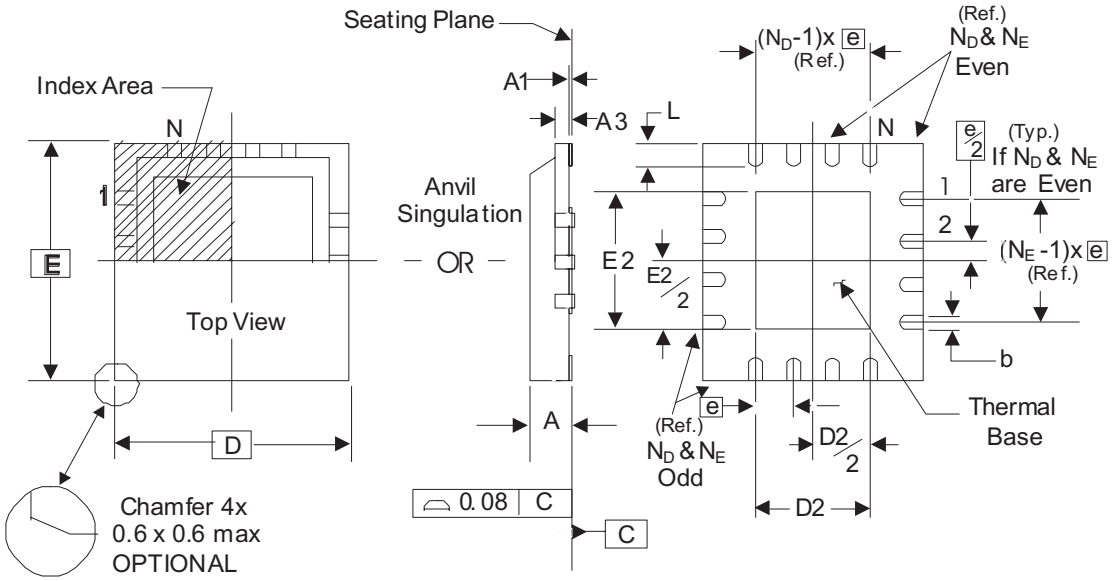


Table 8. Package Dimensions

JEDEC Variation: VEED-2/-4 All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	16	
A	0.80	1.00
A1	0	0.05
A3	0.25 Ref.	
b	0.18	0.30
N_D & N_E	4	
D & E	3.00 Basic	
D2 & E2	1.00	1.80
e	0.50 Basic	
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
840001AKI-34LF	AI4L	“Lead-Free” 16 Lead VFQFN	Tray	-40°C to 85°C
840001AKI-34LFT	AI4L	“Lead-Free” 16 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	 9	11 13 14	Updated VFQFN EPAD Thermal Release Path section. Updated Package Drawing. Ordering Information Table - corrected Temperature column.	10/27/08

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