CRYSTAL-TO-LVCMOS/LVTTL FREQUENCY SYNTHESIZER

ICS840S07I

General Description

The ICS840S07I is a seven output, Crystal or single ended-to-LVCMOS/LVTTL Frequency Synthesizer and a member of HiperClocks™ family of high performance clock solutions from IDT. The ICS840S07I uses a 25MHz parallel resonant crystal to generate 33.33MHz – 166.67MHz clock signals, replacing solutions requiring multiple oscillator and fanout buffer solution. The device supports output slew rate control with two slew select pins (SLEW[1:0]). The VCO operates at a frequency of 2GHz. The device has 3 output banks, Bank AA with one 33.33MHz – 166.67MHz LVCMOS/LVTTL output, Bank AB with one 125MHz LVCMOS/LVTTL output and Bank B with three 33.33MHz – 166.67MHz LVCMOS/LVTTL outputs.

Bank AA and Bank B have their own dedicated frequency select pins and can be independently set for the frequencies mentioned above. The low phase noise characteristic of the ICS840S07I makes it an ideal clock source for Gigabit Ethernet application. Designed for networking and industrial applications, the ICS840S07I can also drive the high-speed clock inputs of communication processors, DSPs, switches and bridges.

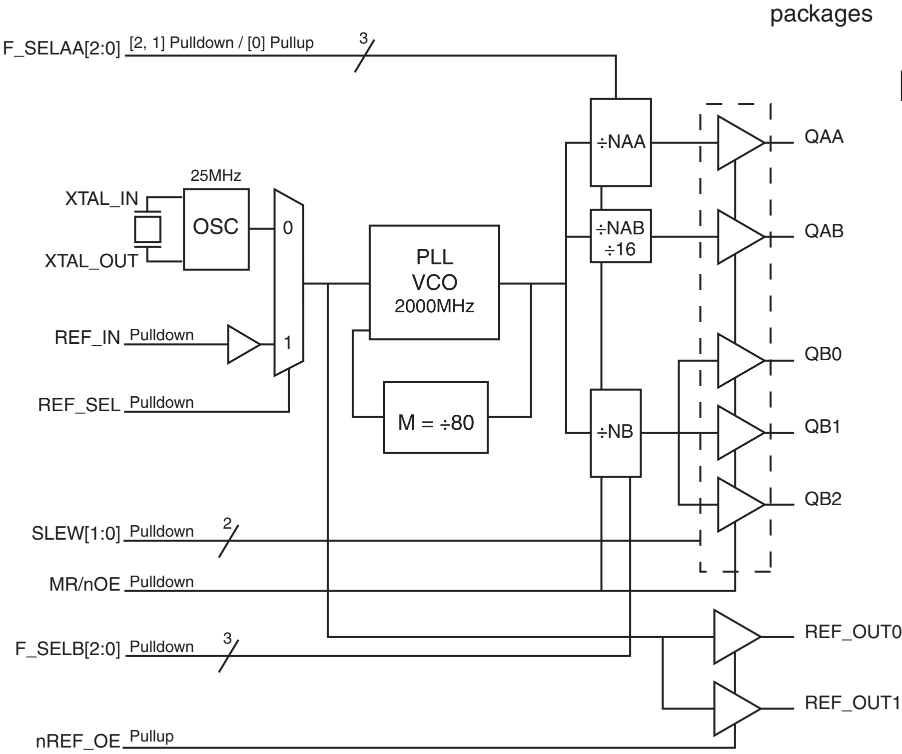
Features

- Five LVCMOS/LVTTL clock outputs, 15Ω typical output impedance

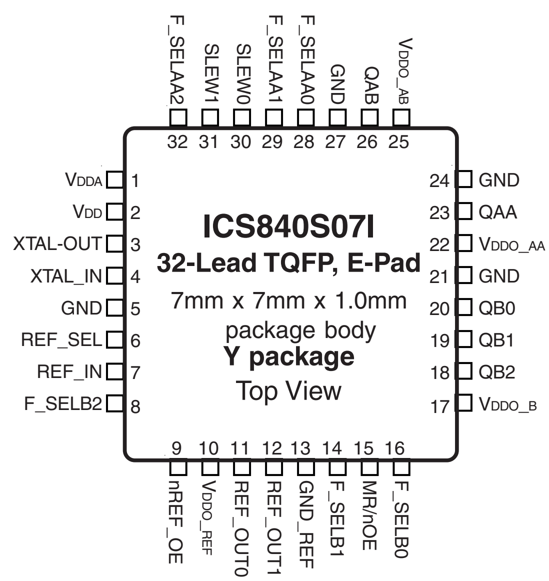
  Two REF_OUT LVCMOS/LVTTL clock outputs, 18Ω typical output impedance
- Selectable crystal oscillator interface, 25MHz, 18pF parallel resonant crystal or LVCMOS/LVTTL single-ended reference input
- Supports the following output frequencies:
  Bank AA/Bank B: 33.33MHz, 50MHz, 66.67MHz, 83.33, 100MHz, 125MHz, 133.33MHz and 166.67MHz

  Bank AB: 125MHz
- VCO: 2GHz
- Slew rate control
- RMS period jitter: TBD
- Output supply modes:
  Core/Output
  3.3V/3.3V
  3.3V/2.5V
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{DDA}	Power		Analog supply pin.
2	V_{DD}	Power		Core supply pins.
3, 4	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_OUT is the output. XTAL_IN is the input.
5, 21, 24, 27	GND	Power		Power supply ground.
6	REF_SEL	Input	Pulldown	Reference select pin. When HIGH selects REF_IN. When LOW, selects crystal. LVCMOS/LVTTL interface levels.
7	REF_IN	Input	Pulldown	Single-ended LVCMOS/LVTTL reference clock input.
8, 14, 16	F_SELB2, F_SELB1, F_SELB0	Input	Pulldown	Frequency select pins for Bank B outputs. See Table 3A. LVCMOS/LVTTL interface levels.
9	nREF_OE	Input	Pullup	Active low REF_OUT enable/disable pin. LVCMOS/LVTTL interface levels.
10	V_{DDO_REF}	Power		Output supply pin for REF_OUTx clock outputs. LVCMOS/LVTTL interface levels.
11, 12	REF_OUT0, REF_OUT1	Output		Single-ended LVCMOS/LVTTL reference clock outputs. 18Ω typical output impedance.
13	GND_REF	Power		Power supply ground for REF_OUTx clock outputs.
15	MR/nOE	Input	Pulldown	Active HIGH Master Reset. Active LOW output enable. When logic HIGH, the internal dividers are reset and the outputs are in high impedance (HI-Z). When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
17	V_{DDO_B}	Power		Output supply pin for QBx outputs.
18, 19, 20	QB2, QB1, QB0	Output		Single-ended Bank QBx clock outputs. LVCMOS/LVTTL interface levels. 15Ω typical output impedance.
22	V_{DDO_AA}	Power		Output supply pin for QAA output.
23	QAA	Output		Single-ended Bank QAA clock output. LVCMOS/LVTTL interface levels. 15Ω typical output impedance.
25	V_{DDO_AB}	Power		Output supply pin for Bank QAB output.
26	QAB	Output		Single-ended Bank QAB clock output. LVCMOS/LVTTL interface levels. 15Ω typical output impedance.
28	F_SELAA0	Input	Pullup	Frequency select pin for Bank QAA output. See Table 3A. LVCMOS/LVTTL interface levels.
29, 32	F_SELAA1, F_SELAA2	Input	Pulldown	Frequency select pins for Bank QAA output. See Table 3A. LVCMOS/LVTTL interface levels.
30, 31	SLEW0, SLEW1	Input	Pulldown	Slew rate select pins for LVCMOS/LVTTL clock output. See Table 3B. LVCMOS/LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance	Slew Rate = 2.75V/ns V_{DD}, V_{DDO_REF}, V_{DDO_AA}, V_{DDO_AB}, V_{DDO_B} = 3.465V		TBD		pF
		Slew Rate = 1ns V_{DD}, V_{DDO_REF}, V_{DDO_AA}, V_{DDO_AB}, V_{DDO_B} = 3.465V		TBD		pF
		Slew Rate = 2.75V/ns V_{DD} = 3.465V, V_{DDO_REF}, V_{DDO_AA}, V_{DDO_AB}, V_{DDO_B} = 2.625V		TBD		pF
		Slew Rate = 1ns V_{DD} = 3.465V, V_{DDO_REF}, V_{DDO_AA}, V_{DDO_AB}, V_{DDO_B} = 2.625V		TBD		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance	QAA, QAB, QB[0:2]		15		Ω
		REF_OUT[0:1]		18		Ω

TABLE 3A. BANK QAA FREQUENCY SELECT FUNCTION TABLE

Inputs					Output Frequency (25MHz Reference)
F_SELAA2	F_SELAA1	F_SELAA0	M Divider Value	NAA Divider Value	QAA (MHz)
L	L	L	80	60	33.33
L	L	H	80	40	50
L	H	L	80	30	66.67
L	H	H	80	24	83.33
H	L	L	80	20	100
H	L	H	80	16	125
H	H	L	80	15	133.33
H	H	H	80	12	166.67

TABLE 3B. BANK QAB FREQUENCY SELECT FUNCTION TABLE

Inputs			Output Frequency
XTAL_IN/REF_IN (MHz)	M Divider Value	NAB Divider Value	QAB (MHz)
25	80	16	125

Table 3C. Bank QB Frequency Select Function Table

Inputs					Output Frequency (25MHz Reference)
F_SELB2	F_SELB1	F_SELB0	M Divider Value	NB Divider Value	QB (0:2) (MHz)
L	L	L	80	60	33.33
L	L	H	80	40	50
L	H	L	80	30	66.67
L	H	H	80	24	83.33
H	L	L	80	20	100
H	L	H	80	16	125
H	H	L	80	15	133.33
H	H	H	80	12	166.67

Table 3D. Slew Rate Function Table

Setting		Slew Rate
SLEW1	SLEW0	(V/ns)
0	0	4
0	1	3
1	0	2
1	1	1

NOTE: Please refer to the AC Characteristics Table for slew rate test condition.

Table 3E. REF_SEL Function Table

Input	
REF_SEL	Input Reference
0	XTAL_IN
1	REF_IN

Table 3F. MR/nOE Function Table

Input	
MR/nOE	Function; NOTE1
0	Output Enable
1	Device reset, output disabled (Low)

NOTE 1: The device requires a reset signal after power-up to function properly.

Table 3G. nREF_OE Function Table

Input	
nREF_OE	Function
0	REF_OUT[1:0] enabled
1	REF_OUT[1:0] disabled (Low)

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO_X} + 0.5V
Package Thermal Impedance, θ_{JA}	36.25°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, V_{DD} = V_{DDO_REF} = V_{DDO_AA} = V_{DDO_AB} = V_{DDO_B} = 3.3V±5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		$V_{DD} – I_{DDA}$*10Ω	3.3	V_{DD}	V
V_{DDO_AA}, V_{DDO_AB}, V_{DDO_B}, V_{DDO_REF}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			TBD		mA
I_{DDA}	Analog Supply Current			TBD		mA
I_{DDO_AA}, I_{DDO_AB}, I_{DDO_B}, I_{DDO_REF}	Output Supply Current			TBD		mA

Table 4B. Power Supply DC Characteristics, V_{DD} = 3.3V±5%, V_{DDO_REF} = V_{DDO_AA} = V_{DDO_AB} = V_{DDO_B} = 2.5V±5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		$V_{DD} – I_{DDA}$*10Ω	3.3	V_{DD}	V
V_{DDO_AA}, V_{DDO_AB}, V_{DDO_B}, V_{DDO_REF}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			TBD		mA
I_{DDA}	Analog Supply Current			TBD		mA
I_{DDO_AA}, I_{DDO_AB}, I_{DDO_B}, I_{DDO_REF}	Output Supply Current			TBD		mA

TABLE 4C. LVCMOS/LVTTL DC CHARACTERISTICS, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD} + 0.3	V
			V_{DD} = 3.3V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
			V_{DD} = 3.3V	-0.3		0.7	V
I_{IH}	Input High Current	nREF_OE, F_SELAA0	V_{DD} = V_{IN} = 3.465V			5	µA
		REF_IN, REF_SEL, SLEW0, SLEW1, F_SELAA[1, 2], F_SELB[0:2], MR/nOE	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	nREF_OE, F_SELAA0	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
		REF_IN, REF_SEL, SLEW0, SLEW1, F_SELAA[1, 2], F_SELB[0:2], MR/nOE	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage; NOTE 1		$V_{DDO\_AA\_AB,,\_B,\_REF}$ = 3.3V±5%	2.6			V
			$V_{DDO\_AA\_AB,,\_B,\_REF}$ = 2.5V±5%	1.8			V
V_{OL}	Output Low Voltage; NOTE 1		$V_{DDO\_AA\_AB,,\_B,\_REF}$ = 3.3V or 2.5V±5%			0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO\_AA\_AB,,\_B,\_REF}$/2. See Parameter Measurement Information, *Output Load Test Circuit diagrams.*

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				100	µW

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6A. AC CHARACTERISTICS, $V_{DD} = V_{DDO\_REF} = V_{DDO\_AA} = V_{DDO\_AB} = V_{DDO\_B}$ = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	QAB			125		MHz
		QAA, QB0:2		33.33		167.67	MHz
*t*sk(o)	Output Skew; NOTE 1, 2				50		ps
*t*sk(b)	Bank Skew; NOTE 2, 3				TBD		ps
*t*jit(per)	RMS Period Jitter		125MHz		TBD		ps
t_{SLEW}	Slew Rate; NOTE 4	SLEWx = 00	Single-ended Output Clock Rise/Fall Time, 20% to 80%; 15pF Load		4		V/ns
		SLEWx = 01			3		V/ns
		SLEWx = 10			2		V/ns
		SLEWx = 11			1		V/ns
t_L	PLL Lock Time				TBD		ms
odc	Output Duty Cycle				50		%

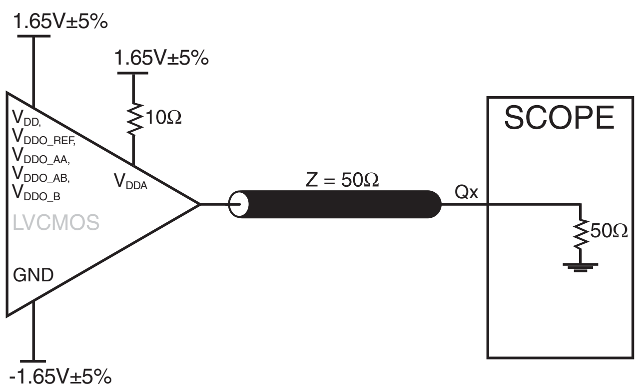
NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDO\_AA, \_AB, \_B, \_REF}/2$.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.
NOTE 4: A slew rate of 2V/ns or greater should be selected for output frequencies of 100MHz and higher.

TABLE 6B. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, $V_{DDO\_REF} = V_{DDO\_AA} = V_{DDO\_AB} = V_{DDO\_B}$ = 2.5V±5%, TA = -40°C TO 85°C

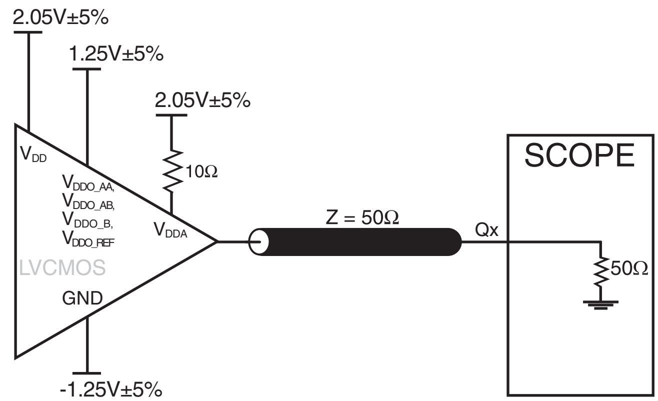
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	QAB			125		MHz
		QAA, QB0:2		33.33		167.67	MHz
*t*sk(o)	Output Skew; NOTE 1, 2				50		ps
*t*sk(b)	Bank Skew; NOTE 2, 3				TBD		ps
*t*jit(per)	RMS Period Jitter		125MHz		TBD		ps
t_{SLEW}	Slew Rate; NOTE 4	SLEWx = 00	Single-ended Output Clock Rise/Fall Time, 20% to 80%; 15pF Load		4		V/ns
		SLEWx = 01			3		V/ns
		SLEWx = 10			2		V/ns
		SLEWx = 11			1		V/ns
t_L	PLL Lock Time				TBD		ms
odc	Output Duty Cycle				50		%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDO\_AA, \_AB, \_B, \_REF}/2$.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.
NOTE 4: A slew rate of 2V/ns or greater should be selected for output frequencies of 100MHz and higher.

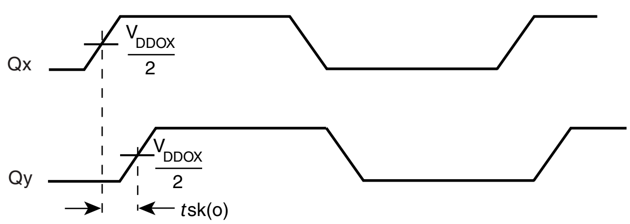
Parameter Measurement Information



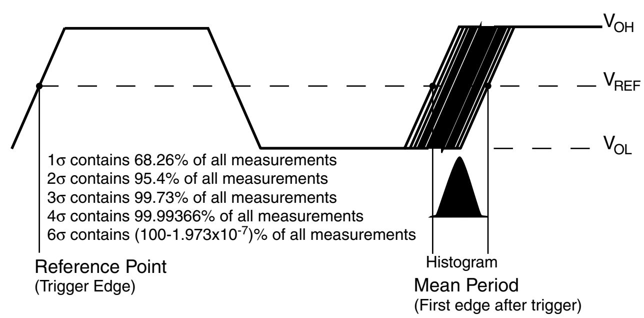
3.3V Core/3.3V Output Load AC Test Circuit



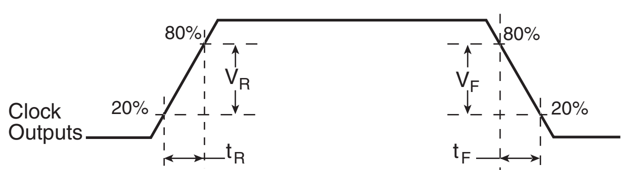
3.3V Core/2.5V Output Load AC Test Circuit



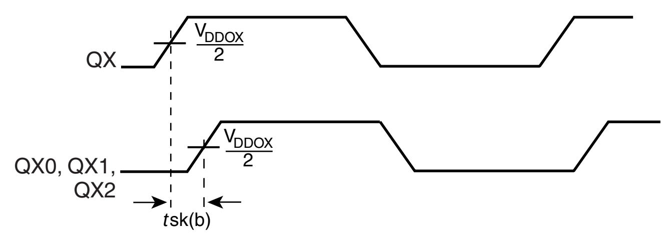
Output Skew



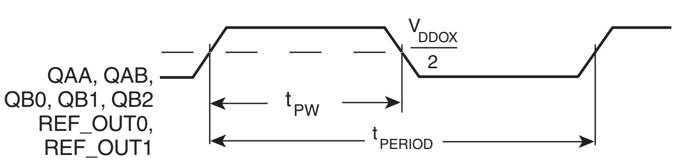
RMS Period Jitter



Output Slew Rate



Bank Skew (where X denotes outputs in the same bank)



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

Output Duty Cycle/Pulse Width/Period

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS840S07I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDO_X} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin. The 10Ω resistor can also be replaced by a ferrite bead.

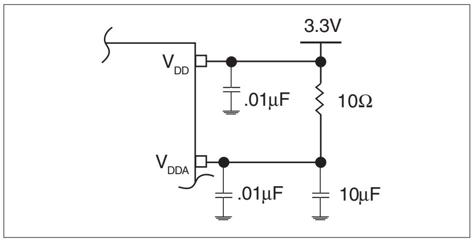


FIGURE 1. POWER SUPPLY FILTERING

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

LVCMOS CONTROL PINS

All control pins have internal pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

CRYSTAL INPUTS

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_IN INPUT

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_IN to ground.

OUTPUTS:

LVCMOS OUTPUTS

All unused LVCMOS output can be left floating. There should be no trace attached.

Crystal Input Interface

The ICS840S07I has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

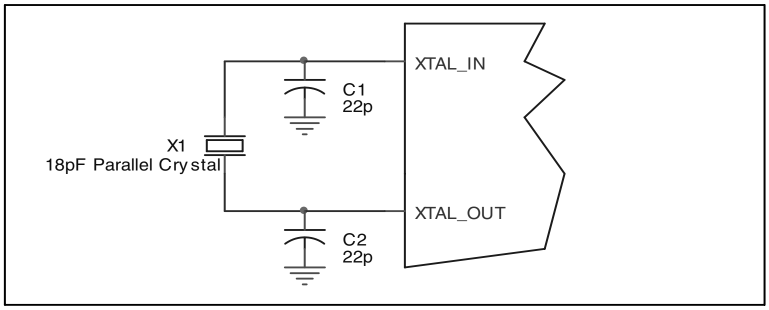


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

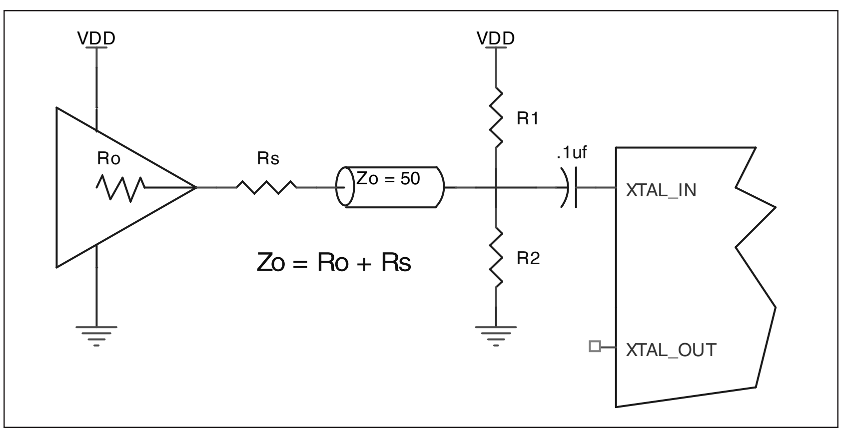


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor's Thermally/Electrically Enhance Leadfame Base Package, Amkor Technology.

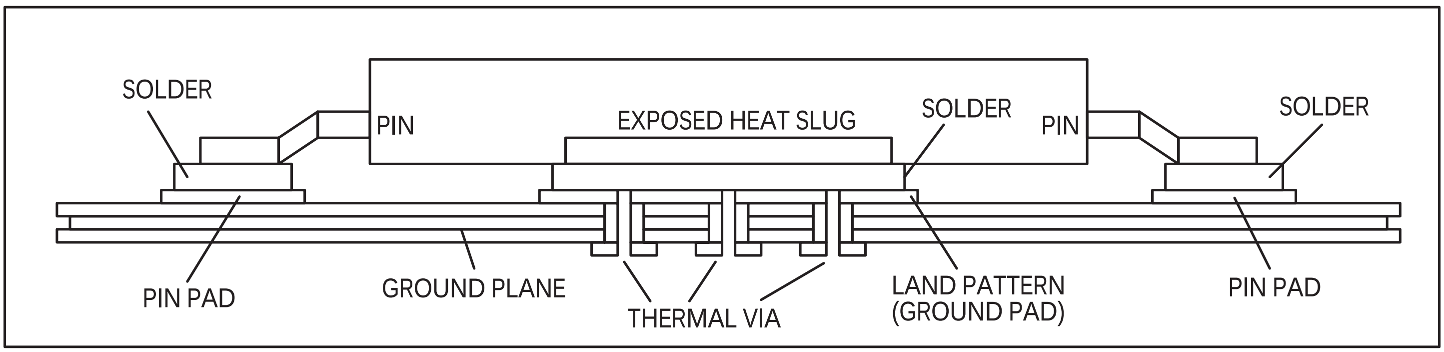


Figure 4. Assembly for Exposed Pad Thermal Release Path –Side View (Drawing not to Scale)

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for 32 Lead TQFP, E-Pad

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	36.2°C/W	30.6°C/W	29.2°C/W

Transistor Count

The transistor count for ICS840S07I is: 2349

TQFP Package Outline - Y Suffix for 32 Lead TQFP, E-Pad

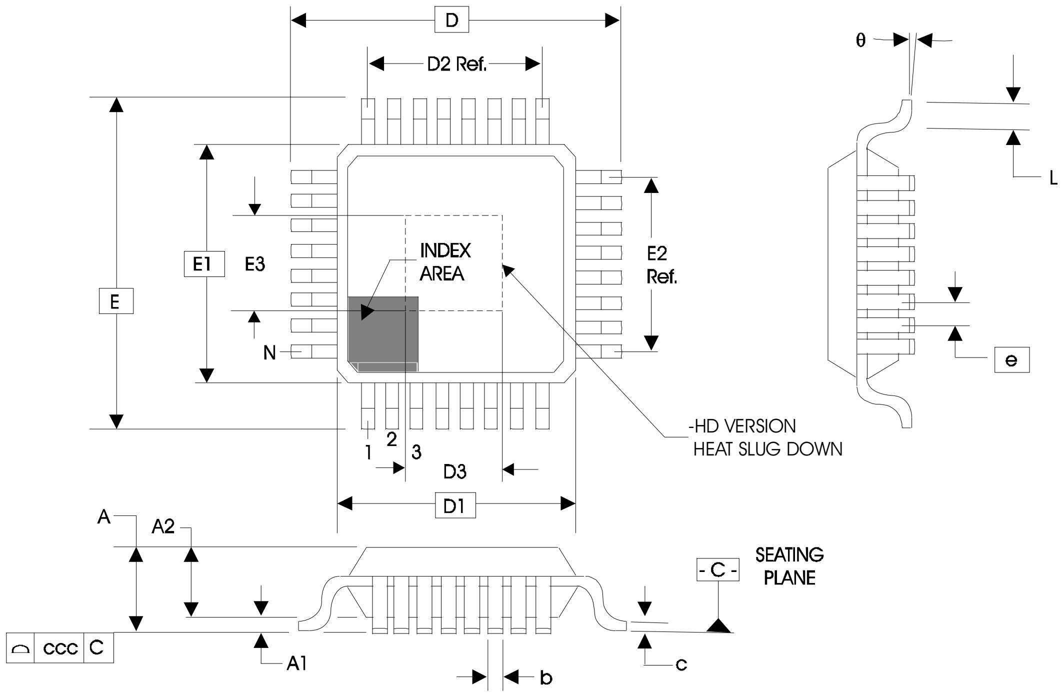


Table 8. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.20
A1	0.05	--	0.15
A2	0.95	1.0	1.05
b	0.30	0.35	0.40
c	0.09	--	0.20
D, E		9.00 BASIC	
D1, E1		7.00 BASIC	
D2, E2		5.60 Ref.	
D3, E3	3.0	3.5	4.0
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS840S07BYI	ICS840S07BYI	32 lead TQFP, E-Pad	tube	-40°C to 85°C
ICS840S07BYIT	ICS840S07BYI	32 lead TQFP, E-Pad	2500 tape & reel	-40°C to 85°C
ICS840S07BYILF	TBD	32 lead "Lead-Free" TQFP, E-Pad	tube	-40°C to 85°C
ICS840S07BYILFT	TBD	32 lead "Lead-Free" TQFP, E-Pad	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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