



**Table 1. Pin Descriptions**

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential output pair. LVDS interface levels.
3	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
4	nPLL_SEL	Input	Pulldown	Selects between the PLL and REF_CLK as input to the dividers. When LOW, selects PLL (PLL Enable). When HIGH, deselects the reference clock (PLL Bypass). LVCMOS/LVTTL interface levels.
5, 6, 7, 8, 15, 16, 20, 21, 28, 29	nc	Unused		No connect.
9	V <sub>DDA</sub>	Power		Analog supply pin.
10, 12	F_SEL0, F_SEL1	Input	Pulldown	Frequency select pin. LVCMOS/LVTTL interface levels.
11	V <sub>DD</sub>	Power		Core supply pin.
13, 14	XTAL_OUT XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
17, 22	GND	Power		Power supply ground.
18	REF_CLK	Input	Pulldown	Single-ended reference clock input. LVCMOS/LVTTL interface levels.
19	nXTAL_SEL	Input	Pulldown	Selects between crystal or REF_CLK inputs as the PLL Reference source. Selects XTAL inputs when LOW. Selects REF_CLK when HIGH. LVCMOS/LVTTL interface levels.
23, 24	nQ3, Q3	Output		Differential output pair. LVDS interface levels.
25, 32	V <sub>DDO</sub>	Power		Output supply pins.
26, 27	Q2, nQ2	Output		Differential output pair. LVDS interface levels.
30, 31	nQ1, Q1	Output		Differential output pair. LVDS interface levels.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $I_O$ Continuous Current Surge Current	10mA 15mA
Package Thermal Impedance, $\theta_{JA}$	42.4°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 3A. Power Supply DC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDA}$	Analog Supply Voltage		$V_{DD} - 0.12$	3.3	$V_{DD}$	V
$V_{DDO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{DD}$	Power Supply Current				105	mA
$I_{DDA}$	Analog Supply Current				12	mA
$I_{DDO}$	Output Supply Current				120	mA

**Table 3B. Power Supply DC Characteristics,  $V_{DD} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		2.375	2.5	2.625	V
$V_{DDA}$	Analog Supply Voltage		$V_{DD} - 0.10$	2.5	$V_{DD}$	V
$V_{DDO}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current				100	mA
$I_{DDA}$	Analog Supply Current				10	mA
$I_{DDO}$	Output Supply Current				100	mA

**Table 3C. LVCMOS/LVTTL DC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	$V_{DD} = 3.3V$	2		$V_{DD} + 0.3$	V
		$V_{DD} = 2.5V$	1.7		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	$V_{DD} = 3.3V$	-0.3		0.8	V
		$V_{DD} = 2.5V$	-0.3		0.7	
$I_{IH}$	Input High Current	REF_CLK, MR, F_SEL[0:1], nPLL_SEL, nXTAL_SEL $V_{DD} = V_{IN} = 3.465V$ or $2.625V$			150	$\mu\text{A}$
$I_{IL}$	Input Low Current	REF_CLK, MR, F_SEL[0:1], nPLL_SEL, nXTAL_SEL $V_{DD} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-5			$\mu\text{A}$

**Table 3D. LVDS DC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OD}$	Differential Output Voltage		300	450	600	mV
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change				50	mV
$V_{OS}$	Offset Voltage		1.2	1.425	1.65	V
$\Delta V_{OS}$	$V_{OS}$ Magnitude Change				50	mV

**Table 3E. LVDS DC Characteristics,  $V_{DD} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OD}$	Differential Output Voltage		250	400	550	mV
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change				50	mV
$V_{OS}$	Offset Voltage		1.0	1.2	1.4	V
$\Delta V_{OS}$	$V_{OS}$ Magnitude Change				50	mV

**Table 4. Crystal Characteristics**

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		23.33	26.5625	28.33	MHz
Equivalent Series Resistance (ESR)				50	$\Omega$
Shunt Capacitance				7	pF

NOTE: Characterized using an 18pF parallel resonant crystal.

## AC Electrical Characteristics

**Table 5A. AC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency	$F\_SEL[1:0] = 00$	186.67		226.66	MHz
		$F\_SEL[1:0] = 01$	140		170	MHz
		$F\_SEL[1:0] = 10$	93.33		113.33	MHz
		$F\_SEL[1:0] = 11$	46.67		56.66	MHz
$t_{sk(o)}$	Output Skew; NOTE 1, 2			35	ps	
$f_{jit}(\emptyset)$	RMS Phase Jitter, Random; NOTE 3	212.5MHz, (637kHz - 10MHz)		0.73		ps
		159.375MHz, (637kHz - 10MHz)		0.78		ps
		106.25MHz, (637kHz - 10MHz)		0.92		ps
		53.125MHz, (637kHz - 10MHz)		0.95		ps
		187.5MHz, (637kHz - 10MHz)		0.75		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	250		500	ps
odc	Output Duty Cycle	$F\_SEL[1:0] \neq \div 3$	48		52	%
		$F\_SEL[1:0] = \div 3$	40		60	%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at the differential cross points.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Please refer to the Phase Noise Plots.

**Table 5B. AC Characteristics,  $V_{DD} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

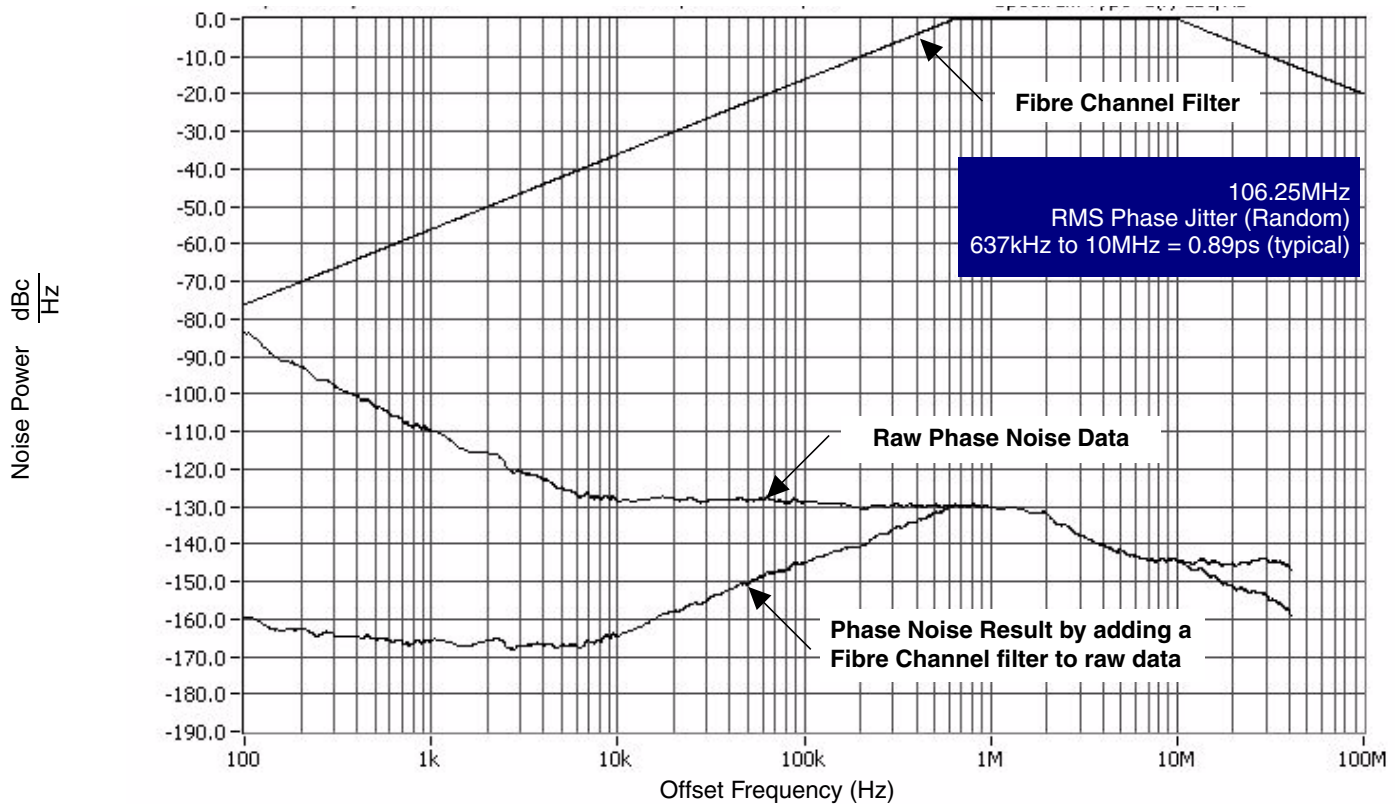
Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency	$F\_SEL[1:0] = 00$	186.67		226.66	MHz
		$F\_SEL[1:0] = 01$	140		170	MHz
		$F\_SEL[1:0] = 10$	93.33		113.33	MHz
		$F\_SEL[1:0] = 11$	46.67		56.66	MHz
$t_{sk(o)}$	Output Skew; NOTE 1, 2			35	ps	
$f_{jit}(\emptyset)$	RMS Phase Jitter, Random; NOTE 3	212.5MHz, (637kHz - 10MHz)		0.72		ps
		159.375MHz, (637kHz - 10MHz)		0.88		ps
		106.25MHz, (637kHz - 10MHz)		0.89		ps
		53.125MHz, (637kHz - 10MHz)		0.96		ps
		187.5MHz, (637kHz - 10MHz)		0.74		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	250		550	ps
odc	Output Duty Cycle	$F\_SEL[1:0] \neq \div 3$	48		52	%
		$F\_SEL[1:0] = \div 3$	40		60	%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at the differential cross points.

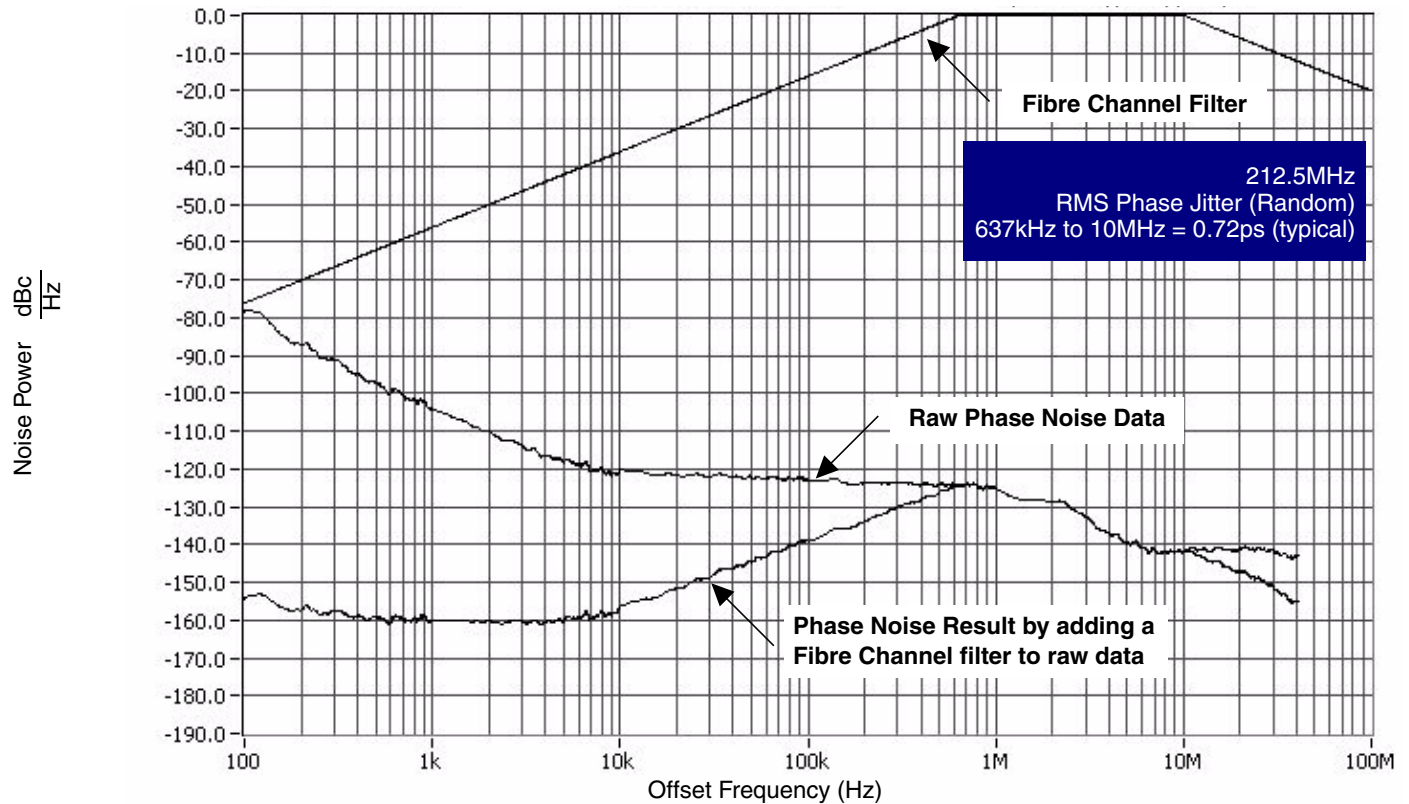
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Please refer to the Phase Noise Plots.

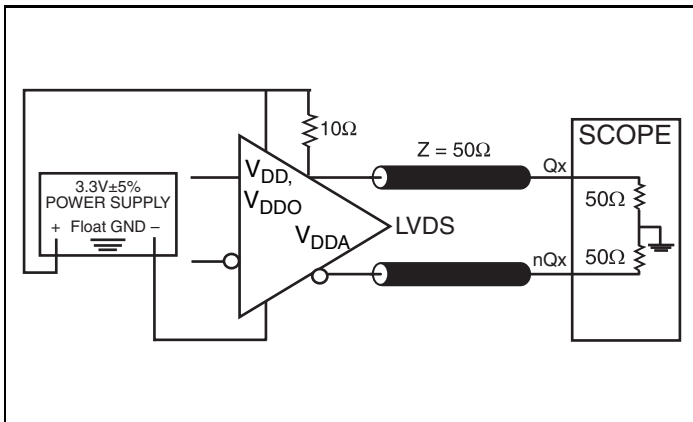
## Typical Phase Noise at 106.25MHz (3.3V)



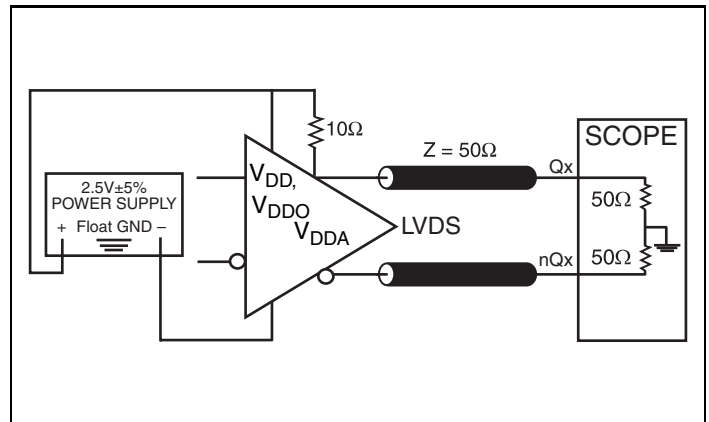
## Typical Phase Noise at 212.5MHz (3.3V)



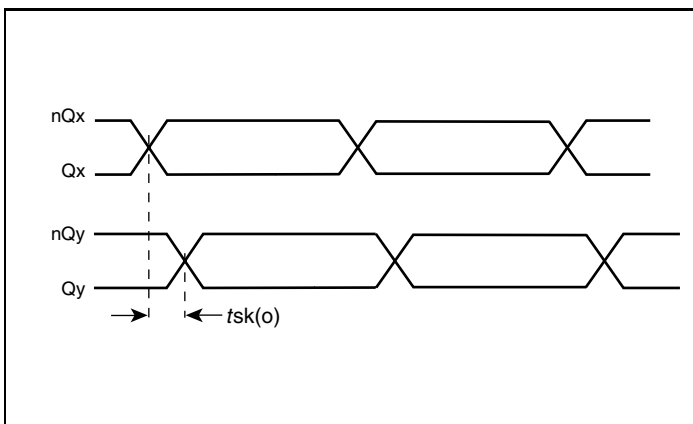
### Parameter Measurement Information



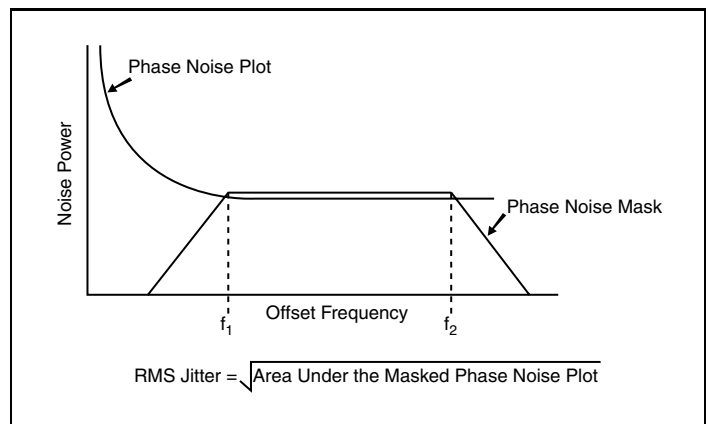
3.3V LVDS Output Load AC Test Circuit



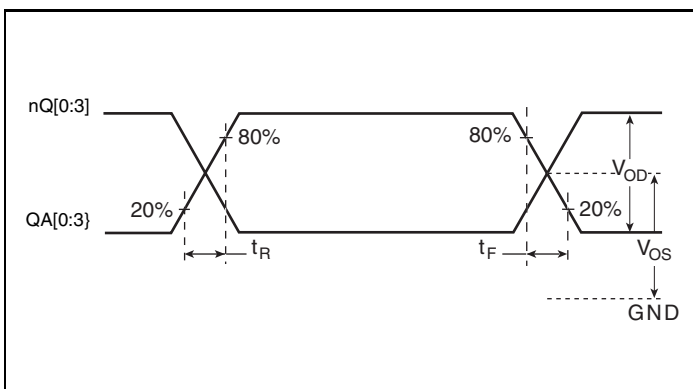
2.5V LVDS Output Load AC Test Circuit



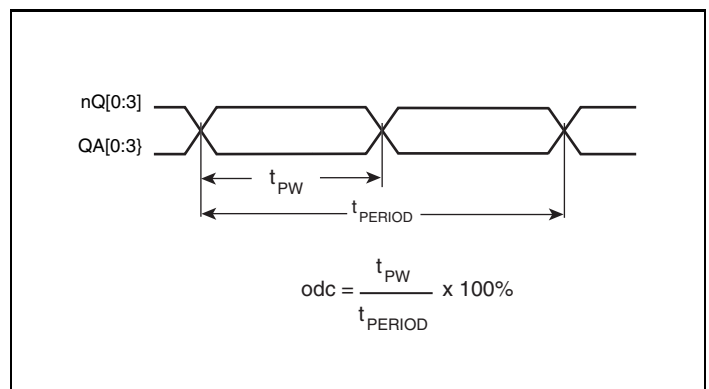
Output Skew



RMS Phase Jitter

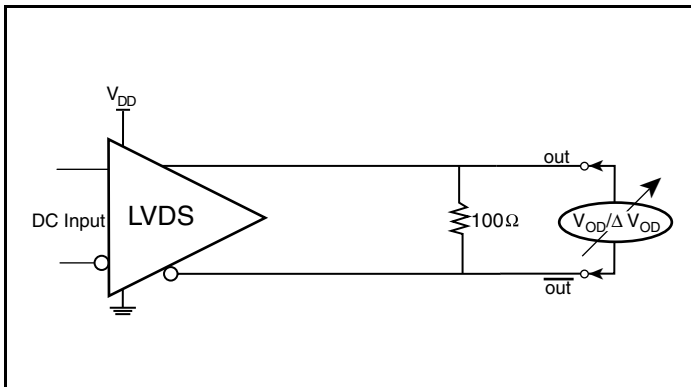


Output Rise/Fall Time

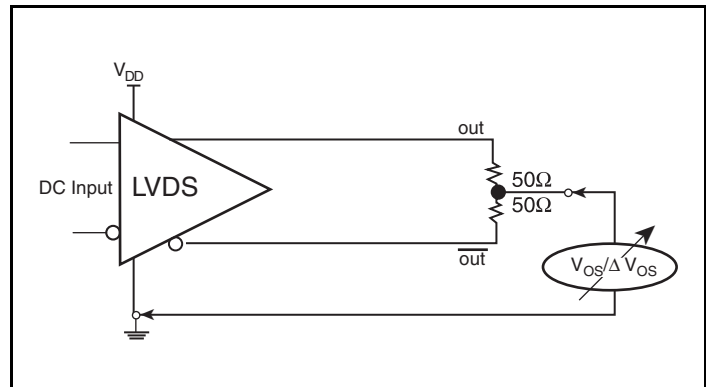


Output Duty Cycle/Pulse Width/Period

## Parameter Measurement Information, continued



Differential Output Voltage Setup



Offset Voltage Setup

## Application Information

### Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS844004-104 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DD}$ ,  $V_{DDA}$  and  $V_{DDO}$  should be individually connected to the power supply plane through vias, and  $0.01\mu\text{F}$  bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic  $V_{DD}$  pin and also shows that  $V_{DDA}$  requires that an additional  $10\Omega$  resistor along with a  $10\mu\text{F}$  bypass capacitor be connected to the  $V_{DDA}$  pin.

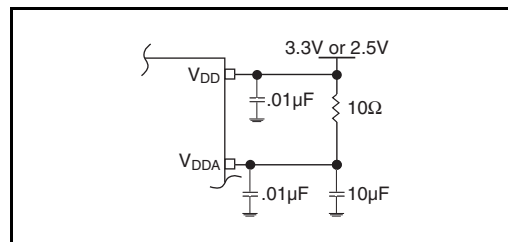


Figure 1. Power Supply Filtering



## Crystal Input Interface

The ICS844004-104 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 26.5625MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

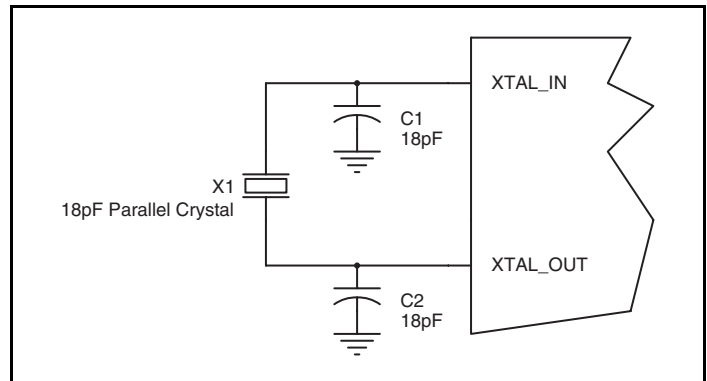


Figure 2. Crystal Input Interface

## LVC MOS to XTAL Interface

The XTAL\_IN input can accept a single-ended LVC MOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3*. The XTAL\_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVC MOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output

impedance of the driver ( $R_o$ ) plus the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most 50Ω applications,  $R_1$  and  $R_2$  can be 100Ω. This can also be accomplished by removing  $R_1$  and making  $R_2$  50Ω.

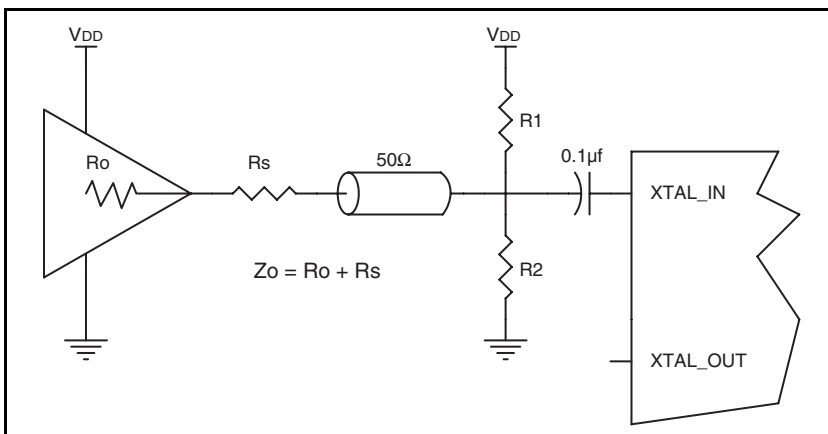


Figure 3. General Diagram for LVC MOS Driver to XTAL Input Interface

## Recommendations for Unused Input and Output Pins

### Inputs:

#### LVC MOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

#### REF\_CLK INPUT

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from the REF\_CLK to ground.

### Outputs:

#### LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100 $\Omega$  across. If they are left floating, we recommend that there is no trace attached.

## 3.3V, 2.5V LVDS Driver Termination

A general LVDS interface is shown in *Figure 4*. In a 100 $\Omega$  differential transmission line environment, LVDS drivers require a matched load termination of 100 $\Omega$  across near the receiver input.

For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

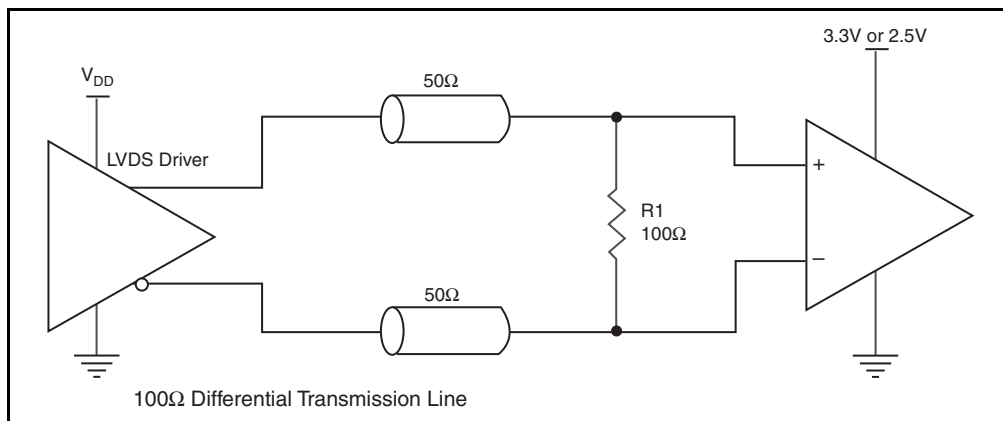


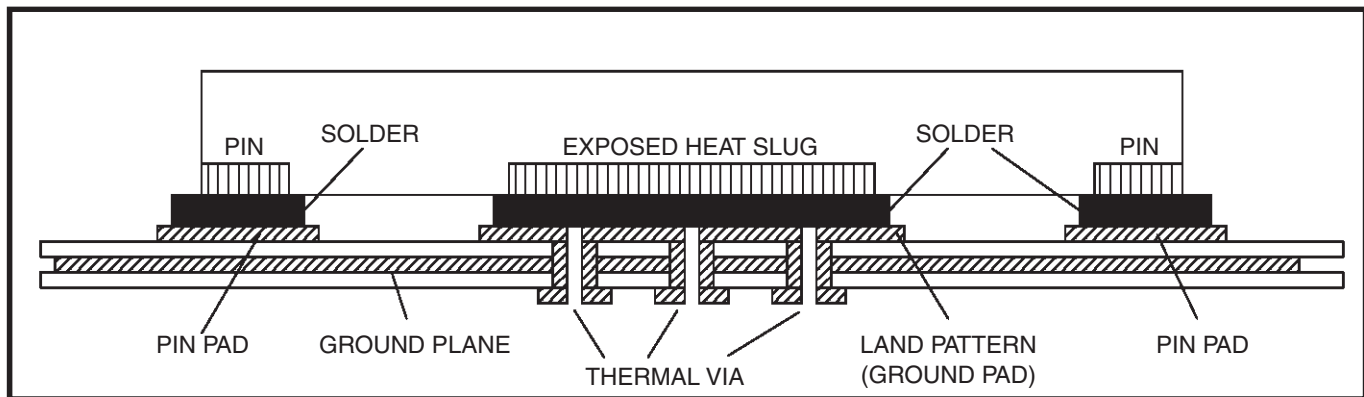
Figure 4. Typical LVDS Driver Termination

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 5*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are

application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.



**Figure 5. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**

### Schematic Example

Figure 6 shows an example of ICS844004-104 application schematic. In this example, the device is operated at VDD = VDDO = 3.3V. The 18pF parallel resonant 25MHz crystal is used. The C1 = 33pF and C2 = 22pF are recommended for frequency accuracy.

For different board layouts, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. Two examples of LVDS for receiver without built-in termination are show in this schematic.

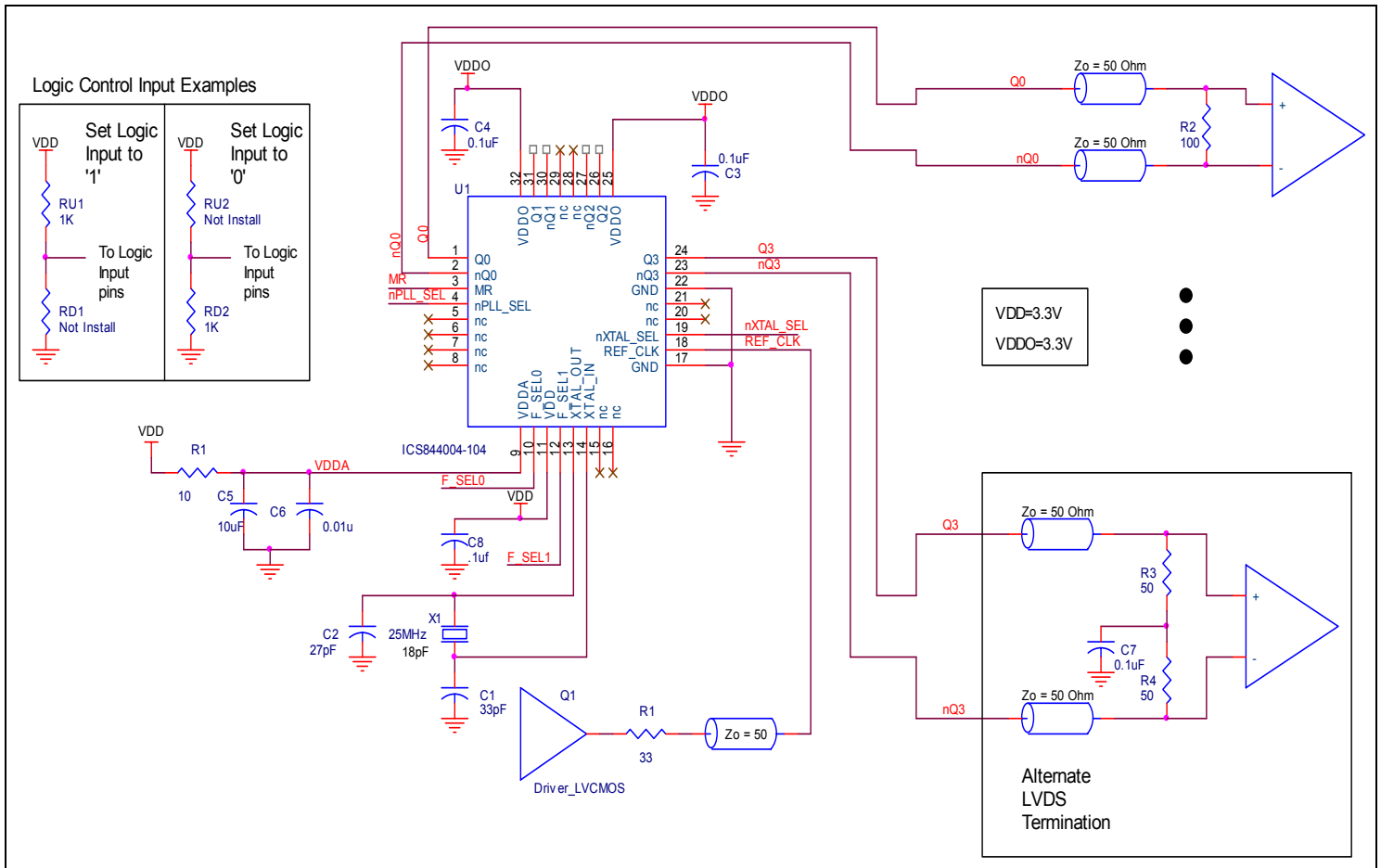


Figure 6. ICS844004-104 Schematic Example

## Power Considerations

This section provides information on power dissipation and junction temperature for the ICS844004-104. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS844004-104 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX}) = 3.465V * (105mA + 12mA) = \mathbf{405.4mW}$
- Power (outputs)<sub>MAX</sub> =  $V_{DDO\_MAX} * I_{DDO\_MAX} = 3.465V * 120mA = \mathbf{415.8mW}$

**Total Power**<sub>MAX</sub> = 405.4mW + 415.8mW = **821.2mW**

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 42.4°C/W per Table 7 below.

Therefore,  $T_j$  for an ambient temperature of 70°C with all outputs switching is:

$70^\circ\text{C} + 0.821W * 42.4^\circ\text{C/W} = 104.8^\circ\text{C}$ . This is well below the limit of 125°C.

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 7. Thermal Resistance  $\theta_{JA}$  for 32 Lead VFQFN, Forced Convection**

Meters per Second	$\theta_{JA}$ vs. Air Flow		
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	42.4°C/W	37.0°C/W	33.2°C/W

## Reliability Information

Table 8.  $\theta_{JA}$  vs. Air Flow Table for a 32 Lead VFQFN

$\theta_{JA}$ vs. Air Flow			
Meter per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	42.4°C/W	37.0°C/W	33.2°C/W

## Transistor Count

The transistor count for ICS844004-104 is: 2914

## Package Outline and Package Dimensions

### Package Outline - K Suffix for VFQFN Packages

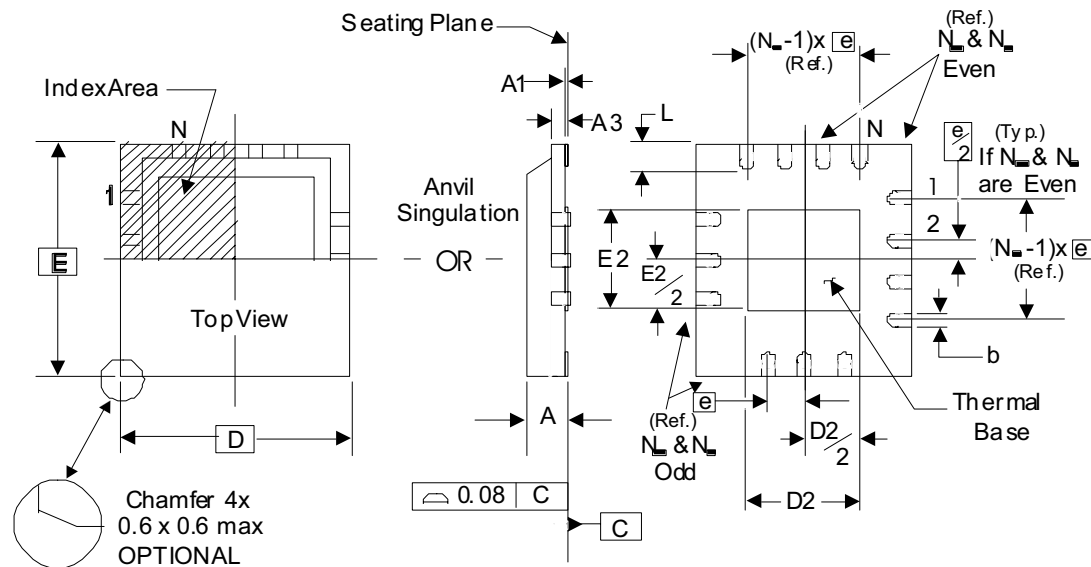


Table 9. Package Dimensions

JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters			
Symbol	Minimum	Nominal	Maximum
N	32		
A	0.80		1.00
A1	0		0.05
A3	0.25 Ref.		
b	0.18	0.25	0.30
N <sub>D</sub> & N <sub>E</sub>	8		
D & E	5.00 Basic		
D2 & E2	3.0		3.3
e	0.50 Basic		
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

**NOTE:** The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 8 below.

## Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
844004AK-104	ICS4044A104	32 Lead VFQFN	Tray	0°C to 70°C
844004AK-104T	ICS4044A104	32 Lead VFQFN	2500 Tape & Reel	0°C to 70°C
844004AK-104LF	ICS004A104L	"Lead-Free" 32 Lead VFQFN	Tray	0°C to 70°C
844004AK-104LFT	ICS004A104L	"Lead-Free" 32 Lead VFQFN	2500 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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