FEMTOCLOCK™ CRYSTAL/LVCMOS-TO-LVDS/LVCMOS FREQUENCY SYNTHESIZER

ICS8440258-46

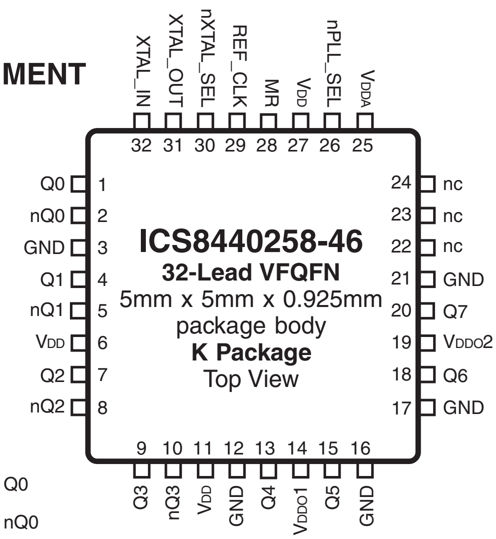
General Description

The ICS8440258-46 is an 8 output synthesizer optimized to generate Ethernet clocks and a member of the HiPerClockS™family of high performance clock solutions from IDT. Using a 25MHz, 18pF parallel resonant crystal, the device will generate both 125MHz and 25MHz clocks with mixed LVDS and LVCMOS/LVTTL output logic. The ICS8440258-46 uses IDT's 3rd generations low phase noise VCO technology and can achieve <1ps typical rms phase jitter, easily meeting Ethernet jitter requirements. The ICS8440258-46 is packaged in a small, 5mm x 5mm VFQFN package.

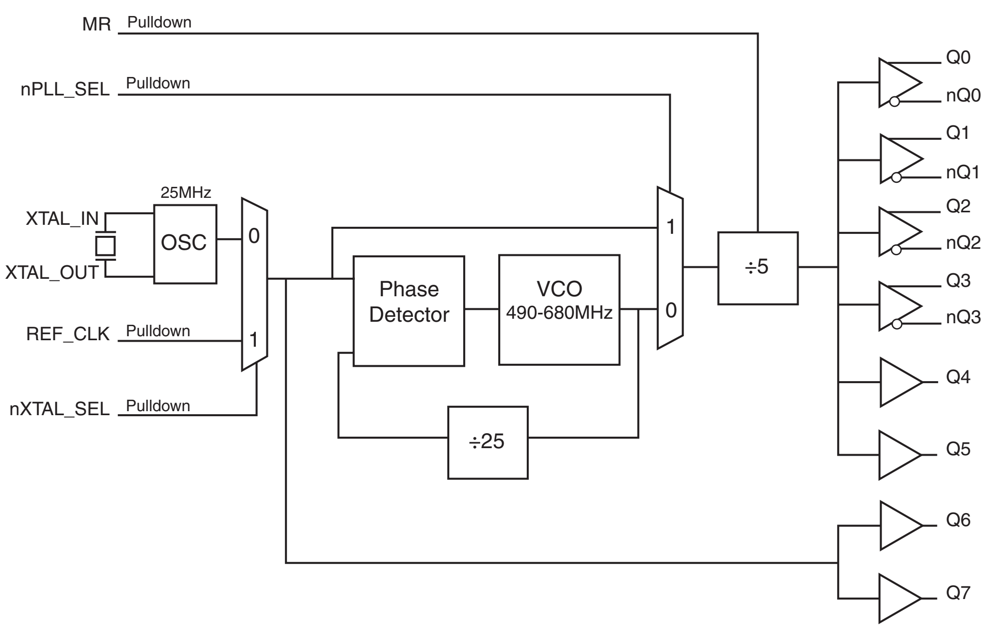
Features

- Four differential LVDS outputs at 125MHz
  Two LVCMOS/LVTTL single-ended outputs at 125MHz
  Two LVCMOS/LVTTL single-ended outputs at 25MHz
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- VCO range: 490MHz - 680MHz
- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.34ps (typical)
- Full 2.5V operating supply
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS6) packages

Pin Assignment



Block Diagram



The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential clock outputs. LVDS interface levels.
3, 12, 16, 17, 21	GND	Power		Power supply ground.
4, 5	Q1, nQ1	Output		Differential clock outputs. LVDS interface levels.
6, 11, 27	V_{DD}	Power		Core supply pin.
7, 8	Q2, nQ2	Output		Differential clock outputs. LVDS interface levels.
9, 10	Q3, nQ3	Output		Differential clock outputs. LVDS interface levels.
13, 15, 18, 20	Q4, Q5, Q6, Q7	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.
14	V_{DDO1}	Power		Power output supply pin for Q4 and Q5 LVCMOS outputs.
19	V_{DDO2}	Power		Power output supply pin for Q6 and Q7 LVCMOS outputs.
22, 23, 24	nc	Unused		No connect.
25	V_{DDA}	Power		Analog supply pin.
26	nPLL_SEL	Input	Pulldown	PLL Bypass. When LOW, the output is driven from the VCO output. When HIGH, the PLL is bypassed and the output frequency = reference clock frequency/N output divider. LVCMOS/LVTTL interface levels.
28	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the outputs to go low. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
29	REF_CLK	Input	Pulldown	Single-ended LVCMOS/LVTTL reference clock input.
30	nXTAL_SEL	Input	Pulldown	Selects between the crystal or REF_CLK inputs as the PLL reference source. When HIGH, selects REF_CLK. When LOW, selects XTAL inputs. LVCMOS/LVTTL interface levels.
31, 32	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_OUT is the output. XTAL_IN is the input.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance			8		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance			22		Ω

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O (LVCMOS)	-0.5V to V_{DD} + 0.5V
Outputs, I_O (LVDS)	
Continuous Current	10mA
Surge Current	15mA
Operating Temperature Range, T_A	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA}	37°C/W (0 mps)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 3A. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO1} = V_{DDO2}$ = 2.5V ± 5%, TA = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.13	2.5	V_{DD}	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}, I_{DDO1}, I_{DDO2}	Power Supply Current			170		mA
I_{DDA}	Analog Supply Current			13		mA

Table 3B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO1} = V_{DDO2}$ = 2.5V ± 5%, TA = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.7	V
I_{IH}	Input High Current	MR, REF_CLK, nPLL_SEL, nXTAL_SEL	$V_{DD} = V_{IN}$ = 2.625V			150	µA
I_{IL}	Input Low Current	MR, REF_CLK, nPLL_SEL, nXTAL_SEL	V_{DD} = 2.625V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage; NOTE 1	Q4:Q7	V_{DDO1}, V_{DDO1} = 2.625V±5%	1.8			V
V_{OL}	Output Low Voltage; NOTE 1	Q4:Q7	V_{DDO1}, V_{DDO1} = 2.625V±5%			0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DDOX}/2. See Parameter Measurement Information, Output Load Test Circuit diagram.

TABLE 3C. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO1} = V_{DDO2} = 2.5V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			390		mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage			1.25		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

TABLE 4. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

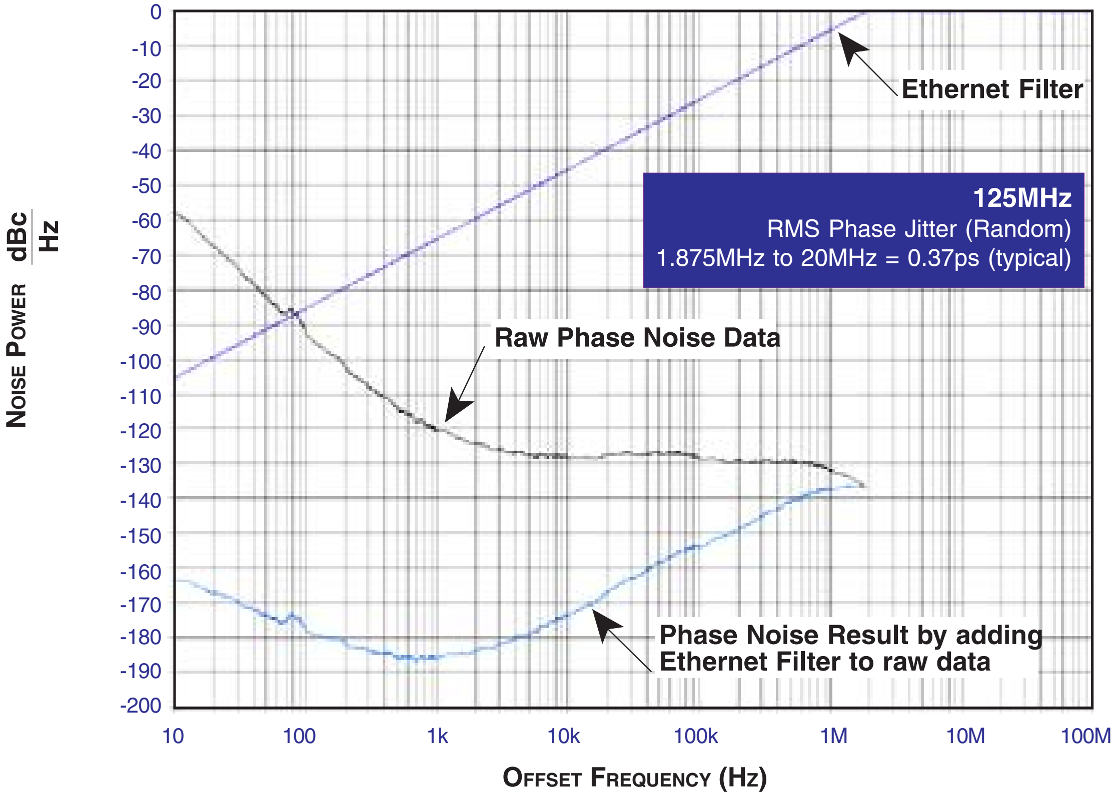
NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 5. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO1} = V_{DDO2} = 2.5V \pm 5\%$, $T_A = 0°C$ TO $70°C$

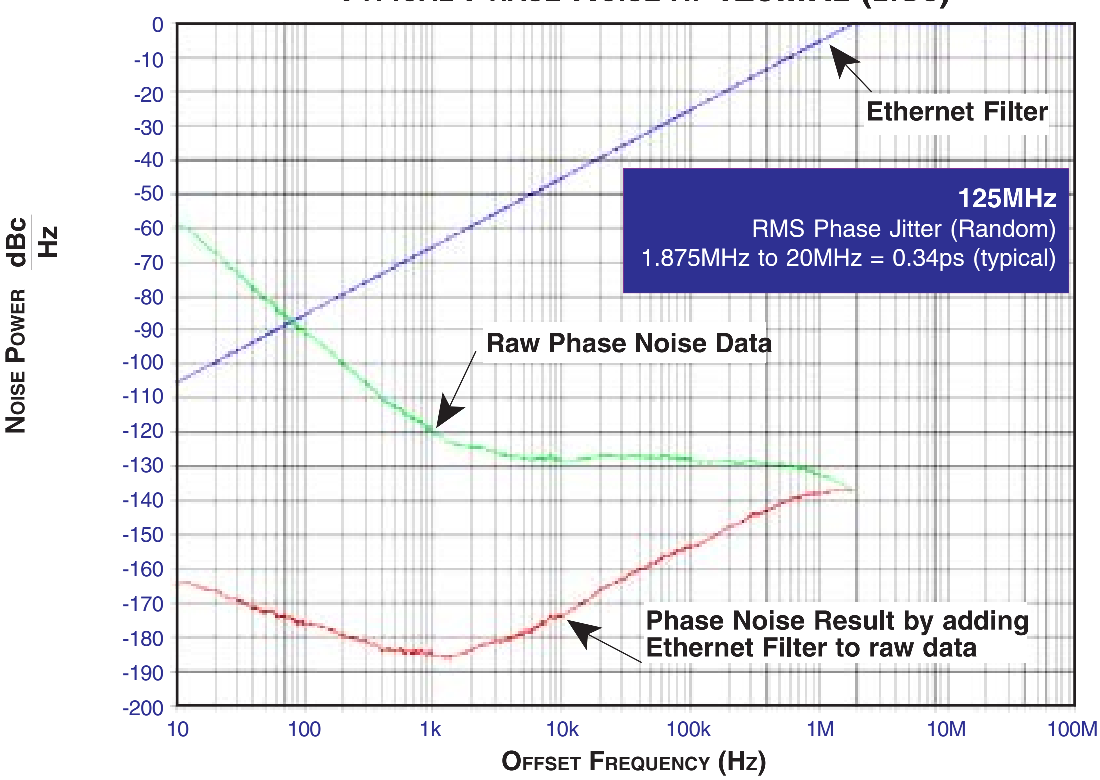
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	Q0:3/nQ0:3			125		MHz
		Q4, Q5			125		MHz
		Q6, Q7			25		MHz
*t*sk(o)	Output Skew; NOTE 1, 2	Q0:3/nQ0:3			50		ps
		Q4:Q7			50		ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 3	Q0:3/nQ0:3	125MHz, (1.875MHz - 20MHz)		0.34		ps
		Q4, Q5	125MHz, (1.875MHz - 20MHz)		0.37		ps
t_R / t_F	Output Rise/Fall Time	Q0:3/nQ0:3	20% to 80%		480		ps
		Q4:Q7	20% to 80%		1.4		ns
odc	Output Duty Cycle	Q0:3/nQ0:3			50		%
		Q4:Q7		46		54	%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDOX}/2$.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Please refer to the Phase Noise Plot.

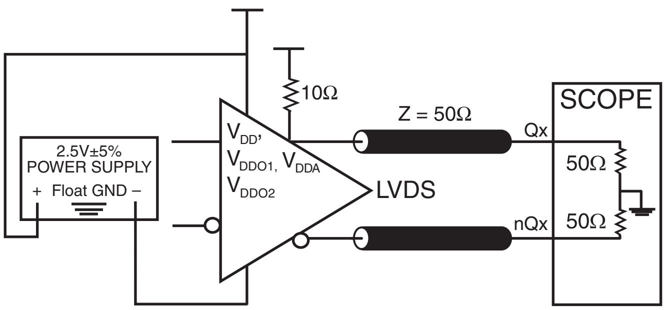
Typical Phase Noise at 125MHz (LVCMOS)



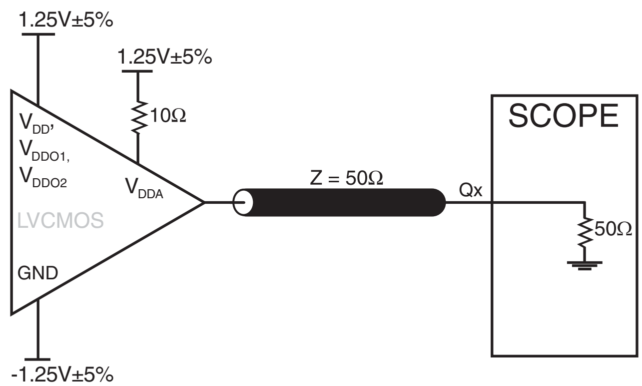
Typical Phase Noise at 125MHz (LVDS)



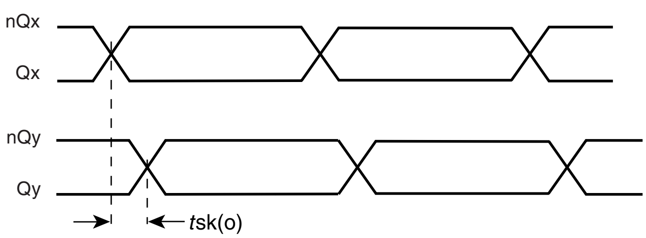
Parameter Measurement Information



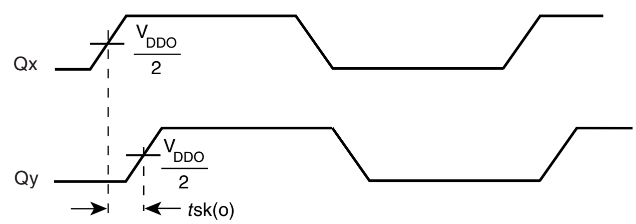
2.5V LVDS Output Load AC Test Circuit



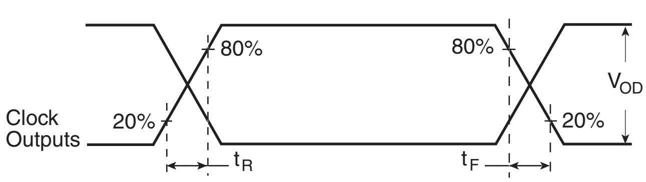
2.5V LVCMOS Output Load AC Test Circuit



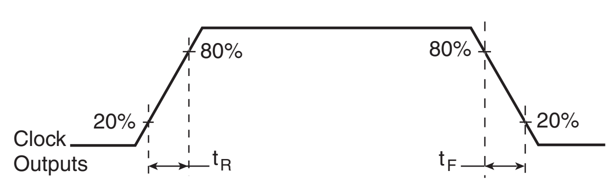
LVDS Output Skew



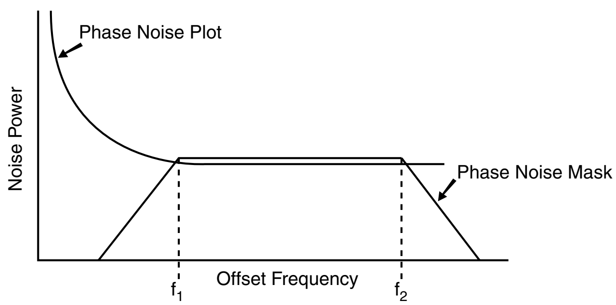
LVCMOS Output Skew



LVDS Output Rise/Fall Time

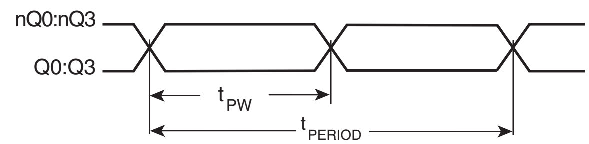


LVCMOS Output Rise/Fall Time



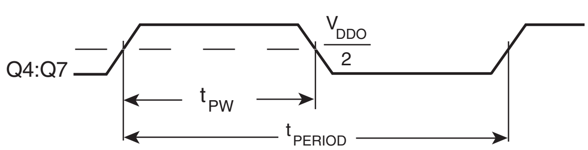
$$\text{RMS Jitter} = \sqrt{\text{Area Under the Masked Phase Noise Plot}}$$

RMS PHASE JITTER



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

LVDS OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

LVCMOS OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS8440258-46 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, V_{DDO1} and V_{DDO2} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a 0.01µF bypass capacitor should be connected to each V_{DDA}.

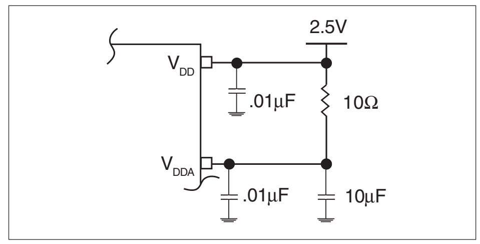


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS8440258-46 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

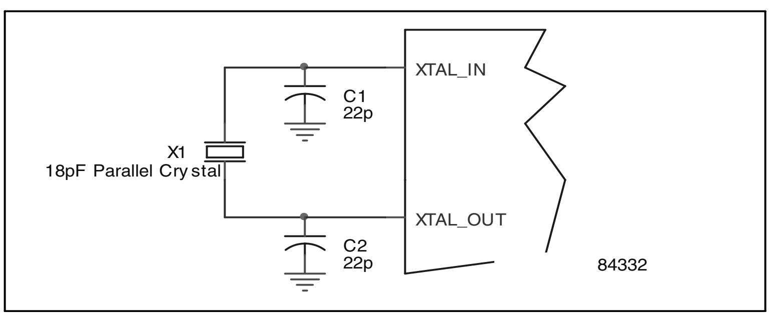


FIGURE 2. CRYSTAL INPUT INTERFACE

LVCMOS TO XTAL INTERFACE

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC couple capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

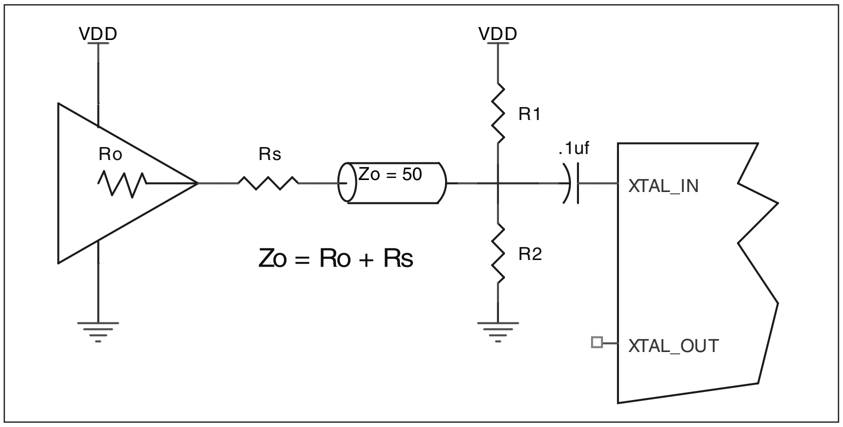


Figure 3. GENERAL DIAGRAM FOR LVCMOS DRIVER TO XTAL INPUT INTERFACE

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUTS
For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kW resistor can be tied from XTAL_IN to ground.

REF_CLK INPUT
For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

LVCMOS CONTROL PINS
All control pins have internal pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUTS
All unused LVCMOS output can be left floating. There should be no trace attached.

LVDS OUTPUTS
All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

2.5V LVDS Driver Termination

Figure 4 shows a typical termination for LVDS driver in characteristic impedance of 100Ω differential (50Ω single) transmission line environment. For buffer with multiple LDVS driver, it is recommended to terminate the unused outputs.

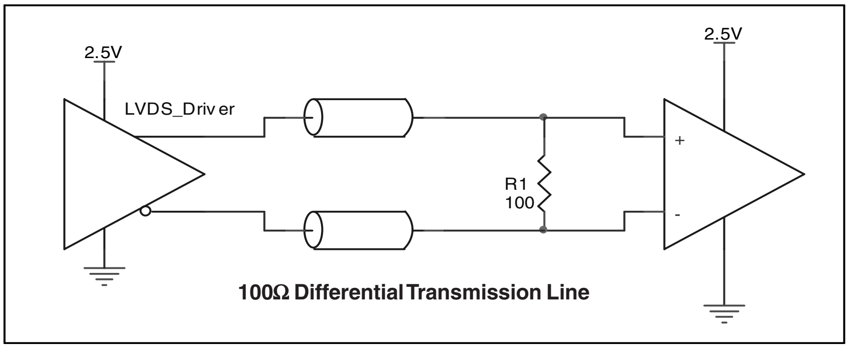


Figure 4. Typical LVDS Driver Termination

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 5.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/ slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/ Electrically Enhance Leadfame Base Package, Amkor Technology.

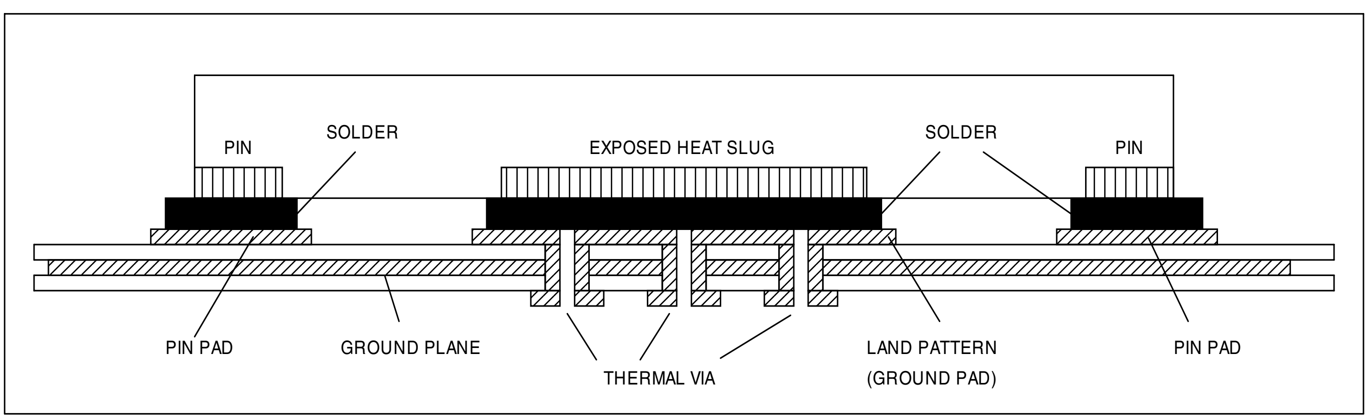


Figure 5. P.C.Assembly for Exposed Pad Thermal Release Path –Side View (Drawing not to Scale)

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8440258-46.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS840258-46 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 2.5V + 5% = 2.625V, which gives worst case results.

Core and LVDS Output Power Dissipation

- Power (core, LVDS) = V_{DD_MAX} * (I_{DD} + I_{DDO1} + I_{DDO2} + I_{DDA}) = 2.625V * (170mA + 13mA) = **480.4mW**

LVCMOS Output Power Dissipation

- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to V_{DDO}/2

  Output Current I_{OUT} = V_{DDO_MAX} / [2 * (50Ω + R_{OUT})] = 2.625V / [2 * (50Ω + 12Ω)] = **21.2mA**

- Power Dissipation on the R_{OUT} per LVCMOS output
  Power (R_{OUT}) = R_{OUT} * $(I_{OUT})^2$ = 12Ω * $(21.2mA)^2$ = **5.4mW per output**

- Total Power Dissipation on the R_{OUT}
  Total Power (R_{OUT}) = 5.4mW * 4 = **21.6mW**

- Dynamic Power Dissipation at 125MHz
  Power (125MHz) = C_{PD} * Frequency * $(V_{DDO})^2$ = 8pF * 125MHz * $(2.625V)^2$ = **6.9mW per output**
  Total Power (125MHz) = **6.9mW * 2 = 13.8mW**

- Dynamic Power Dissipation at 25MHz
  Power (25MHz) = C_{PD} * frequency * $(V_{DDO})^2$ = 8pF * 25MHz * $(2.625V)^2$ = **1.4 mW per output**
  Total Power (25MHz) = **1.4mW * 2 = 2.8mW**

Total Power Dissipation

- **Total Power**
  = Power (core, LVDS) + Total Power (R_{OUT}) + Total Power (125MHz) + Total Power (25MHz)
  = 480.4mW + 21.6mW + 13.8mW + 2.8mW
  = 518.6mW

2. *Junction Temperature.*

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37°C/W per Table 6.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.519W * 37°C/W = 89.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

Table 6. Thermal Resistance θ_{JA} for 32-Lead VFQFN, Forced Convection

θ_{JA} vs. Air Flow (Meters per Second)	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

Reliability Information

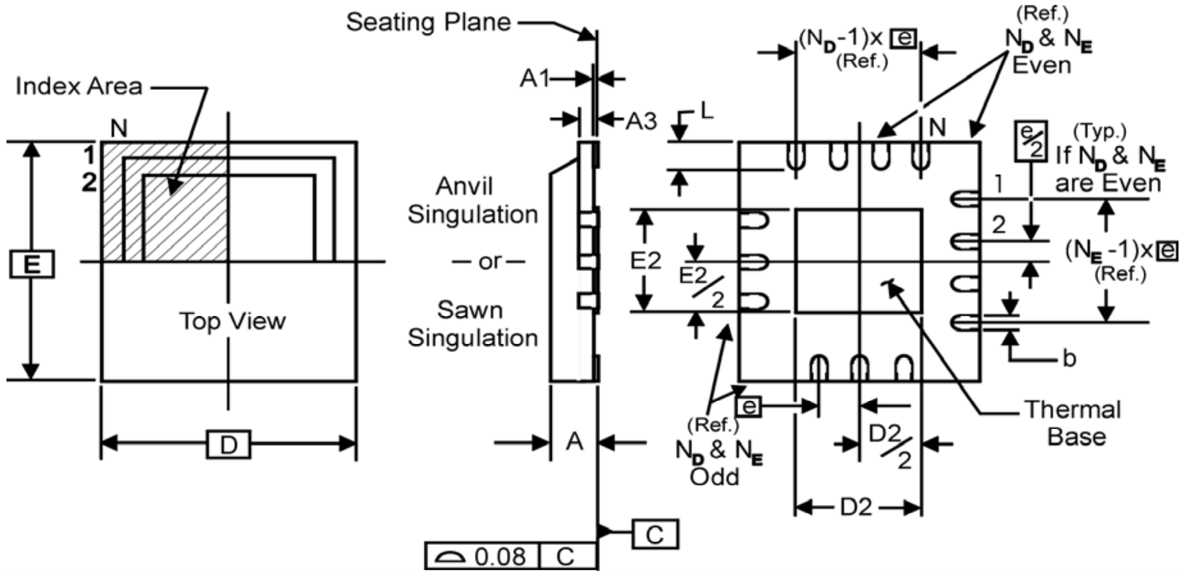
Table 7. θ_{JA} vs. Air Flow Table for 32 Lead VFQFN

θ_{JA} vs. Air Flow (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

Transistor Count

The transistor count for ICS8440258-46 is: 2589

Package Outline - K Suffix for 32 Lead VFQFN



NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 8 below.

Table 8. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	VHHD-2		
	MINIMUM	NOMINAL	MAXIMUM
N	32		
A	0.80	--	1.00
A1	0	--	0.05
A3	0.25 Ref.		
b	0.18	0.25	0.30
N_D			8
N_E			8
D	5.00 BASIC		
D2	1.25	2.25	3.25
E	5.00 BASIC		
E2	1.25	2.25	3.25
e	0.50 BASIC		
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS8440258AK-46	ICS40258A46	32 Lead VFQFN	Tray	0°C to 70°C
ICS8440258AK-46T	ICS40258A46	32 Lead VFQFN	1000 Tape & Reel	0°C to 70°C
ICS8440258AK-46LF	ICS0258A46L	32 Lead "Lead-Free" VFQFN	Tray	0°C to 70°C
ICS8440258AK-46LFT	ICS0258A46L	32 Lead "Lead-Free" VFQFN	1000 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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