FEMTOCLOCK™ CRYSTAL/LVCMOS-TO-LVDS/LVCMOS FREQUENCY SYNTHESIZER

ICS8440259-45

General Description

The ICS8440259-45 is a 9 output synthesizer optimized to generate Gigabit and 10 Gigabit Ethernet clocks and is a member of the HiPerClockS™family of high performance clock solutions from IDT. Using a 25MHz, 18pF parallel resonant crystal, the device will generate both 156.25MHz, 125MHz and 3.90625MHz clocks with mixed LVDS and LVCMOS/LVTTL output levels. The ICS8440259-45 uses IDT's 3rd generation low phase noise VCO technology and can achieve <1ps typical rms phase jitter, easily meeting Ethernet jitter requirements. The ICS8440259-45 is packaged in a small, 5mm x 5mm VFQFN package that is optimum for applications with space limitations.

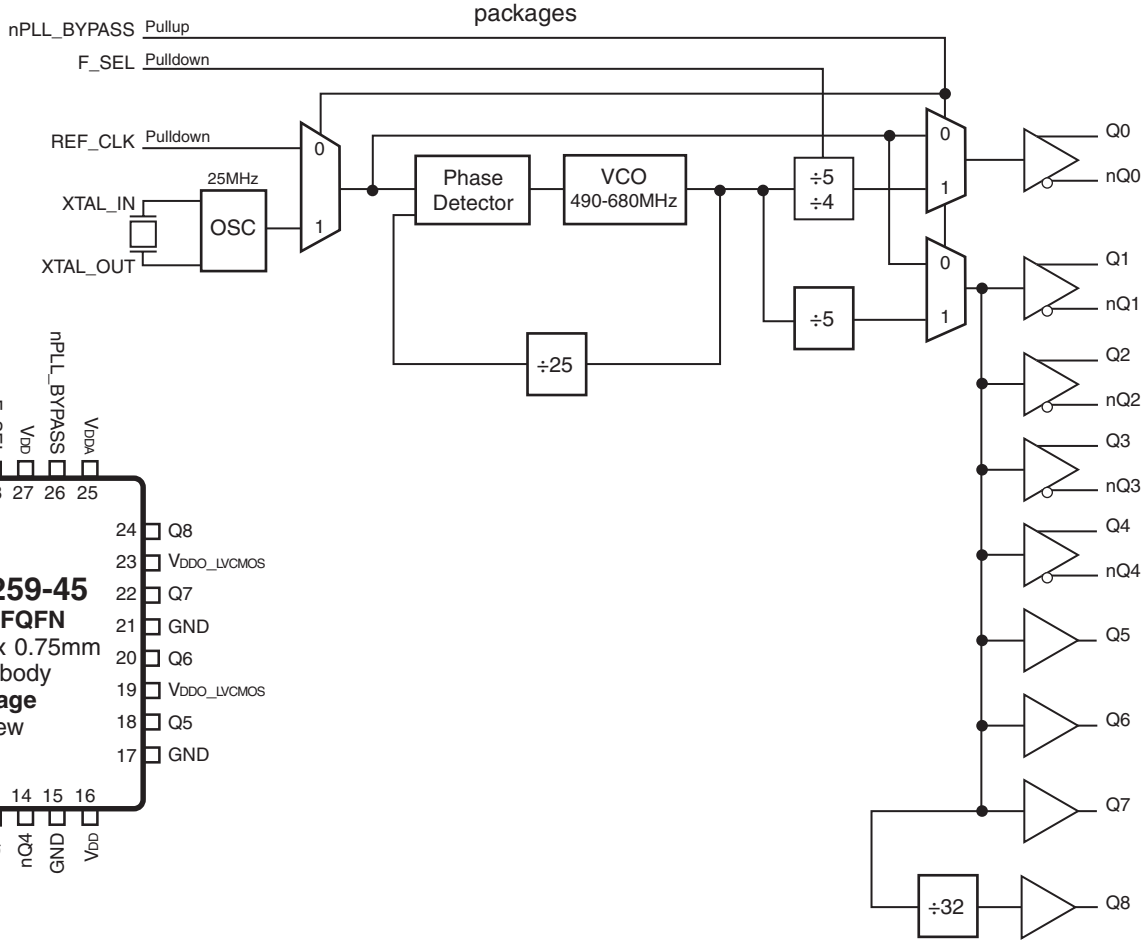
Features

- One differential LVDS output at 156.25MHz or 125MHz
  Four differential LVDS outputs at 125MHz
  Three LVCMOS/LVTTL single-ended outputs at 125MHz
  One LVCMOS/LVTTL single-ended output at 3.90625MHz
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input and PLL bypass from a single select pin
- VCO range: 490MHz - 680MHz
- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.42ps (typical)
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.45ps (typical)
- LVDS supply voltage modes: full 3.3V and full 2.5V
- LVCMOS supply voltage modes:

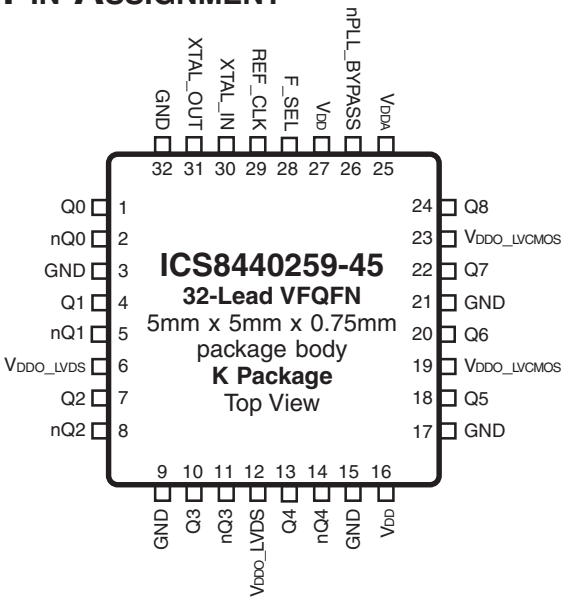
Core/Output	Core/Output	Core/Output
3.3V/3.3V	3.3V/2.5V	2.5V/2.5V

- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS6) packages

Block Diagram



Pin Assignment



The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential clock outputs. LVDS interface levels.
3, 9, 15, 17, 21, 32	GND	Power		Power supply ground.
4, 5	Q1, nQ1	Output		Differential clock outputs. LVDS interface levels.
6, 12	V_{DDO_LVDS}	Power		Output supply pins for Qx/nQx LVDS outputs.
7, 8	Q2, nQ2	Output		Differential clock outputs. LVDS interface levels.
10, 11	Q3, nQ3	Output		Differential clock outputs. LVDS interface levels.
13, 14	Q4, nQ4	Output		Differential clock outputs. LVDS interface levels.
16, 27	V_{DD}	Power		Core supply pins.
18, 20, 22, 24	Q5, Q6, Q7, Q8	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.
19, 23	V_{DDO_LVCMOS}	Power		Output supply pins for Q5:Q8 LVCMOS outputs.
25	V_{DDA}	Power		Analog supply pin.
26	nPLL_BYPASS	Input	Pullup	Input select and PLL bypass control pin. See Table 3B. LVCMOS/LVTTL interface levels.
28	F_SEL	Input	Pulldown	Frequency select pin. See Table 3A. LVCMOS/LVTTL interface levels.
29	REF_CLK	Input	Pulldown	Single-ended LVCMOS/LVTTL reference clock input.
30, 31	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_OUT is the output. XTAL_IN is the input.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4		pF
C_{PD}	Power Dissipation Capacitance		V_{DD}, V_{DDO_LVCMOS} = 3.465V		TBD		pF
			V_{DD}, V_{DDO_LVCMOS} = 2.625V		TBD		pF
			V_{DD} = 3.465, V_{DDO_LVCMOS} = 2.625V		TBD		pF
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{OUT}	Output Impedance	Q5:Q8			TBD		Ω

TABLE 3A. FREQUENCY SELECT FUNCTION TABLE

Input		Outputs
F_SEL	Output Divider	Q0/nQ0 Frequency
0	÷5	125MHz (default)
1	÷4	156.25MHz

TABLE 3B. PLL BYPASS AND INPUT SELECT FUNCTION TABLE

Inputs		
nPLL_BYPASS	PLL Bypass	Input Selected
0	PLL Bypassed	REF_CLK
1	PLL Enabled	XTAL_IN/XTAL_OUT (default)

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O (LVCMOS)	-0.5V to V_{DDO_LVCMOS} + 0.5V
Outputs, I_O (LVDS)	
Continuous Current	10mA
Surge Current	15mA
Operating Temperature Range, T_A	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA}	37°C/W (0 mps)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 3A. Power Supply DC Characteristics, $V_{DD} = V_{DDO\_LVCMOS} = V_{DDO\_LVDS}$ = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.10	3.3	V_{DD}	V
V_{DDO_LVCMOS}, V_{DDO_LVDS}	Output Supply Voltage		3.135	2.5	3.465	V
I_{DD}	Power Supply Current			108		mA
I_{DDA}	Analog Supply Current			10		mA
I_{DDO_LVCMOS}, I_{DDO_LVDS}	Power Supply Current			160		mA

Table 3B. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO_LVCMOS} = 2.5V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.10	3.3	V_{DD}	V
V_{DDO_LVCMOS}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			105		mA
I_{DDA}	Analog Supply Current			10		mA
I_{DDO_LVCMOS}	Power Supply Current			145		mA

Table 3C. Power Supply DC Characteristics, $V_{DD} = V_{DDO\_LVCMOS} = V_{DDO\_LVDS}$ = 2.5V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.10	2.5	V_{DD}	V
V_{DDO_LVCMOS}, V_{DDO_LVDS}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			72		mA
I_{DDA}	Analog Supply Current			10		mA
I_{DDO_LVCMOS}, I_{DDO_LVDS}	Power Supply Current			100		mA

TABLE 4D. LVCMOS/LVTTL DC CHARACTERISTICS, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
			V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	REF_CLK	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
		nPLL_BYPASS	V_{DD} = V_{IN} = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	REF_CLK	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
		nPLL_BYPASS	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1	Q5:Q8	V_{DDO_LVCMOS} = 3.3V±5%	2.1			V
		Q5:Q8	V_{DDO_LVCMOS} = 2.5V±5%	1.75			V
V_{OL}	Output Low Voltage; NOTE 1	Q5:Q8	V_{DDO_LVCMOS} = 3.3V or 2.5V±5%			0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO_LVCMOS}/2. See Parameter Measurement Information, Output Load Test Circuit diagram.

TABLE 4E. LVDS DC CHARACTERISTICS, V_{DD} = V_{DDO_LVDS} = 3.3V ± 5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		250	325	450	mV
ΔV_{OD}	V_{OD} Magnitude Change			25		mV
V_{OS}	Offset Voltage			1.35		V
ΔV_{OS}	V_{OS} Magnitude Change			25		mV

TABLE 4F. LVDS DC CHARACTERISTICS, V_{DD} = V_{DDO_LVDS} = 2.5V ± 5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		250	315	450	mV
ΔV_{OD}	V_{OD} Magnitude Change			25		mV
V_{OS}	Offset Voltage			1.25		V
ΔV_{OS}	V_{OS} Magnitude Change			25		mV

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6A. AC CHARACTERISTICS, $V_{DD} = V_{DDO\_LVCMOS} = V_{DDO\_LVDS} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	Q0/nQ0:Q4/nQ4			125		MHz
		Q5:Q7			125		MHz
		Q8			3.90625		MHz
		Q0/nQ0			156.25		MHz
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 1	Q0:4/nQ0:4	125MHz, (1.875MHz - 20MHz)		0.41		ps
		Q0/nQ0	156.25MHz, (1.875MHz - 20MHz)		0.45		ps
		Q5:Q7	125MHz, (1.875MHz - 20MHz)		0.45		ps
t_R / t_F	Output Rise/Fall Time	Q0/nQ0:Q4/nQ4	125MHz, 20% to 80%		375	550	ps
		Q0/nQ0	156.25MHz, 20% to 80%		335	550	ps
		Q5:Q7	125MHz, 20% to 80%		950	1.2	ps
		Q8 (NOTE 2)	3.90625MHz, 20% to 80%		1	20	ns
odc	Output Duty Cycle	Q0/nQ0:Q4/nQ4	125MHz	45	47	55	%
		Q0/nQ0	156.25MHz	45	50	55	%
		Q5:Q7	125MHz	45	46	55	%
		Q8	3.90625MHz	45	50	55	%
odc	Output Duty Cycle, BYPASS Mode	Q0/nQ0:Q4/nQ4	125MHz		TBD		%
		Q0/nQ0	156.25MHz		TBD		%
		Q5:Q7	125MHz		TBD		%
		Q8	3.90625MHz		TBD		%

NOTE 1: Please refer to the Phase Noise Plots.
NOTE 2: Output loaded with 15pF.

TABLE 6B. AC CHARACTERISTICS, $V_{DD} = V_{DDO\_LVCMOS} = V_{DDO\_LVDS} = 2.5V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	Q0/nQ0:Q4/nQ4			125		MHz
		Q5:Q7			125		MHz
		Q8			3.90625		MHz
		Q0/nQ0			156.25		MHz
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 1	Q0:4/nQ0:4	125MHz, (1.875MHz - 20MHz)		0.41		ps
		Q0/nQ0	156.25MHz, (1.875MHz - 20MHz)		0.43		ps
		Q5:Q7	125MHz, (1.875MHz - 20MHz)		0.44		ps
t_R / t_F	Output Rise/Fall Time	Q0/nQ0:Q4/nQ4	125MHz, 20% to 80%		350	550	ps
		Q0/nQ0	156.25MHz, 20% to 80%		335	550	ps
		Q5:Q7	125MHz, 20% to 80%		1.1	1.2	ns
		Q8 (NOTE 2)	3.90625MHz, 20% to 80%		1.5	20	ns
odc	Output Duty Cycle	Q0/nQ0:Q4/nQ4	125MHz	45	47	55	%
		Q0/nQ0	156.25MHz	45	50	55	%
		Q5:Q7	125MHz	45	47	55	%
		Q8	3.90625MHz	45	50	55	%
odc	Output Duty Cycle, BYPASS Mode	Q0/nQ0:Q4/nQ4	125MHz		50		%
		Q0/nQ0	156.25MHz		50		%
		Q5:Q7	125MHz		50		%
		Q8	3.90625MHz		50		%

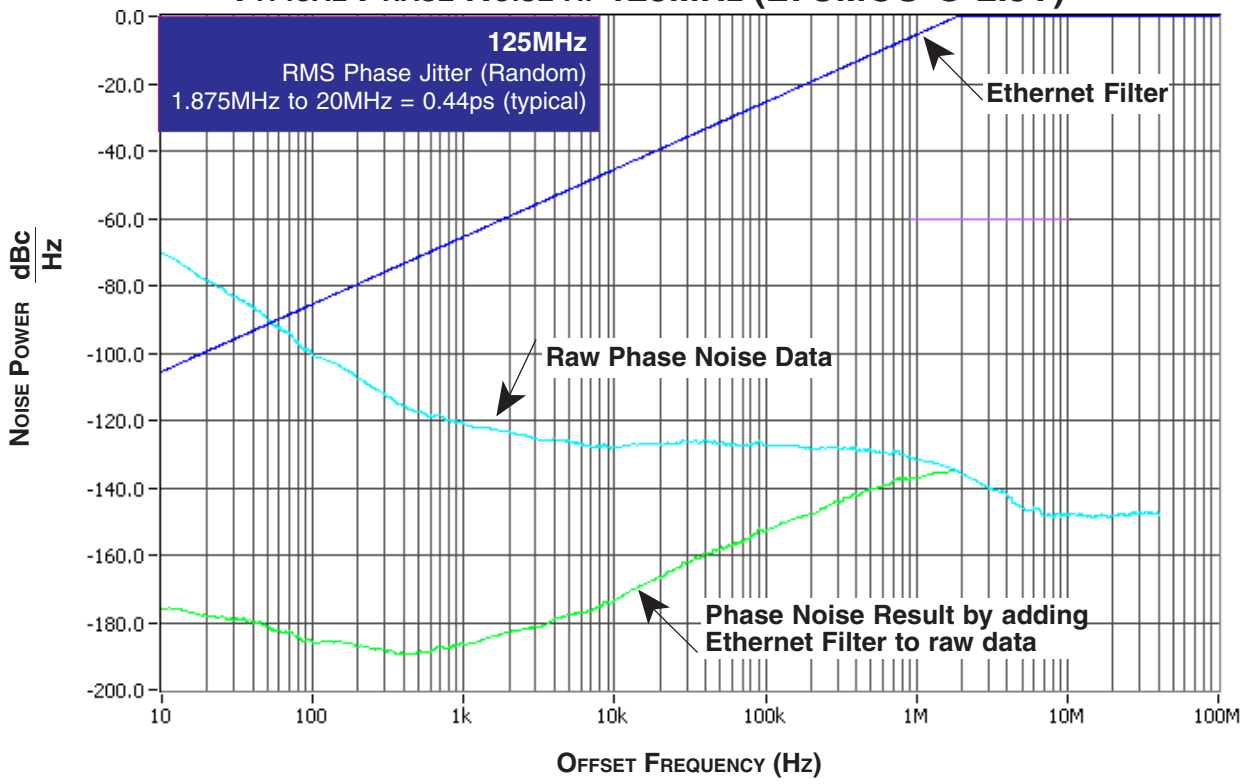
NOTE 1: Please refer to the Phase Noise Plots.
NOTE 2: Output loaded with 15pF.

TABLE 6C. AC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO\_LVCMOS} = 2.5V \pm 5\%$, $T_A = 0°C$ TO $70°C$

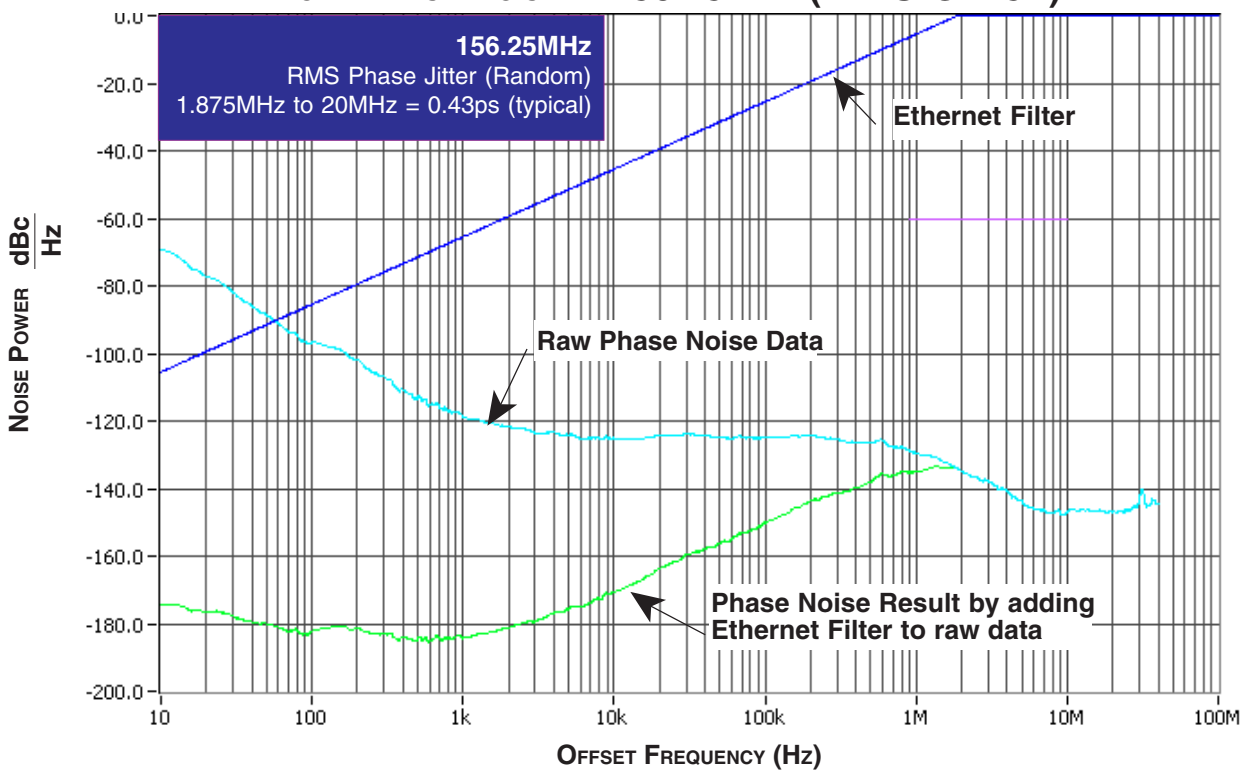
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	Q5:Q7			125		MHz
		Q8			3.90625		MHz
*t*jit(Ø)	RMS Phase Jitter (Random)	Q5:Q7	125MHz		TBD		ps
		Q8	3.90625MHz		TBD		ps
t_R / t_F	Output Rise/Fall Time	Q5:Q7	125MHz, 20% to 80%		1.1	1.2	ns
		Q8 (NOTE 1)	3.90625MHz, 20% to 80%		20		ns
odc	Output Duty Cycle	Q5:Q7	125MHz	45	47	55	%
		Q8	3.90625MHz	45	5	55	%
odc	Output Duty Cycle, BYPASS Mode	Q5:Q7	125MHz		50		%
		Q8	3.90625MHz		50		%

NOTE 1: Output loaded with 15pF.

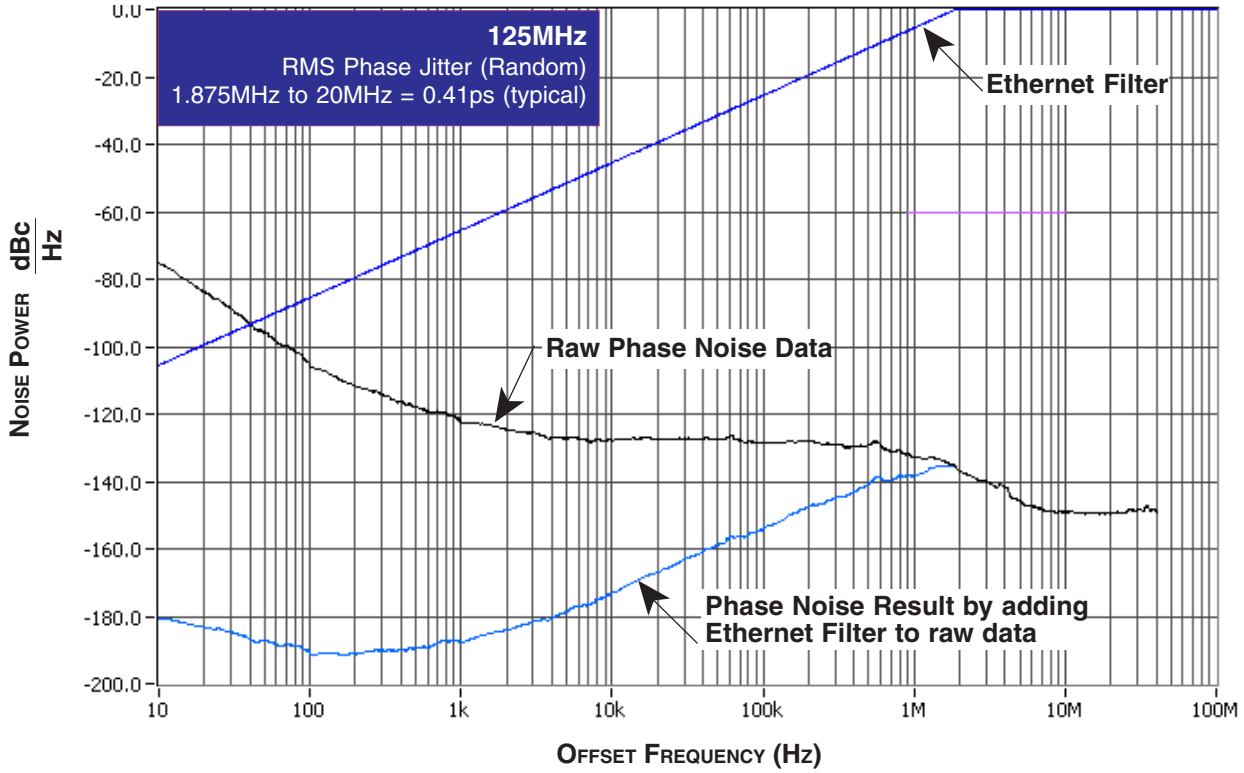
TYPICAL PHASE NOISE AT 125MHZ (LVCMOS @ 2.5V)



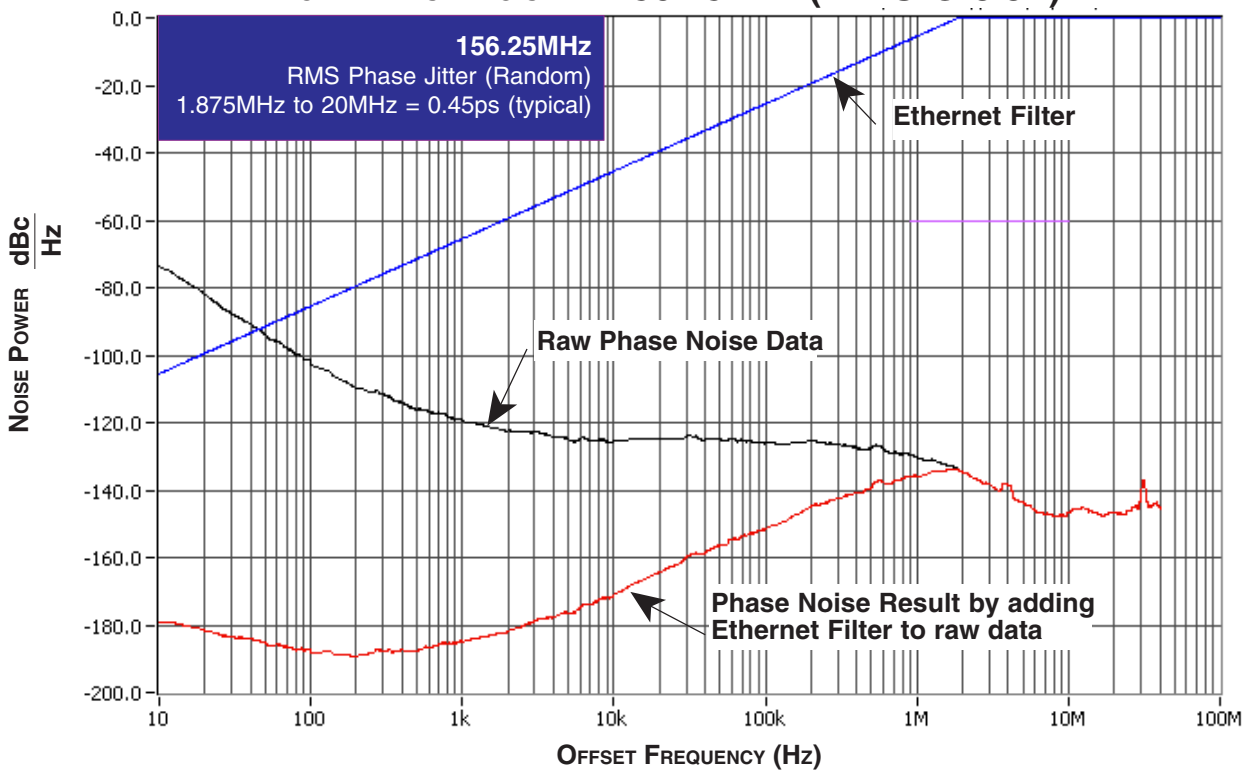
TYPICAL PHASE NOISE AT 156.25MHZ (LVDS @ 2.5V)



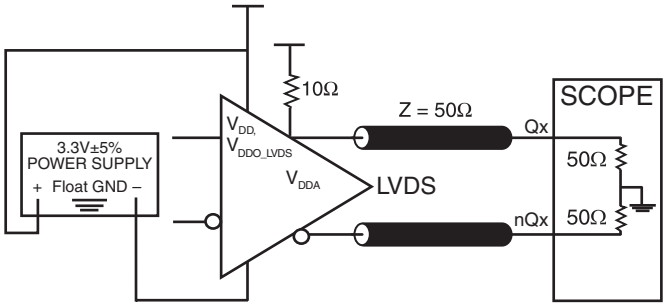
TYPICAL PHASE NOISE AT 125MHZ (LVDS @ 3.3V)



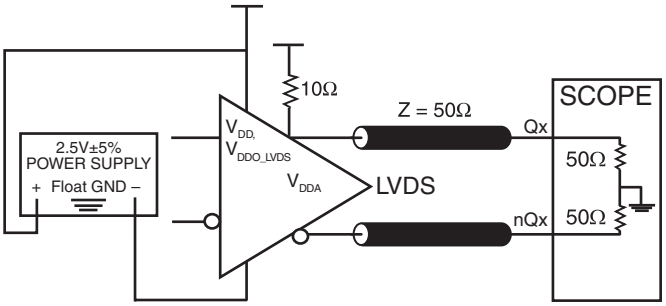
TYPICAL PHASE NOISE AT 156.25MHZ (LVDS @ 3.3V)



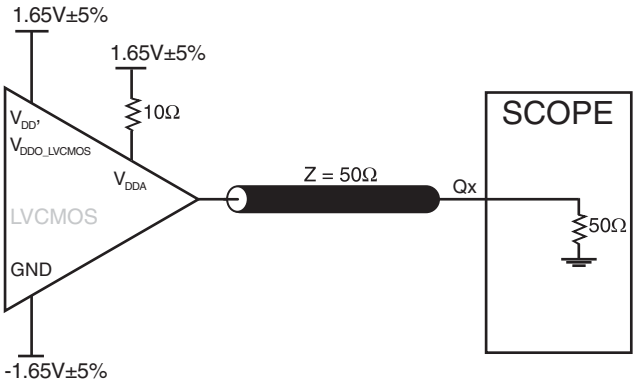
PARAMETER MEASUREMENT INFORMATION



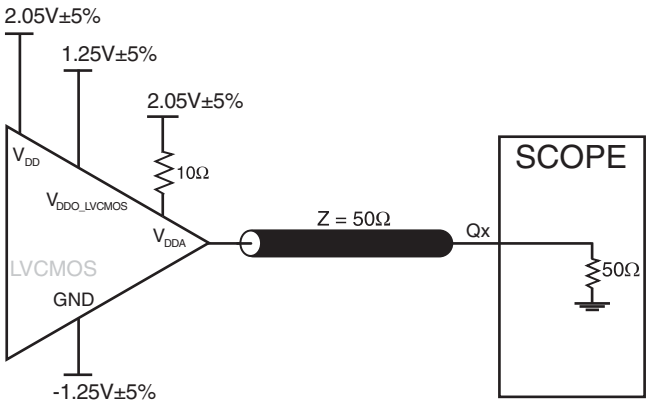
3.3V LVDS OUTPUT LOAD AC TEST CIRCUIT



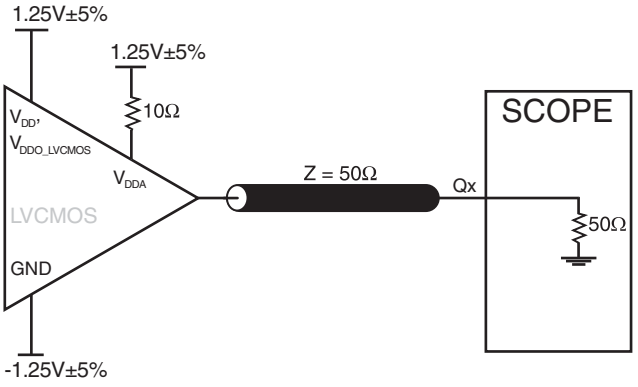
2.5V LVDS OUTPUT LOAD AC TEST CIRCUIT



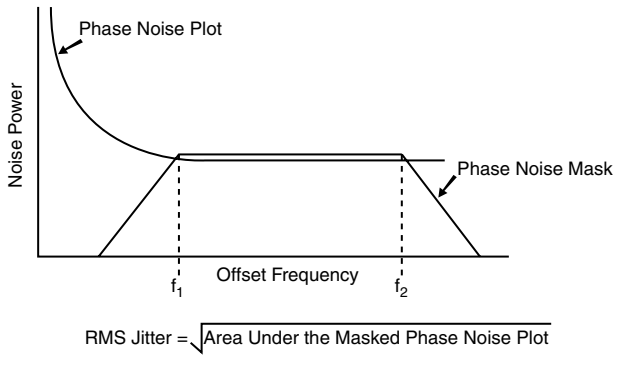
3.3V LVCMOS OUTPUT LOAD AC TEST CIRCUIT



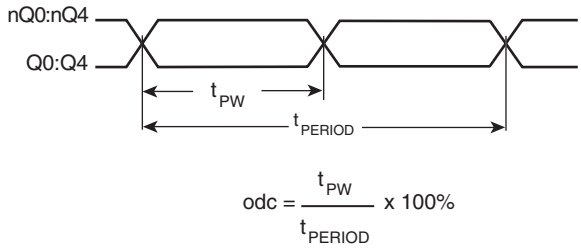
3.3V/2.5V LVCMOS OUTPUT LOAD AC TEST CIRCUIT



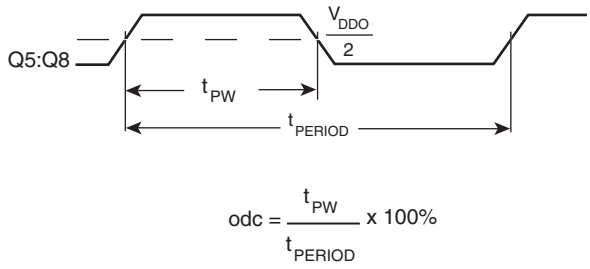
2.5V LVCMOS OUTPUT LOAD AC TEST CIRCUIT



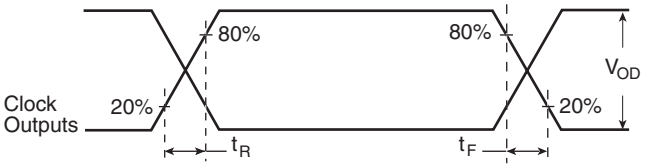
RMS PHASE JITTER



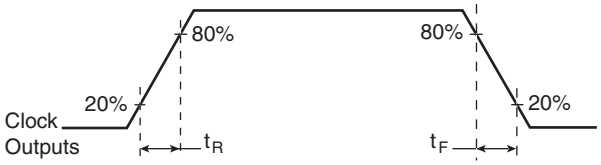
LVDS Output Duty Cycle/Pulse Width/Period



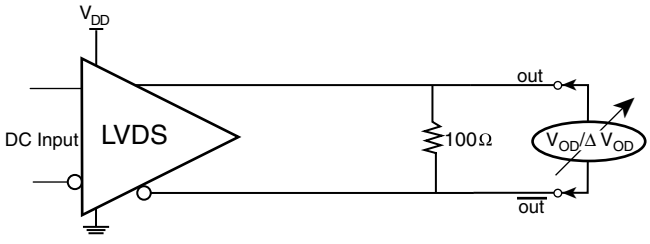
LVCMOS Output Duty Cycle/Pulse Width/Period



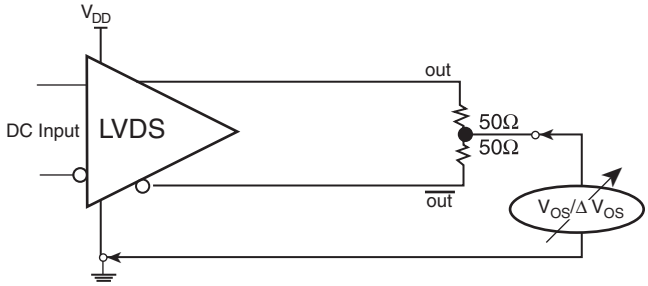
LVDS Output Rise/Fall Time



LVCMOS Output Rise/Fall Time



Differential Output Voltage Setup



Offset Voltage Setup

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS8440259-45 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, V_{DDO_LVDS} and V_{DDO_LVCMOS} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA}.

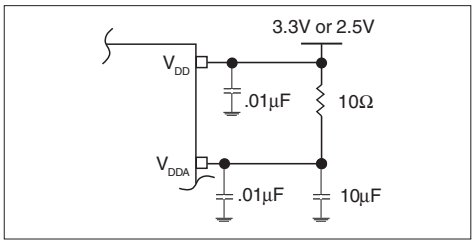


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS8440259-45 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

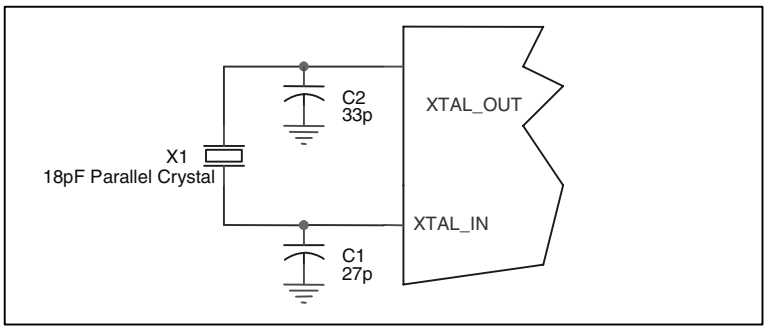


FIGURE 2. CRYSTAL INPUT INTERFACE

LVCMOS TO XTAL INTERFACE

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC couple capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

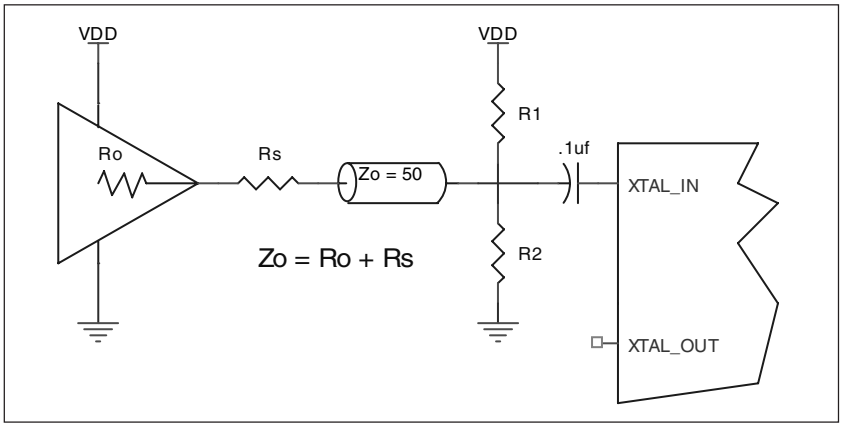


FIGURE 3. GENERAL DIAGRAM FOR LVCMOS DRIVER TO XTAL INPUT INTERFACE

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUT:
For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kW resistor can be tied from XTAL_IN to ground.

REF_CLK INPUT:
For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

LVCMOS CONTROL PINS:
All control pins have internal pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUT:
All unused LVCMOS output can be left floating. There should be no trace attached.

LVDS OUTPUT
All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

3.3V, 2.5V LVDS Driver Termination

A general LVDS interface is shown in *Figure 4.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

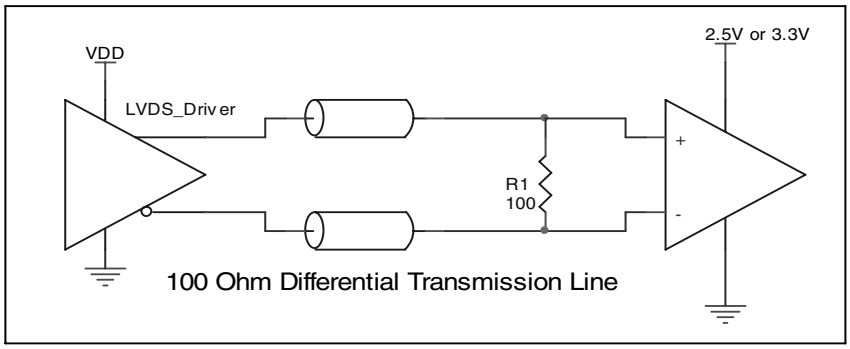


Figure 4. Typical LVDS Driver Termination

Thermal Release Path

The expose metal pad provides heat transfer from the device to the P.C. board. The expose metal pad is ground pad connected to ground plane through thermal via. The exposed pad on the device to the exposed metal pad on the PCB is contacted through solder as shown in *Figure 5.* For further information, please refer to the Application Note on Surface Mount Assembly of Amkor's Thermally /Electrically Enhance Leadframe Base Package, Amkor Technology.

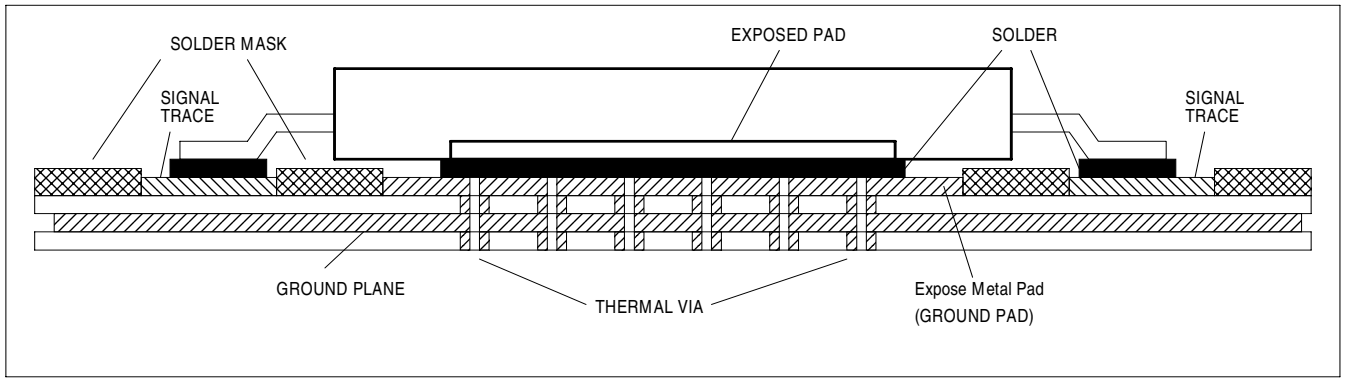


Figure 5. P.C. Board for Exposed Pad Thermal Release Path Example

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8440259-45. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS840259-45 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

Core and LVDS Output Power Dissipation

- Power (core, LVDS) = V_{DD_MAX} * (I_{DD} + I_{DDO} + I_{DDA}) = 3.465V * (108mA + 160mA + 10mA) = **963.27mW**

LVCMOS Output Power Dissipation

- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to V_{DDO}/2
  Output Current I_{OUT} = V_{DDO_MAX} / [2 * (50Ω + R_{OUT})] = 3.465V / [2 * (50Ω + 20Ω)] = **24.8mA**
- Power Dissipation on the R_{OUT} per LVCMOS output
  Power (R_{OUT}) = R_{OUT} * (I_{OUT})^2 = 20Ω * (24.8mA)^2 = **12.3mW per output**
- Total Power Dissipation on the R_{OUT}
  Total Power (R_{OUT}) = 12.3mW * 4 = **49.2mW**
- Dynamic Power Dissipation at 125MHz
  Power (125MHz) = C_{PD} * Frequency * (V_{DDO})^2 = 15pF * 125MHz * (3.465V)^2 = **22.5mW per output**
  Total Power (125MHz) = **22.5mW * 3 = 67.5mW**
- Dynamic Power Dissipation at 25MHz
  Power (25MHz) = C_{PD} * frequency * (V_{DDO})^2 = 15pF * 3.90625MHz * (3.465V)^2 = **0.7 mW per output**

Total Power Dissipation

- **Total Power**
  = Power (core, LVDS) + Total Power (R_{OUT}) + Total Power (125MHz) + Total Power (25MHz)
  = 963.3mW + 49.2mW + 67.5mW + 0.7mW
  = 1080.7mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming air flow of 1 meter per second and a multi-layer board, the appropriate value is 32.4°C/W per Table 7.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 1.085W * 32.4°C/W = 105.2°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 32-LEAD VFQFN, FORCED CONVECTION

θ_{JA} vs. Air Flow (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

RELIABILITY INFORMATION

TABLE 8. θ_{JA} VS. AIR FLOW TABLE FOR 32 LEAD VFQFN

θ_{JA} vs. Air Flow (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

TRANSISTOR COUNT

The transistor count for ICS8440259-45 is: 2975

PACKAGE OUTLINE - K SUFFIX FOR 32 LEAD VFQFN

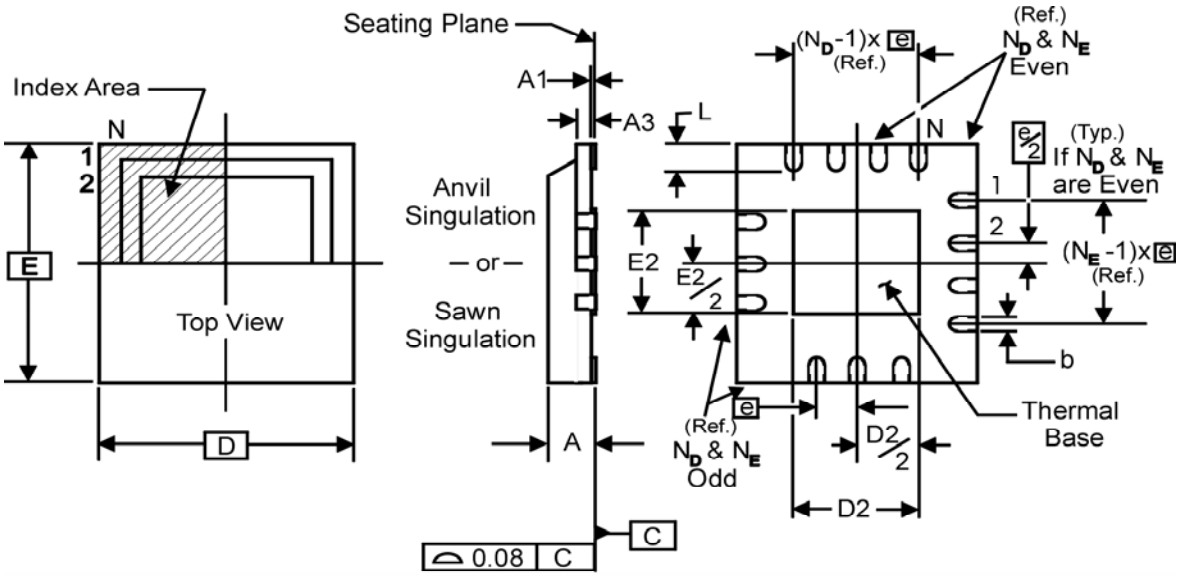


TABLE 9. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	VHHD-2		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	0.80	--	1.00
A1	0	--	0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D			8
N_E			8
D		5.00 BASIC	
D2	1.25	2.25	3.25
E		5.00 BASIC	
E2	1.25	2.25	3.25
e		0.50 BASIC	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8440259AK-45	ICS40259A45	32 Lead VFQFN	Tray	0°C to 70°C
8440259AK-45T	ICS40259A45	32 Lead VFQFN	1000 Tape & Reel	0°C to 70°C
8440259AK-45LF	ICS0259A45L	32 Lead "Lead-Free" VFQFN	Tray	0°C to 70°C
8440259AK-45LFT	ICS0259A45L	32 Lead "Lead-Free" VFQFN	1000 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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