

13-Bit Differential Input, Low Power A/D Converter with SPI™ Serial Interface

Features

- Full Differential Inputs
- ± 1 LSB max DNL
- ± 1 LSB max INL (MCP3301-B)
- ± 2 LSB max INL (MCP3301-C)
- Single supply operation: 2.7V to 5.5V
- 100 ksp/s sampling rate with 5V supply voltage
- 50 ksp/s sampling rate with 2.7V supply voltage
- 50 nA typical standby current, 1 μ A max
- 450 μ A max active current at 5V
- Industrial temp range: -40°C to $+85^{\circ}\text{C}$
- 8-pin MSOP, PDIP, and SOIC packages
- MXDEV™ Evaluation kit available

Applications

- Remote Sensors
- Battery Operated Systems
- Transducer Interface

Description

The Microchip Technology Inc. MCP3301 13-bit A/D converter features full differential inputs and low power consumption in a small package that is ideal for battery powered systems and remote data acquisition applications.

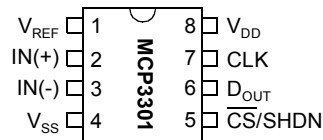
Incorporating a successive approximation architecture with on-board sample and hold circuitry, this 13-bit A/D converter is specified to have ± 1 LSB Differential Non-linearity (DNL), and ± 1 LSB Integral Nonlinearity (INL) for B-grade and ± 2 LSB for C-grade devices. The industry-standard SPI™ serial interface enables 13-bit A/D converter capability to be added to any PICmicro® microcontroller.

The MCP3301 features low current design that permits operation with typical standby and active currents of only 50 nA and 300 μ A, respectively. The device operates over a broad voltage range of 2.7V to 5.5V and is capable of conversion rates of up to 100 ksp/s. The reference voltage can be varied from 400 mV to 5V, yielding input-referred resolution between 98 μ V and 1.22 mV.

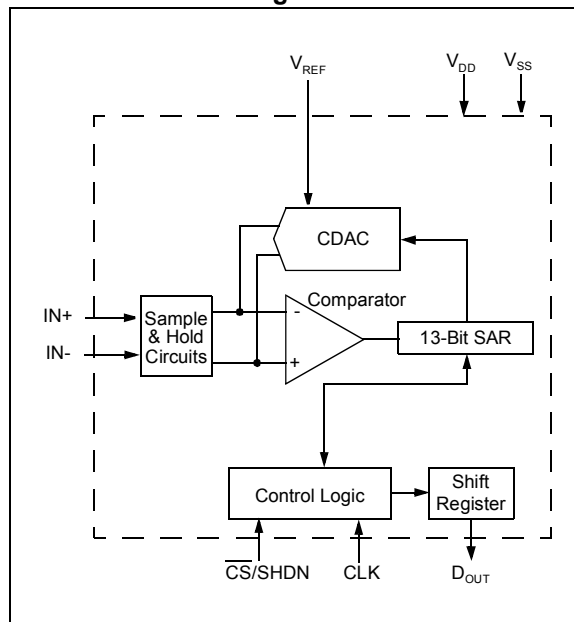
The MCP3301 is available in 8-pin PDIP, 150 mil SOIC, and MSOP packages. The full differential inputs of this device enable a wide variety of signals to be used in applications such as remote data acquisition, portable instrumentation, and battery operated applications.

Package Types

MSOP, PDIP, SOIC



Functional Block Diagram



MCP3301

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

V_{DD} 7.0V
 All inputs and outputs w.r.t. V_{SS} -0.3V to V_{DD} +0.3V
 Storage temperature -65°C to +150°C
 Ambient temp. with power applied -65°C to +125°C
 Maximum Junction Temperature 150°C
 ESD protection on all pins (HBM) > 4 kV

***Notice:** Stresses above those listed under “Maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
V_{REF}	Reference Voltage Input
IN(+)	Positive Analog Input
IN(-)	Negative Analog Input
V_{SS}	Ground
CS/SHDN	Chip Select / Shutdown Input
D_{OUT}	Serial Data Out
CLK	Serial Clock
V_{DD}	+2.7V to 5.5V Power Supply

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, all parameters apply at $V_{DD} = 5V$, $V_{SS} = 0V$, and $V_{REF} = 5V$. Full differential input configuration (Figure 3-4) with fixed common mode voltage of 2.5V. All parameters apply over temperature with $T_{AMB} = -40^{\circ}C$ to +85°C (**Note 7**). Conversion speed (f_{SAMPLE}) is 100 ksp/s with $f_{CLK} = 17 * f_{SAMPLE}$

Parameter	Sym	Min	Typ	Max	Units	Conditions
Conversion Rate:						
Maximum Sampling Frequency	f_{SAMPLE}	—	—	100 50	ksp/s ksp/s	$V_{DD} = V_{REF} = 2.7V, V_{CM} = 1.35V$
Conversion Time	t_{CONV}	13			CLK periods	
Acquisition Time	t_{ACQ}	1.5			CLK periods	
DC Accuracy:						
Resolution		12 data bits + sign			bits	
Integral Nonlinearity	INL	—	±0.5 ±1	±1 ±2	LSB	MCP3301-B MCP3301-C
Differential Nonlinearity	DNL	—	±0.5	±1	LSB	Monotonic with no missing codes over temperature
Positive Gain Error		-3	-0.75	+2	LSB	
Negative Gain Error		-3	-0.5	+2	LSB	
Offset Error		-3	+3	+6	LSB	
Dynamic Performance:						
Total Harmonic Distortion	THD	—	-91	—	dB	Note 3
Signal to Noise and Distortion	SINAD	—	78	—	dB	Note 3
Spurious Free Dynamic Range	SFDR	—	92	—	dB	Note 3
Common-Mode Rejection	CMRR	—	79	—	dB	Note 6
Power Supply Rejection	PSR	—	74	—	dB	Note 4

Note 1: This specification is established by characterization and not 100% tested.

2: See characterization graphs that relate converter performance to V_{REF} level.

3: $V_{IN} = 0.1V$ to $4.9V$ @ 1 kHz.

4: $V_{DD} = 5VDC \pm 500 mV_{p-p}$ @ 1 kHz, see test circuit Figure 3-3.

5: Maximum clock frequency specification must be met.

6: $V_{REF} = 400 mV$, $V_{IN} = 0.1V$ to $4.9V$ @ 1 kHz

7: MSOP devices are only specified at 25°C and +85°C.

Unless otherwise noted, all parameters apply at $V_{DD} = 5V$, $V_{SS} = 0V$, and $V_{REF} = 5V$. Full differential input configuration (Figure 3-4) with fixed common mode voltage of 2.5V. All parameters apply over temperature with $T_{AMB} = -40^{\circ}C$ to $+85^{\circ}C$ (**Note 7**). Conversion speed (f_{SAMPLE}) is 100 kbps with $f_{CLK} = 17 * f_{SAMPLE}$

Parameter	Sym	Min	Typ	Max	Units	Conditions
Reference Input:						
Voltage Range		0.4	—	V_{DD}	V	Note 2
Current Drain		—	100 0.001	150 3	μA μA	$\overline{CS} = V_{DD} = 5V$
Analog Inputs:						
Full-Scale Input Span	IN(+)-IN(-)	$-V_{REF}$	—	V_{REF}	V	
Absolute Input Voltage	IN(+)	-0.3	—	$V_{DD} + 0.3$	V	
	IN(-)	-0.3	—	$V_{DD} + 0.3$	V	
Leakage Current		—	0.001	± 1	μA	
Switch Resistance	R_S	—	1	—	k Ω	See Figure 6-2
Sample Capacitor	C_{SAMPLE}	—	25	—	pF	See Figure 6-2
Digital Input/Output:						
Data Coding Format		Binary Two's Complement				
High Level Input Voltage	V_{IH}	$0.7 V_{DD}$	—	—	V	
Low Level Input Voltage	V_{IL}	—	—	$0.3 V_{DD}$	V	
High Level Output Voltage	V_{OH}	4.1	—	—	V	$I_{OH} = -1 mA, V_{DD} = 4.5V$
Low Level Output Voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 1 mA, V_{DD} = 4.5V$
Input Leakage Current	I_{LI}	-10	—	10	μA	$V_{IN} = V_{SS}$ or V_{DD}
Output Leakage Current	I_{LO}	-10	—	10	μA	$V_{OUT} = V_{SS}$ or V_{DD}
Pin Capacitance	C_{IN}, C_{OUT}	—	—	10	pF	$T_{AMB} = 25^{\circ}C, f = 1 MHz, \mathbf{Note 1}$
Timing Specifications:						
Clock Frequency	f_{CLK}	—	—	1.7 0.85	MHz MHz	$V_{DD} = 5V, f_{SAMPLE} = 100 kbps$ $V_{DD} = 2.7V, f_{SAMPLE} = 50 kbps$
Clock High Time	t_{HI}	275	—	—	ns	Note 5
Clock Low Time	t_{LO}	275	—	—	ns	Note 5
CS Fall To First Rising CLK Edge	t_{SUCS}	100	—	—	ns	
CLK Fall To Output Data Valid	t_{DO}	—	—	125 200	ns ns	$V_{DD} = 5V$, see Figure 3-1 $V_{DD} = 2.7V$, see Figure 3-1
CLK Fall To Output Enable	t_{EN}	—	—	125 200	ns ns	$V_{DD} = 5V$, see Figure 3-1 $V_{DD} = 2.7V$, see Figure 3-1
CS Rise To Output Disable	t_{DIS}	—	—	100	ns	See test circuits, Figure 3-1 (Note 1)
CS Disable Time	t_{CSH}	580	—	—	ns	
D_{OUT} Rise Time	t_R	—	—	100	ns	See test circuits, Figure 3-1 (Note 1)
D_{OUT} Fall Time	t_F	—	—	100	ns	See test circuits, Figure 3-1 (Note 1)

Note 1: This specification is established by characterization and not 100% tested.

2: See characterization graphs that relate converter performance to V_{REF} level.

3: $V_{IN} = 0.1V$ to $4.9V @ 1 kHz$.

4: $V_{DD} = 5VDC \pm 500 mV_{P-P} @ 1 kHz$, see test circuit Figure 3-3.

5: Maximum clock frequency specification must be met.

6: $V_{REF} = 400 mV, V_{IN} = 0.1V$ to $4.9V @ 1 kHz$

7: MSOP devices are only specified at $25^{\circ}C$ and $+85^{\circ}C$.

MCP3301

Unless otherwise noted, all parameters apply at $V_{DD} = 5V$, $V_{SS} = 0V$, and $V_{REF} = 5V$. Full differential input configuration (Figure 3-4) with fixed common mode voltage of 2.5V. All parameters apply over temperature with $T_{AMB} = -40^{\circ}C$ to $+85^{\circ}C$ (**Note 7**). Conversion speed (f_{SAMPLE}) is 100 kpsps with $f_{CLK} = 17 * f_{SAMPLE}$

Parameter	Sym	Min	Typ	Max	Units	Conditions
Power Requirements:						
Operating Voltage	V_{DD}	2.7	—	5.5	V	
Operating Current	I_{DD}	—	300	450	μA	$V_{DD}, V_{REF} = 5V, D_{OUT}$ unloaded $V_{DD}, V_{REF} = 2.7V, D_{OUT}$ unloaded
Standby Current	I_{DDS}	—	0.05	1	μA	$\overline{CS} = V_{DD} = 5.0V$
Temperature Ranges:						
Specified Temperature Range	T_A	-40	—	+85	$^{\circ}C$	
Operating Temperature Range	T_A	-40	—	+85	$^{\circ}C$	
Storage Temperature Range	T_A	-65	—	+150	$^{\circ}C$	
Thermal Package Resistance:						
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	$^{\circ}C/W$	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	$^{\circ}C/W$	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	$^{\circ}C/W$	

Note 1: This specification is established by characterization and not 100% tested.

2: See characterization graphs that relate converter performance to V_{REF} level.

3: $V_{IN} = 0.1V$ to $4.9V @ 1 kHz$.

4: $V_{DD} = 5VDC \pm 500 mV_{p-p} @ 1 kHz$, see test circuit Figure 3-3.

5: Maximum clock frequency specification must be met.

6: $V_{REF} = 400 mV, V_{IN} = 0.1V$ to $4.9V @ 1 kHz$

7: MSOP devices are only specified at $25^{\circ}C$ and $+85^{\circ}C$.

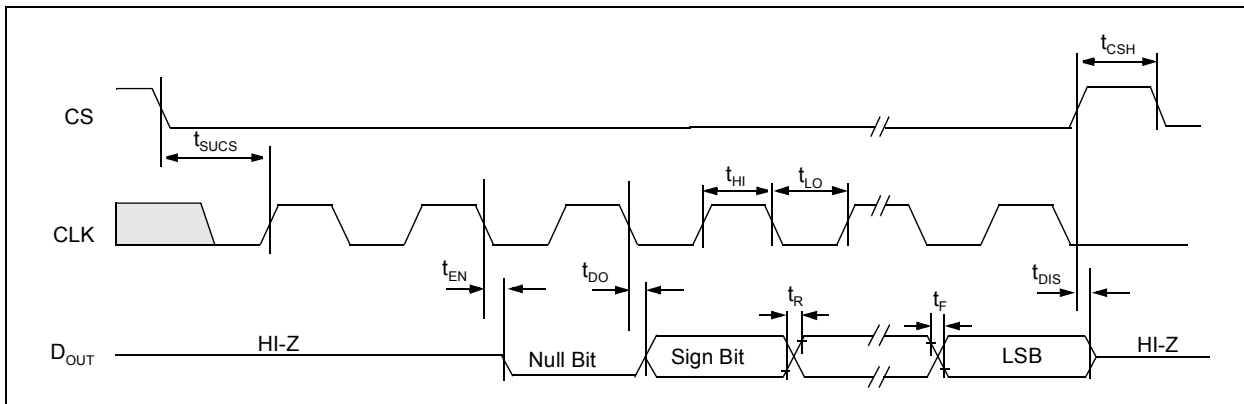


FIGURE 1-1: Timing Parameters.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, Full differential input configuration, $V_{SS} = 0V$, $f_{SAMPLE} = 100$ kps, $f_{CLK} = 17 * f_{SAMPLE}$, $T_A = 25^{\circ}C$.

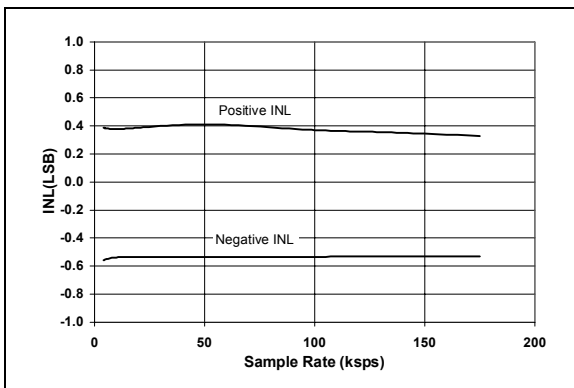


FIGURE 2-1: Integral Nonlinearity (INL) vs. Sample Rate.

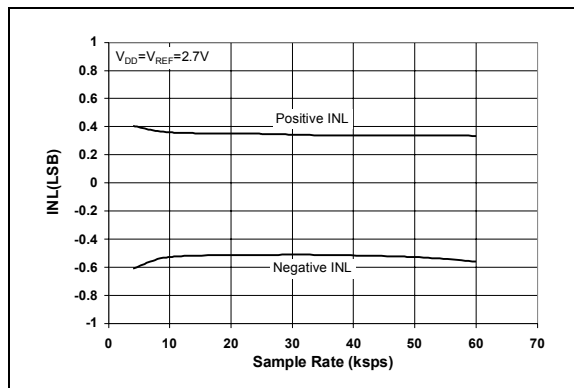


FIGURE 2-4: Integral Nonlinearity (INL) vs. Sample Rate ($V_{DD} = 2.7V$).

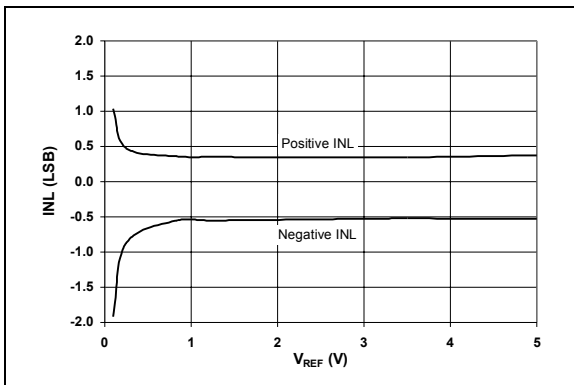


FIGURE 2-2: Integral Nonlinearity (INL) vs. V_{REF} .

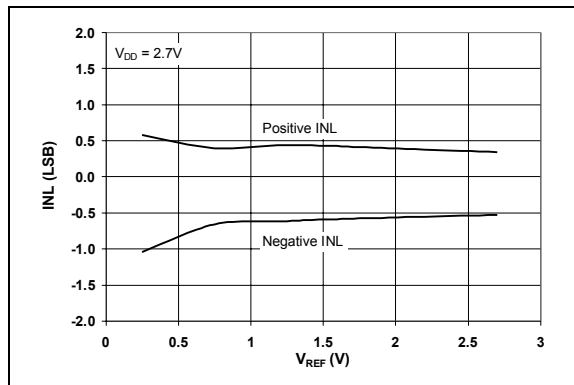


FIGURE 2-5: Integral Nonlinearity (INL) vs. V_{REF} ($V_{DD} = 2.7V$).

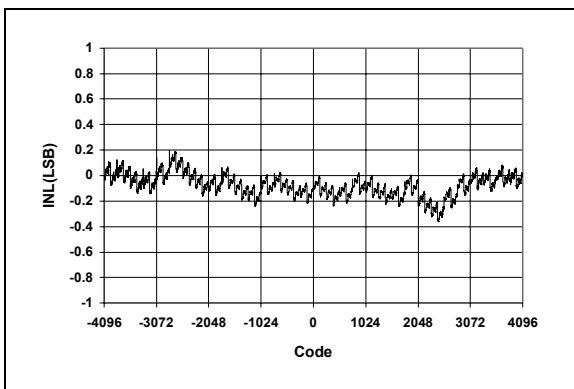


FIGURE 2-3: Integral Nonlinearity (INL) vs. Code (Representative Part).

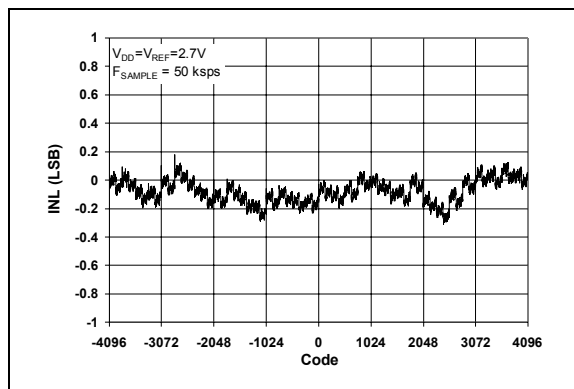


FIGURE 2-6: Integral Nonlinearity (INL) vs. Code (Representative Part, $V_{DD} = 2.7V$).

MCP3301

Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, Full differential input configuration, $V_{SS} = 0V$, $f_{SAMPLE} = 100$ kpsps, $f_{CLK} = 17 * f_{SAMPLE}$, $T_A = 25^{\circ}C$.

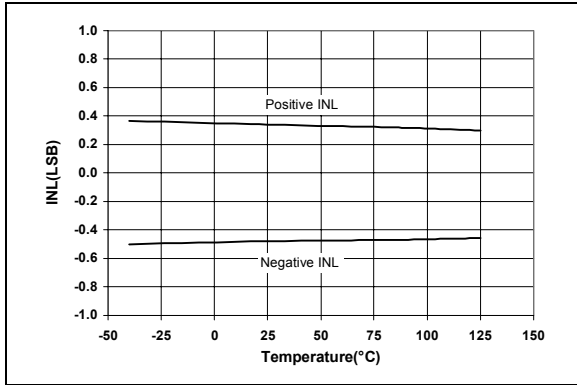


FIGURE 2-7: Integral Nonlinearity (INL) vs. Temperature.

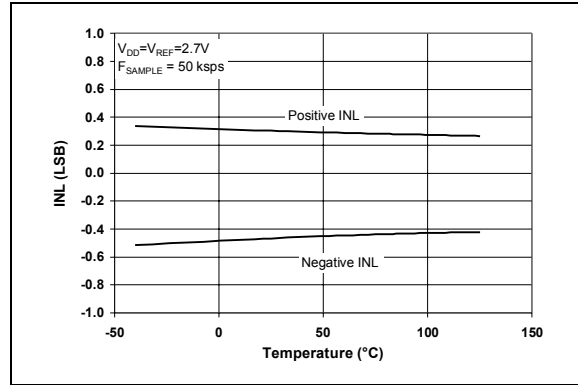


FIGURE 2-10: Integral Nonlinearity (INL) vs. Temperature ($V_{DD} = 2.7V$).

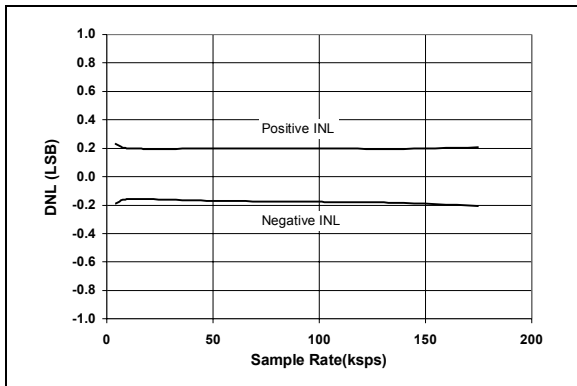


FIGURE 2-8: Differential Nonlinearity (DNL) vs. Sample Rate.

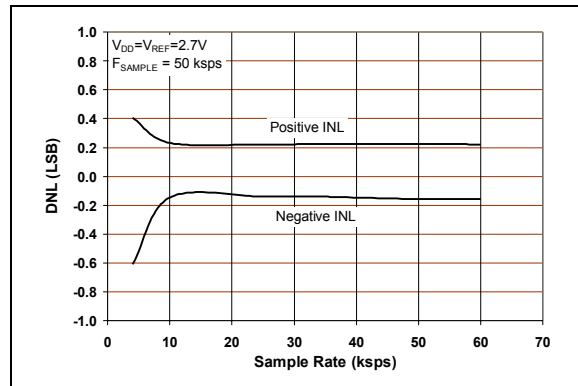


FIGURE 2-11: Differential Nonlinearity (DNL) vs. Sample Rate ($V_{DD} = 2.7V$).

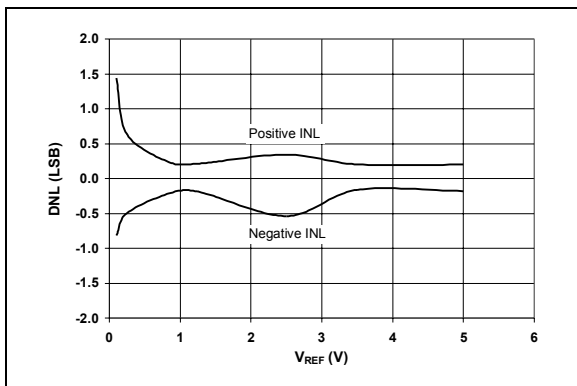


FIGURE 2-9: Differential Nonlinearity (DNL) vs. V_{REF} .

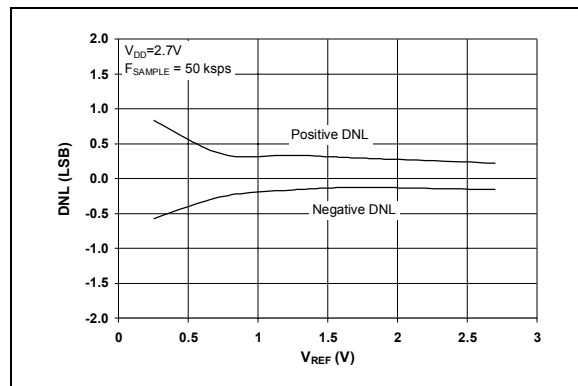


FIGURE 2-12: Differential Nonlinearity (DNL) vs. V_{REF} ($V_{DD} = 2.7V$).

Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, Full differential input configuration, $V_{SS} = 0V$, $f_{SAMPLE} = 100$ kps, $f_{CLK} = 17 \cdot f_{SAMPLE}$, $T_A = 25^\circ C$.

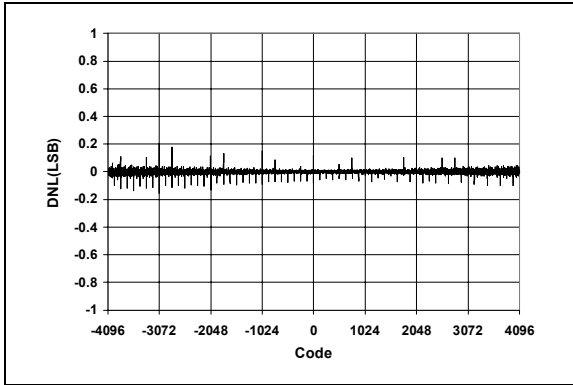


FIGURE 2-13: Differential Nonlinearity (DNL) vs. Code (Representative Part).

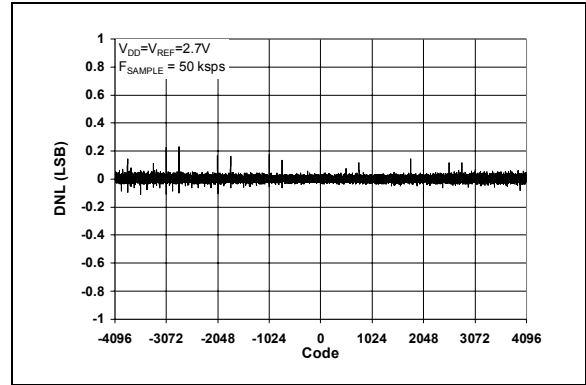


FIGURE 2-16: Differential Nonlinearity (DNL) vs. Code (Representative Part, $V_{DD} = 2.7V$).

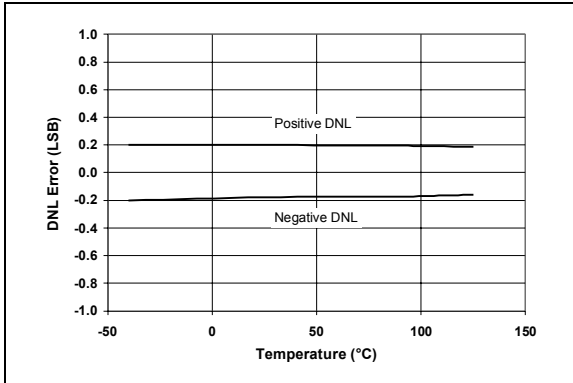


FIGURE 2-14: Differential Nonlinearity (DNL) vs. Temperature.

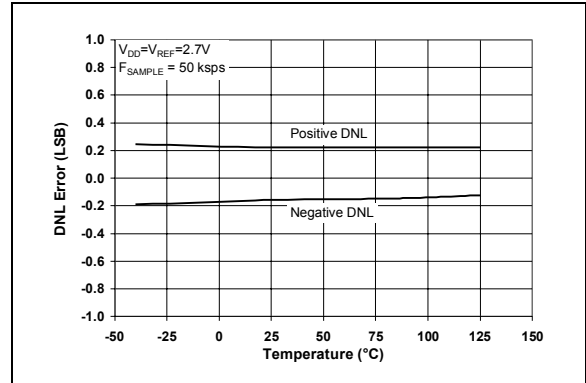


FIGURE 2-17: Differential Nonlinearity (DNL) vs. Temperature ($V_{DD} = 2.7V$).

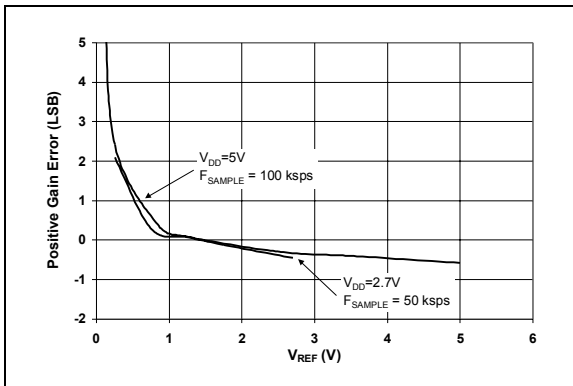


FIGURE 2-15: Positive Gain Error vs. V_{REF} .

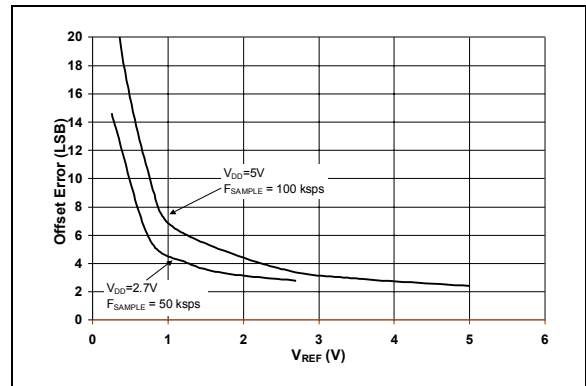


FIGURE 2-18: Offset Error vs. V_{REF} .

MCP3301

Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, Full differential input configuration, $V_{SS} = 0V$, $f_{SAMPLE} = 100$ kpsps, $f_{CLK} = 17 * f_{SAMPLE}$, $T_A = 25^{\circ}C$.

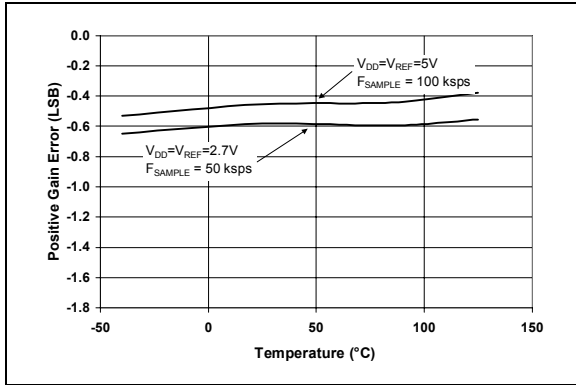


FIGURE 2-19: Positive Gain Error vs. Temperature.

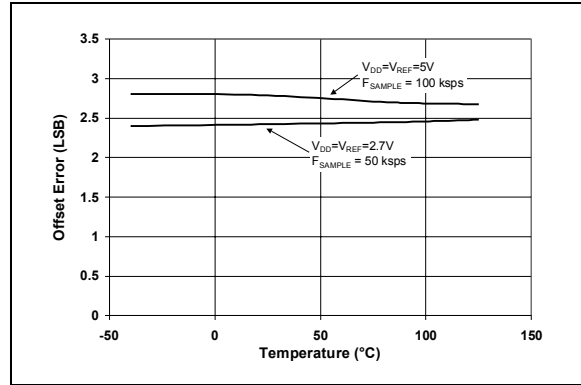


FIGURE 2-22: Offset Error vs. Temperature.

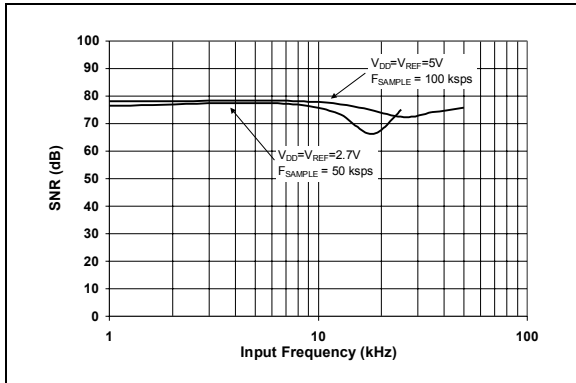


FIGURE 2-20: Signal to Noise Ratio (SNR) vs. Input Frequency.

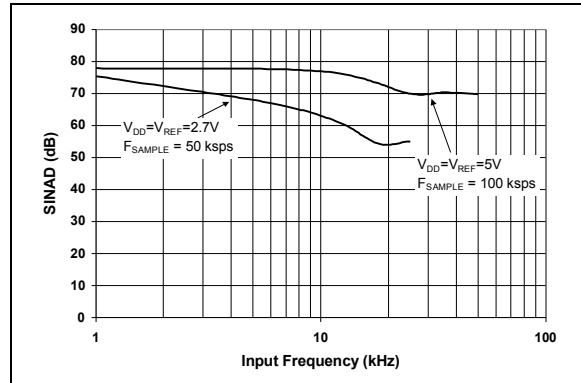


FIGURE 2-23: Signal to Noise and Distortion (SINAD) vs. Input Frequency.

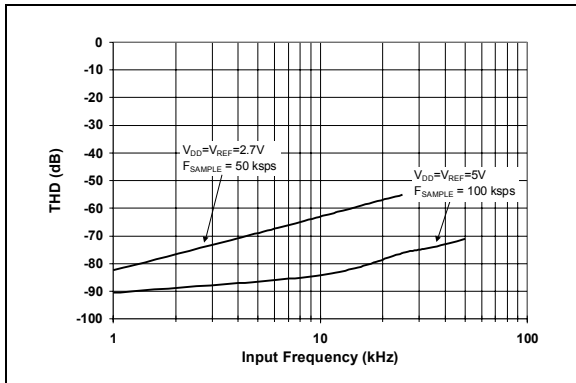


FIGURE 2-21: Total Harmonic Distortion (THD) vs. Input Frequency.

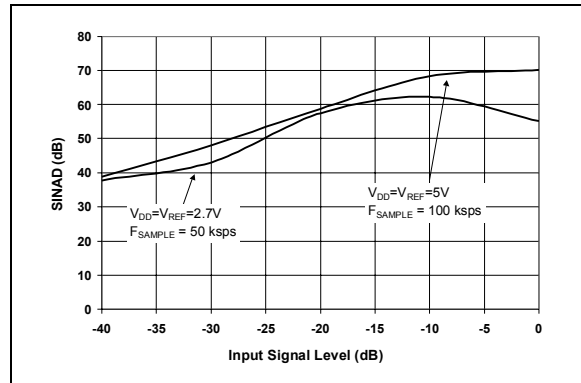


FIGURE 2-24: Signal to Noise and Distortion (SINAD) vs. Input Signal Level.

Note: Unless otherwise indicated, $V_{DD} = 5V$, Full differential input configuration, $V_{SS} = 0V$, $f_{SAMPLE} = 100$ ksp/s, $f_{CLK} = 17 \cdot f_{SAMPLE}$, $T_A = 25^\circ C$.

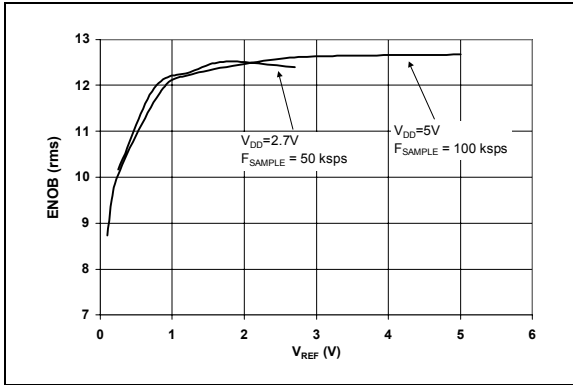


FIGURE 2-25: Effective Number of Bits (ENOB) vs. V_{REF} .

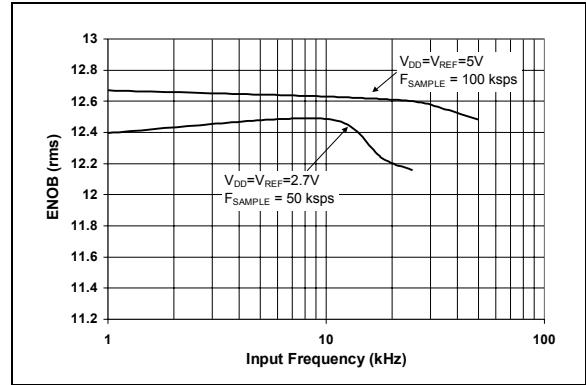


FIGURE 2-28: Effective Number of Bits (ENOB) vs. Input Frequency.

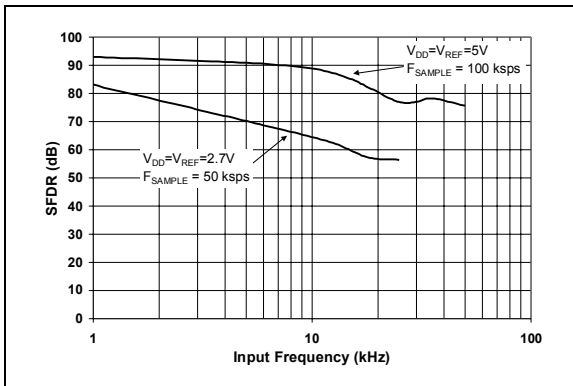


FIGURE 2-26: Spurious Free Dynamic Range (SFDR) vs. Input Frequency.

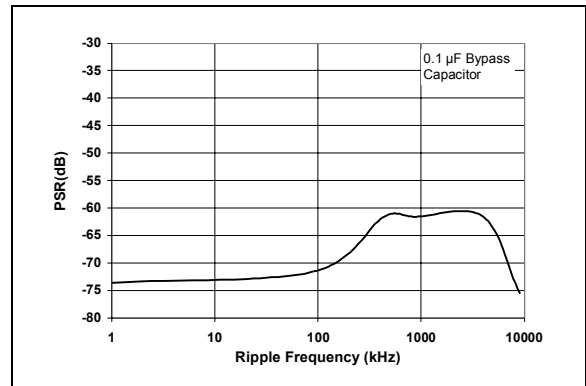


FIGURE 2-29: Power Supply Rejection (PSR) vs. Ripple Frequency.

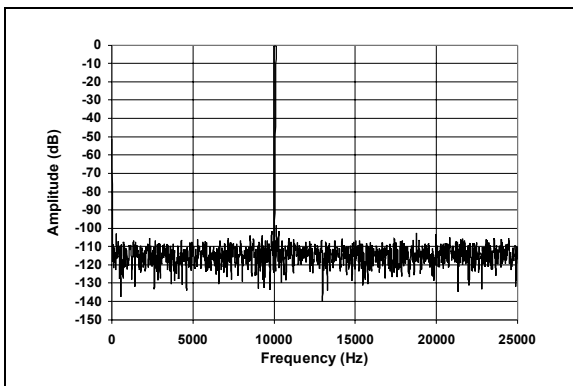


FIGURE 2-27: Frequency Spectrum of 10 kHz Input (Representative Part).

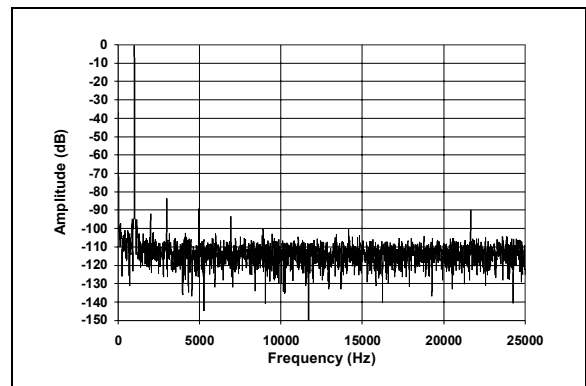


FIGURE 2-30: Frequency Spectrum of 1 kHz Input (Representative Part, $V_{DD} = 2.7V$).

MCP3301

Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, Full differential input configuration, $V_{SS} = 0V$, $f_{SAMPLE} = 100$ kpsps, $f_{CLK} = 17 * f_{SAMPLE}$, $T_A = 25^{\circ}C$.

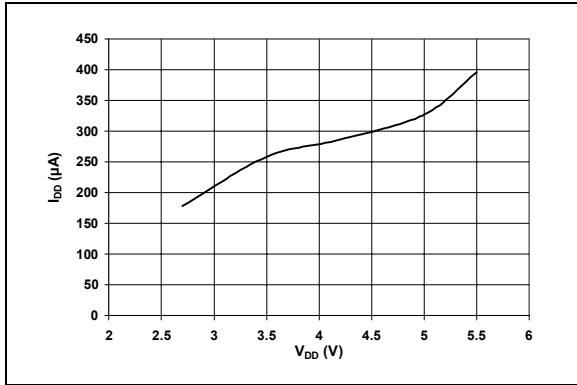


FIGURE 2-31: I_{DD} vs. V_{DD} .

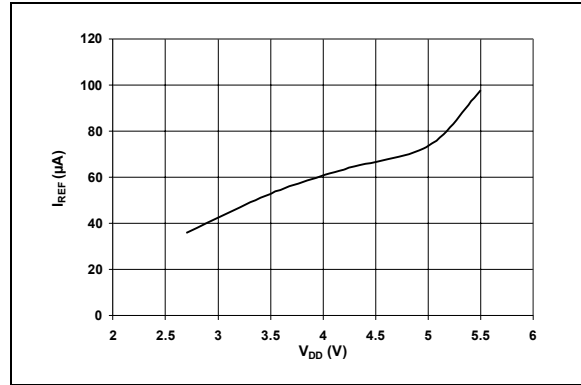


FIGURE 2-34: I_{REF} vs. V_{DD} .

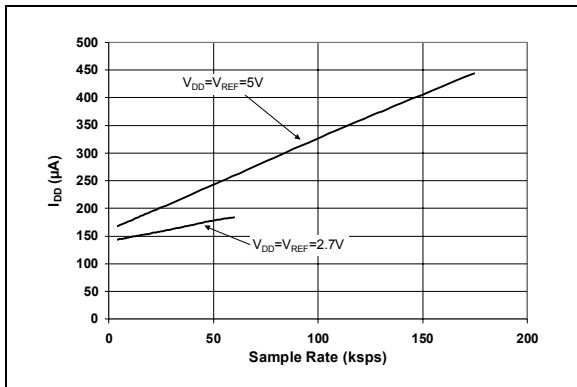


FIGURE 2-32: I_{DD} vs. Sample Rate.

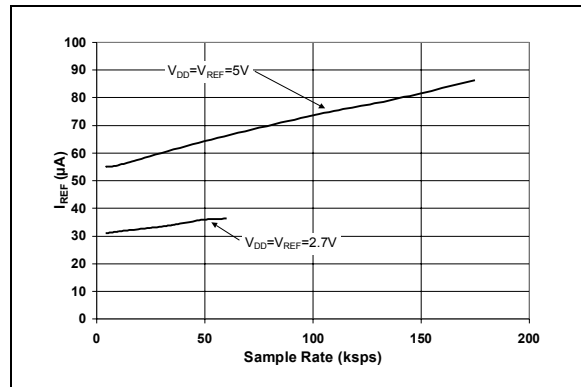


FIGURE 2-35: I_{REF} vs. Sample Rate.

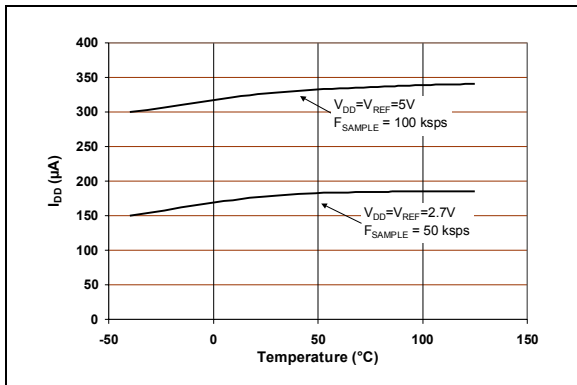


FIGURE 2-33: I_{DD} vs. Temperature.

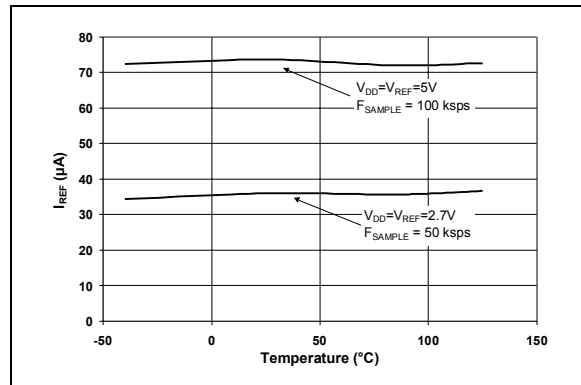


FIGURE 2-36: I_{REF} vs. Temperature.

Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, Full differential input configuration, $V_{SS} = 0V$, $f_{SAMPLE} = 100$ ksp/s, $f_{CLK} = 17 * f_{SAMPLE}$, $T_A = 25^{\circ}C$.

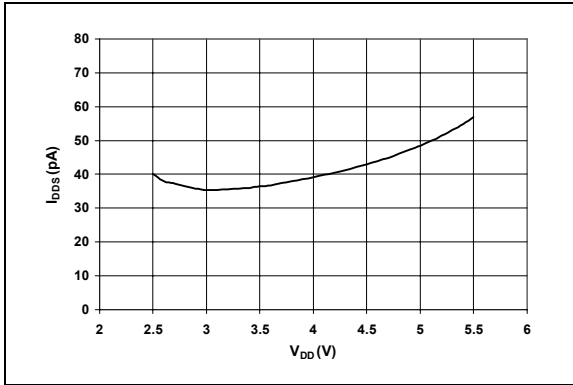


FIGURE 2-37: I_{DDS} vs. V_{DD} .

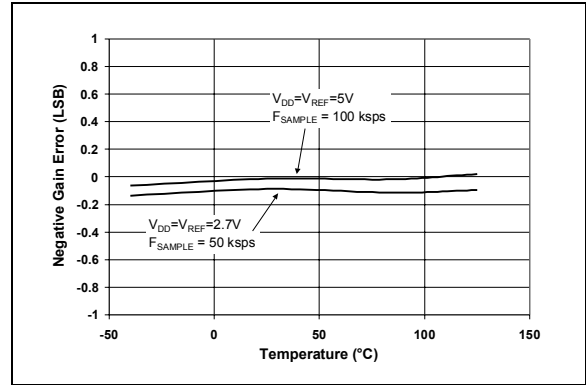


FIGURE 2-40: Negative Gain Error vs. Temperature.

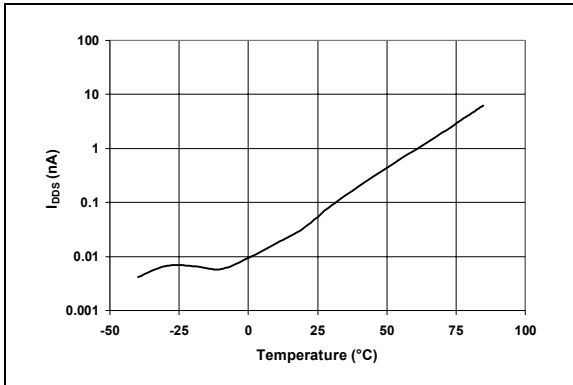


FIGURE 2-38: I_{DDS} vs. Temperature.

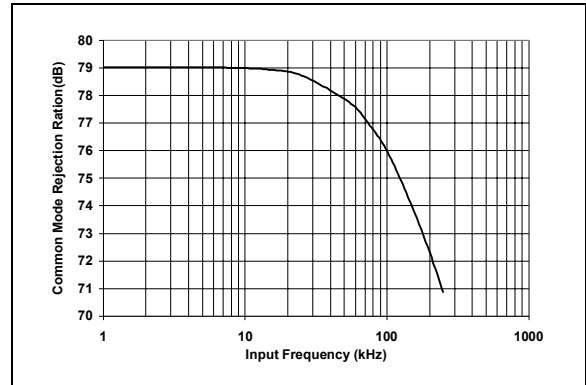


FIGURE 2-41: Common Mode Rejection vs. Frequency.

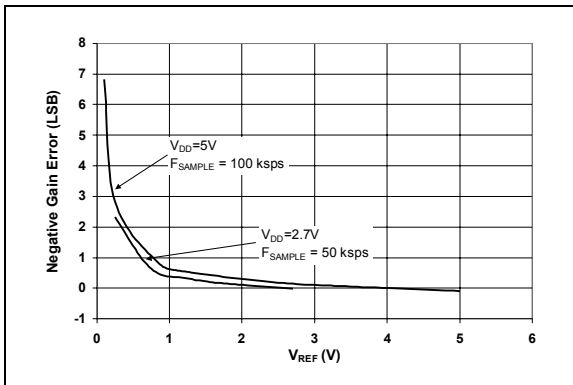


FIGURE 2-39: Negative Gain Error vs. Reference Voltage.

MCP3301

3.0 TEST CIRCUITS

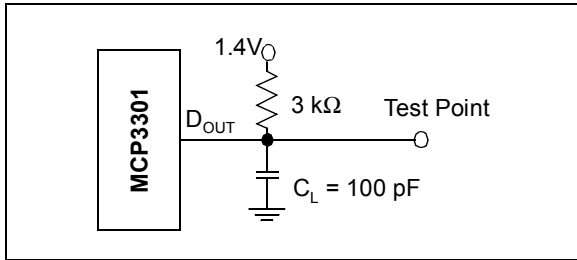


FIGURE 3-1: Load circuit for t_R , t_F , t_{DO}

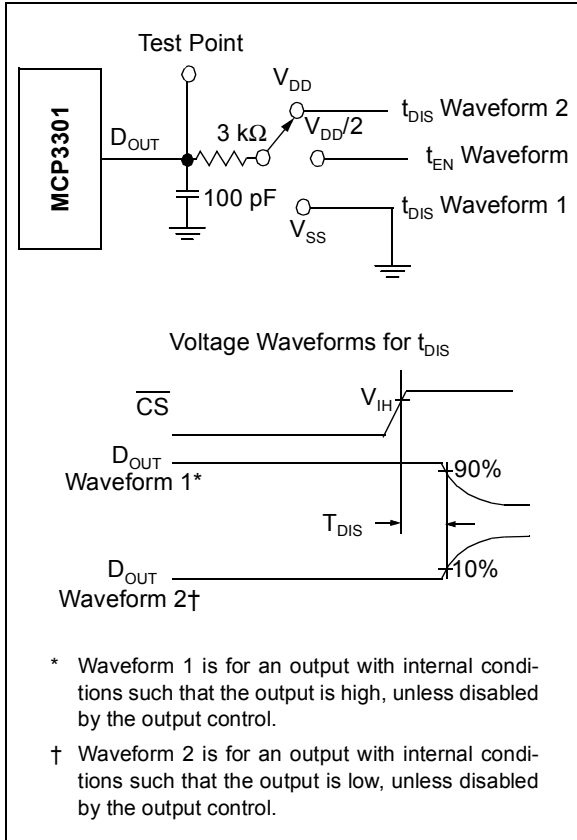


FIGURE 3-2: Load circuit for t_{DIS} and t_{EN}

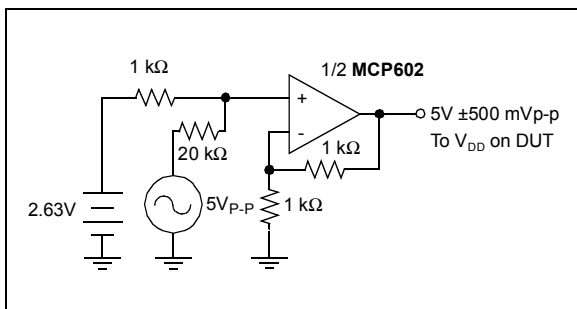


FIGURE 3-3: Power Supply Sensitivity Test Circuit (PSRR).

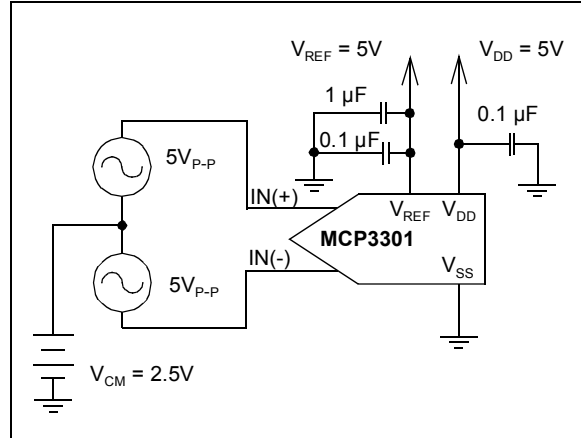


FIGURE 3-4: Full Differential Test Configuration Example.

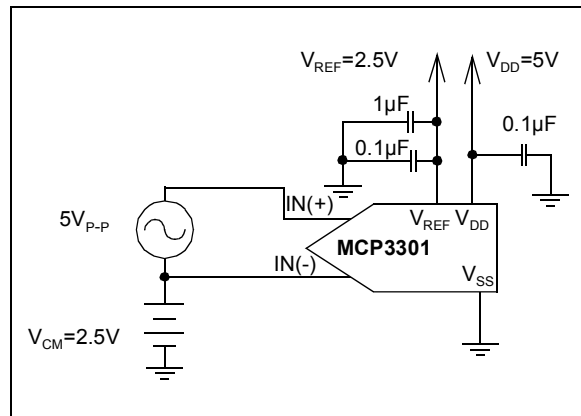


FIGURE 3-5: Pseudo Differential Test Configuration Example.

4.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 4-1.

Name	Function
V _{REF}	Reference Voltage Input
IN(+)	Positive Analog Input
IN(-)	Negative Analog Input
V _{SS}	Ground
CS/SHDN	Chip Select / Shutdown Input
D _{OUT}	Serial Data Out
CLK	Serial Clock
V _{DD}	+2.7V to 5.5V Power Supply

TABLE 4-1: Pin Function Table.

4.1 Voltage Reference (V_{REF})

This input pin provides the reference voltage for the device, which determines the maximum range of the analog input signal and the LSB size.

The LSB size is determined according to the equation shown below. As the reference input is reduced, the LSB size is reduced accordingly.

$$LSB\ Size = \frac{2 \cdot V_{REF}}{8192}$$

When using an external voltage reference device, the system designer should always refer to the manufacturer's recommendations for circuit layout. Any instability in the operation of the reference device will have a direct effect on the accuracy of the ADC conversion results.

4.2 IN(+)

Positive analog input. This pin has an absolute voltage range of V_{SS}-0.3V to V_{DD}+0.3V. The full scale input range is defined as the absolute value of (IN+) - (IN-).

4.3 IN(-)

Negative analog input. This pin has an absolute voltage range of V_{SS}-0.3V to V_{DD}+0.3V. The full scale input range is defined as the absolute value of (IN+) - (IN-).

4.4 V_{SS}

Ground connection to internal circuitry. If an analog ground plane is available it is recommended that this device be tied to the analog ground plane in the circuit. Section 6.6 for more information regarding circuit layout.

4.5 $\overline{\text{CS/SHDN}}$ (Chip Select/Shutdown)

The $\overline{\text{CS/SHDN}}$ pin is used to initiate communication with the device when pulled low. This pin will end a conversion and put the device in low power standby when

pulled high. The $\overline{\text{CS/SHDN}}$ pin must be pulled high between conversions and cannot be tied low for multiple conversions. See Figure 7-2 for serial communication protocol.

4.6 Serial Data Output (D_{OUT})

The SPI serial data output pin is used to shift out the results of the A/D conversion. Data will always change on the falling edge of each clock as the conversion takes place. See Figure 7-2 for serial communication protocol.

4.7 Serial Clock (CLK)

The SPI clock pin is used to initiate a conversion and to clock out each bit of the conversion as it takes place. See Section 6.2 for constraints on clock speed. See Figure 7-2 for serial communication protocol.

4.8 V_{DD}

The voltage on this pin can range from 2.7 to 5.5V. To ensure accuracy a 0.1 μF ceramic bypass capacitor should be placed as close as possible to the pin. See Section 6.6 for more information regarding circuit layout.

5.0 DEFINITION OF TERMS

Bipolar Operation - This applies to either a differential or single ended input configuration where both positive and negative codes are output from the A/D converter. Full bipolar range includes all 8192 codes. For bipolar operation on a single ended input signal, the A/D converter must be configured to operate in pseudo differential mode.

Unipolar Operation - This applies to either a single ended or differential input signal where only one side of the device transfer is being used. This could be either the positive or negative side depending on the which input (IN+ or IN-) is being used for the DC bias. Full unipolar operation is equivalent to a 12-bit converter.

Full Differential Input - Applying a differential signal to both the IN(+) and IN(-) inputs is referred to as full differential operation. This configuration is described in Figure 3-4.

Pseudo-Differential Input - Applying a single ended signal to only one of the input channels with a bipolar output is referred to as pseudo differential operation. To obtain a bipolar output from a single ended input signal the inverting input of the A/D converter must be biased above V_{SS} . This operation is described in Figure 3-5.

Integral Nonlinearity - The maximum deviation from a straight line passing through the endpoints of the bipolar transfer function is defined as the maximum integral nonlinearity error. The endpoints of the transfer function are a point 1/2 LSB above the first code transition (0x1000), and 1/2 LSB below the last code transition (0x0FFF).

Differential Nonlinearity - The difference between two measured adjacent code transitions and the 1 LSB ideal is defined as differential nonlinearity.

Positive Gain Error - This is the deviation between the last positive code transition (0x0FFF) and the ideal voltage level of $V_{REF}-1/2$ LSB, after the bipolar offset error has been adjusted out.

Negative Gain Error - This is the deviation between the last negative code transition (0x1000) and the ideal voltage level of $-V_{REF}-1/2$ LSB, after the bipolar offset error has been adjusted out.

Offset Error - This is the deviation between the first positive code transition (0x0001) and the ideal 1/2 LSB voltage level.

Acquisition Time - The acquisition time is defined as the time during which the internal sample capacitor is charging. This occurs for 1.5 clock cycles of the external CLK as defined in Figure 7-2.

Conversion Time - The conversion time occurs immediately after the acquisition time. During this time successive approximation of the input signal occurs as the 13-bit result is being calculated by the internal circuitry. This occurs for 13 clock cycles of the external CLK as defined in Figure 7-2.

Signal to Noise Ratio - Signal to Noise Ratio (SNR) is defined as the ratio of the signal to noise measured at the output of the converter. The signal is defined as the rms amplitude of the fundamental frequency of the input signal. The noise value is dependant on the device noise as well as the quantization error of the converter and is directly affected by the number of bits in the converter. The theoretical signal to noise ratio for an N-bit converter based on quantization noise only is defined as:

$$SNR = (6.02N + 1.76)dB$$

For a 13-bit converter, the theoretical SNR limit is 80.02 dB.

Total Harmonic Distortion - Total Harmonic Distortion (THD) is the ratio of the rms sum of the harmonics to the fundamental, measured at the output of the converter. For the MCP3301, it is defined using the first 9 harmonics:

$$THD(-dB) = -20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \dots + V_8^2 + V_9^2}}{V_1^2}$$

Here V_1 is the rms amplitude of the fundamental, and V_2 through V_9 are the rms amplitudes of the second through ninth harmonics.

Signal to Noise plus Distortion (SINAD) - Numerically defined, SINAD is the calculated combination of SNR and THD. This number represents the dynamic performance of the converter including any harmonic distortion.

$$SINAD(dB) = 20 \log \sqrt{10^{(SNR/10)} + 10^{-(THD/10)}}$$

Effective Number of Bits - Effective number of bits (ENOB) states the relative performance of the ADC in terms of its resolution. This term is directly related to SINAD by the following equation:

$$ENOB(N) = \frac{SINAD - 1.76}{6.02}$$

For SINAD performance of 78 dB the effective number of bits is 12.66.

Spurious Free Dynamic Range - Spurious Free Dynamic Range (SFDR) is the ratio of the rms value of the fundamental to the next largest component in ADCs output spectrum. This is typically the second harmonic, but could also be a noise peak.

6.0 APPLICATIONS INFORMATION

6.1 Conversion Description

The MCP3301 A/D converter employs a conventional SAR architecture. With this architecture, the potential between the IN+ and IN- inputs are simultaneously sampled and stored with the internal sample circuits for 1.5 clock cycles (t_{ACQ}). Following this sample time, the input hold switches of the converter open and the device uses the collected charge to produce a serial 13-bit binary two's complement output code. This conversion process is driven by the external clock and must include 13 clock cycles, one for each bit. During this process, the most significant bit (MSB) is output first. This bit is the sign bit and indicates if the IN+ or IN- input is at a higher potential.

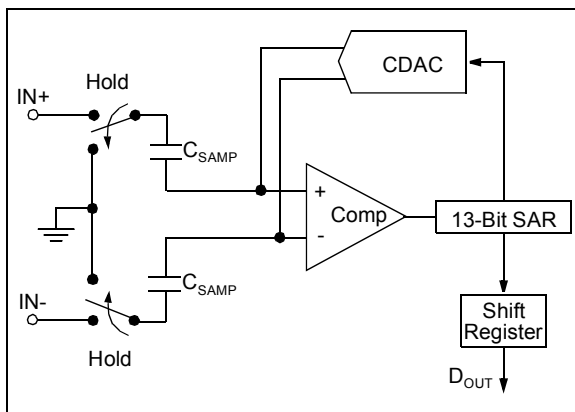


FIGURE 6-1: Simplified Block Diagram.

6.2 Driving the Analog Input

The analog input of the MCP3301 is easily driven either differentially or single ended. Any signal that is common to the two input channels will be rejected by the common mode rejection of the device. During the charging time of the sample capacitor, a small charging current will be required. For low source impedances, this input can be driven directly. For larger source impedances, a larger acquisition time will be required due to the RC time constant that includes the source impedance. For the A/D Converter to meet specification, the charge holding capacitor (C_{SAMPLE}) must be given enough time to acquire a 13-bit accurate voltage level during the 1.5 clock cycle acquisition period.

An analog input model is shown in Figure 6-2. This model is accurate for an analog input, regardless if it is configured as a single ended input or the IN+ and IN- input in differential mode. In this diagram, it is shown that the source impedance (R_S) adds to the internal sampling switch (R_{SS}) impedance, directly affecting the time that is required to charge the capacitor (C_{SAMPLE}). Consequently, a larger source impedance with no additional acquisition time increases the offset, gain, and integral linearity errors of the conversion. To overcome this a slower clock speed can be used to allow for the longer charging time. Figure 6-3 shows the maximum clock speed associated with source impedances.

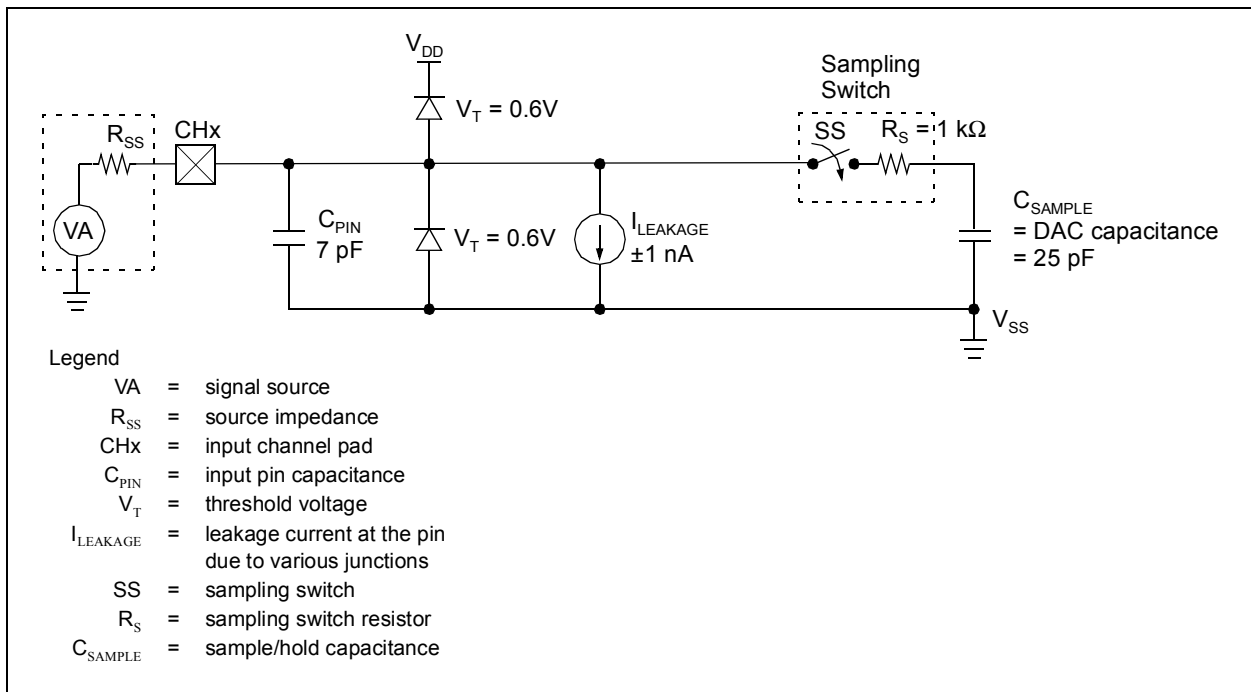


FIGURE 6-2: Analog Input Model.

MCP3301

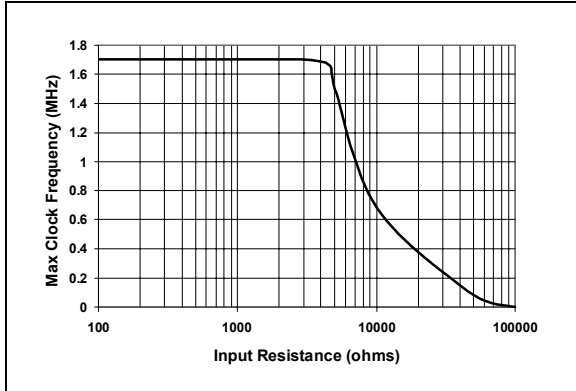


FIGURE 6-3: Maximum Clock Frequency vs. Source Resistance (R_{SS}) to maintain ± 1 LSB INL.

6.2.1 MAINTAINING MINIMUM CLOCK SPEED

When the MCP3301 initiates, charge is stored on the sample capacitor. When the sample period is complete, the device converts one bit for each clock that is received. It is important for the user to note that a slow clock rate will allow charge to bleed off the sample cap while the conversion is taking place. At 85°C (worst case condition), the part will maintain proper charge on the sample capacitor for at least 1.2 ms after the sample period has ended. This means that the time between the end of the sample period and the time that all 13 data bits have been clocked out (t_{CONV}) must not exceed 1.2 ms (effective clock frequency of 10 kHz). Failure to meet this criteria may induce linearity errors into the conversion outside the rated specifications. It should be noted that during the entire conversion cycle, the A/D converter does not have requirements for clock speed or duty cycle, as long as all timing specifications are met.

6.3 Biasing Solutions

For pseudo-differential bipolar operation, the biasing circuit shown in Figure 6-4 shows a single ended input AC coupled to the converter. This configuration will give a digital output range of -4096 to +4095. With the 2.5V reference the LSB size is equal to 610 μ V.

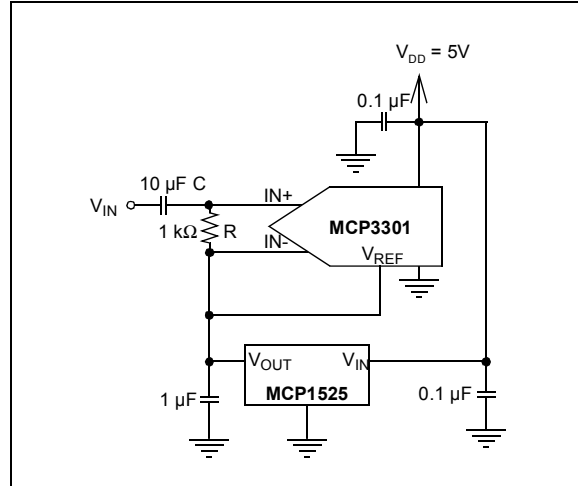


FIGURE 6-4: Pseudo-differential biasing circuit for bipolar operation.

Although the ADC is not production tested with a 2.5V reference as shown, linearity will not change more than 0.1 LSB. See Figure 2-2 and 2-9 for DNL and INL errors versus V_{REF} at $V_{DD} = 5V$. A trade-off exists between the high pass corner and the acquisition time. The value of C will need to be quite large in order to bring down the high pass corner. The value of R will need to be 1 k Ω or less since higher input impedances require additional acquisition time. Using the values in Figure 6-4, we have a 100 Hz corner frequency. See Figure 2-12 for the relationship between input impedance and acquisition time.

Using an external operational amplifier on the input allows for gain and also buffers the input signal from the input to the ADC allowing for a higher source impedance. This circuit is shown in Figure 6-5.

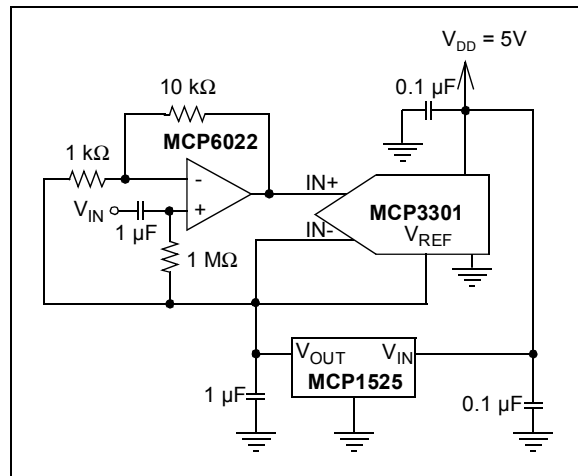


FIGURE 6-5: Adding an amplifier allows for gain and also buffers the input from any high impedance sources.

This circuit shows that some headroom will be lost due to the amplifier output not being able to swing all the way to the rail. An example would be for an output swing of 0V to 5V. This limitation can be overcome by supplying a V_{REF} that is slightly less than the common mode voltage. Using a 2.048V reference for the A/D converter while biasing the input signal at 2.5V solves the problem. This circuit is shown in Figure 6-6.

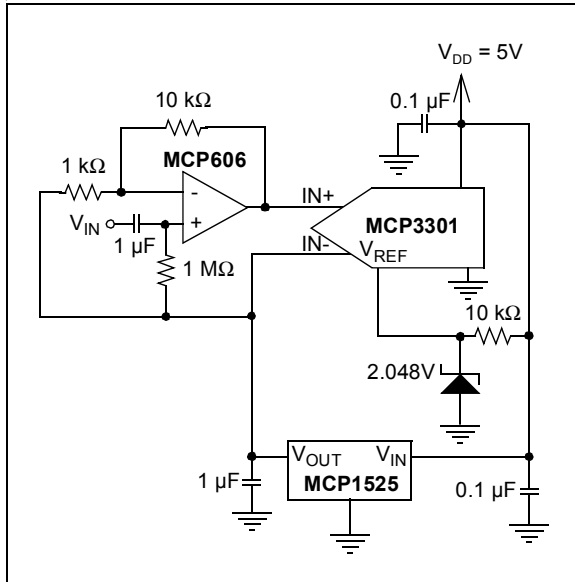


FIGURE 6-6: Circuit solution to overcome amplifier output swing limitation.

6.4 Common Mode Range

The common mode input range has no restriction and is equal to the absolute input voltage range: $V_{SS} - 0.3V$ to $V_{DD} + 0.3V$. However, for a given V_{REF} , the common mode voltage has a limited swing, if the entire range of the A/D converter is to be used. Figure 6-7 and Figure 6-8 show the relationship between V_{REF} and the common mode voltage. A smaller V_{REF} allows for wider flexibility in a common mode voltage. V_{REF} levels down to 400 mV exhibit less than 0.1 LSB change in DNL and INL. Characterization graphs are provided that show this performance relationship, see Figure 2-9 and Figure 2-12.

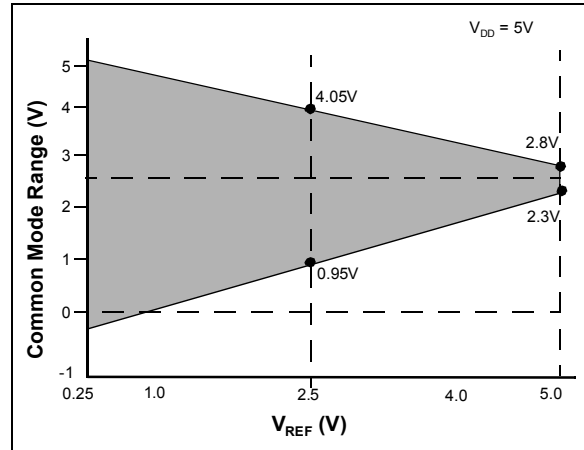


FIGURE 6-7: Common Mode Range of Full Differential input signal versus V_{REF} .

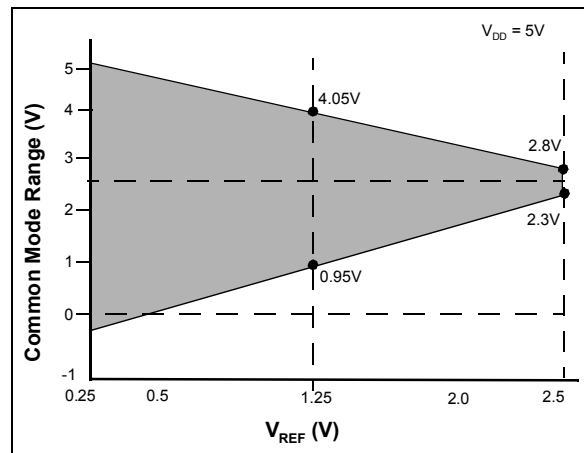


FIGURE 6-8: Common Mode Range versus V_{REF} for Pseudo Differential Input.

6.5 Buffering/Filtering the Analog Inputs

Inaccurate conversion results may occur if the signal source for the A/D converter is not a low impedance source. Buffering the input will overcome the impedance issue. It is also recommended that an analog filter be used to eliminate any signals that may be aliased back into the conversion results. This is illustrated in Figure 6-9 where an op amp is used to drive the analog input of the MCP3301. This amplifier provides a low impedance source for the converter input and a low pass filter, which eliminates unwanted high frequency noise. Values shown are for a 10 Hz Butterworth Low pass filter.

Low pass (anti-aliasing) filters can be designed using Microchip's interactive FilterLab™ software. FilterLab will calculate capacitor and resistor values, as well as determine the number of poles that are required for the application. For more information on filtering signals, see the application note AN699 "Anti-Aliasing Analog Filters for Data Acquisition Systems."

MCP3301

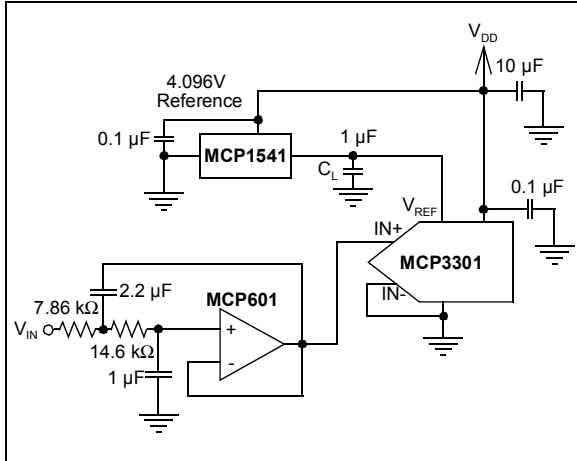


FIGURE 6-9: The MCP601 Operational Amplifier is used to implement a 2nd order anti-aliasing filter for the signal being converted by the MCP3301.

6.6 Layout Considerations

When laying out a printed circuit board for use with analog components, care should be taken to reduce noise wherever possible. A bypass capacitor from V_{DD} to ground should always be used with this device and should be placed as close as possible to the device pin. A bypass capacitor value of 0.1 μF is recommended.

Digital and analog traces should be separated as much as possible on the board and no traces should run underneath the device or the bypass capacitor. Extra precautions should be taken to keep traces with high frequency signals (such as clock lines) as far as possible from analog traces.

Use of an analog ground plane is recommended in order to keep the ground potential the same for all devices on the board. Providing V_{DD} connections to devices in a “star” configuration can also reduce noise by eliminating current return paths and associated errors. See Figure 6-10. For more information on layout tips when using the MCP3301 or other ADC devices, refer to AN-688 “Layout Tips for 12-Bit A/D Converter Applications”.

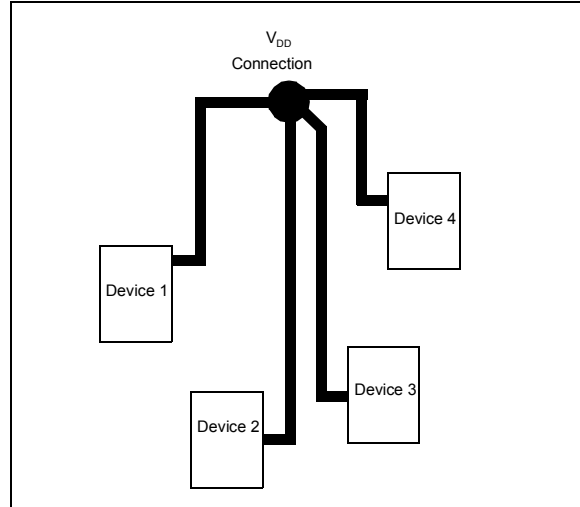


FIGURE 6-10: V_{DD} traces arranged in a ‘Star’ configuration in order to reduce errors caused by current return paths.

7.0 SERIAL COMMUNICATIONS

7.1 Output Code Format

The output code format is a binary two's complement scheme with a leading sign bit that indicates the sign of the output. If the IN+ input is higher than the IN- input, the sign bit will be a zero. If the IN- input is higher, the sign bit will be a '1'.

The diagram shown in Figure 7-1 shows the output code transfer function. In this diagram, the horizontal axis is the analog input voltage and the vertical axis is the output code of the ADC. It shows that when IN+ is equal to IN-, both the sign bit and the data word is zero. As IN+ gets larger with respect to IN-, then the sign bit is a zero and the data word gets larger. The full scale output code is reached at +4095 when the input [(IN+) - (IN-)] reaches $V_{REF} - 1 \text{ LSB}$. When IN- is larger than IN+, the two's complement output codes will be seen with the sign bit being a one. Some examples of analog input levels and corresponding output codes are shown in Table 7-1

Analog Input Levels	Sign Bit	Binary Data	Decimal DATA
Full Scale Positive (IN+)-(IN-)= $V_{REF}-1 \text{ LSB}$	0	1111 1111 1111	+4095
(IN+)-(IN-) = $V_{REF}-2 \text{ LSB}$	0	1111 1111 1110	+4094
IN+ = (IN-) +2 LSB	0	0000 0000 0010	+2
IN+ = (IN-) +1 LSB	0	0000 0000 0001	+1
IN+ = IN-	0	0000 0000 0000	0
IN+ = (IN-) - 1 LSB	1	1111 1111 1111	-1
IN+ = (IN-) - 2 LSB	1	1111 1111 1110	-2
(IN+)-(IN-) = $V_{REF}-2 \text{ LSB}$	1	0000 0000 0001	-4095
Full Scale Negative (IN+)-(IN-) = $V_{REF}-1 \text{ LSB}$	1	0000 0000 0000	-4096

TABLE 7-1: Binary Two's Complement Output Code Examples.

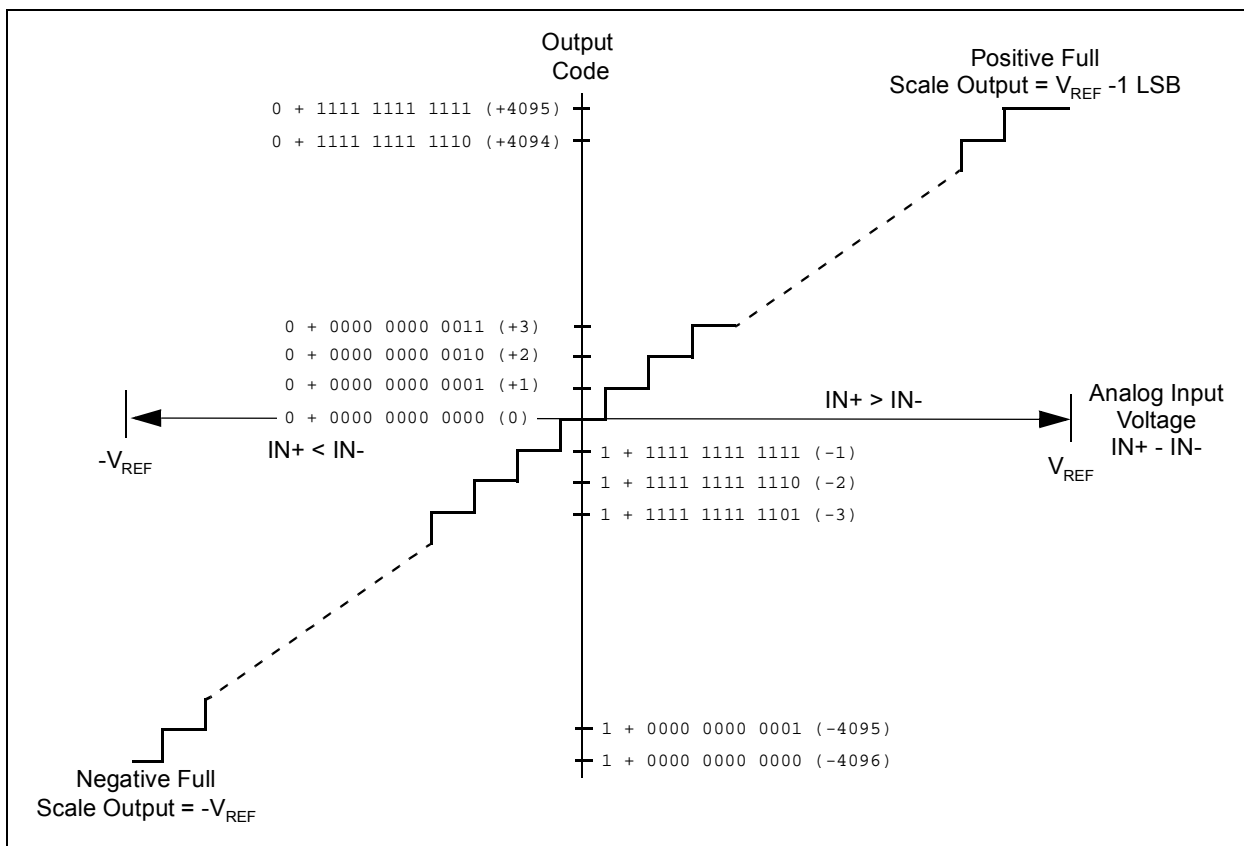


FIGURE 7-1: Output Code Transfer Function.

MCP3301

7.2 Communicating with the MCP3301

Communication with the device is done using a standard SPI compatible serial interface. Initiating communication with the MCP3301 begins with the \overline{CS} going low. If the device was powered up with the \overline{CS} pin low, it must be brought high and back low to initiate communication. The device will begin to sample the analog input on the first rising edge of CLK after \overline{CS} goes low. The sample period will end in the falling edge of the second clock, at which time the device will output a low null bit. The next 13 clocks will output the result of the

conversion with the sign bit first, followed by the 12 remaining data bits, as shown in Figure 7-2. Data is always output from the device on the falling edge of the clock. If all 13 data bits have been transmitted and the device continues to receive clocks while the \overline{CS} is held low, the device will output the conversion result LSB first, as shown in Figure 7-3. If more clocks are provided to the device while \overline{CS} is still low (after the LSB first data has been transmitted), the device will clock out zeros indefinitely.

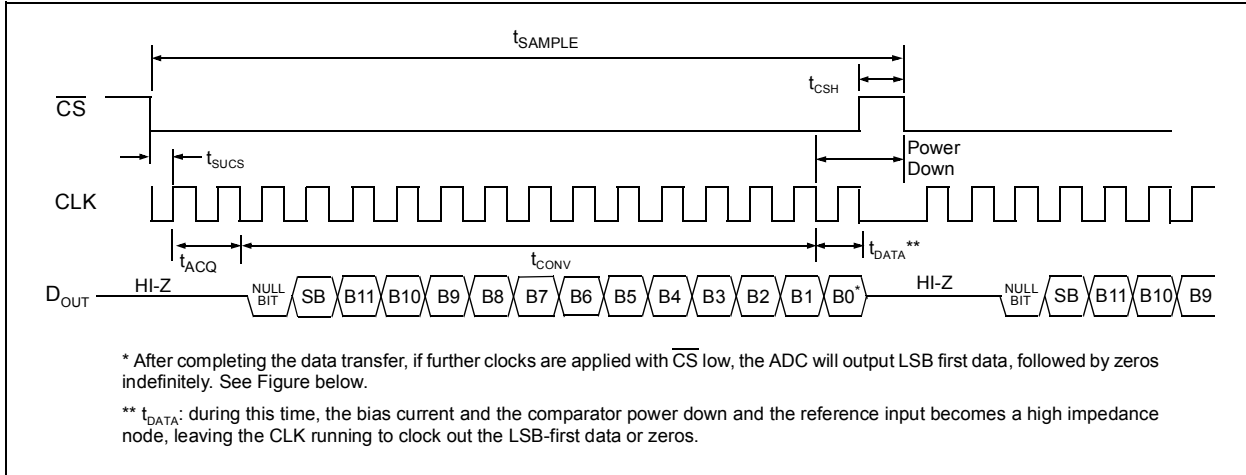


FIGURE 7-2: Communication with MCP3301 (MSB first Format).

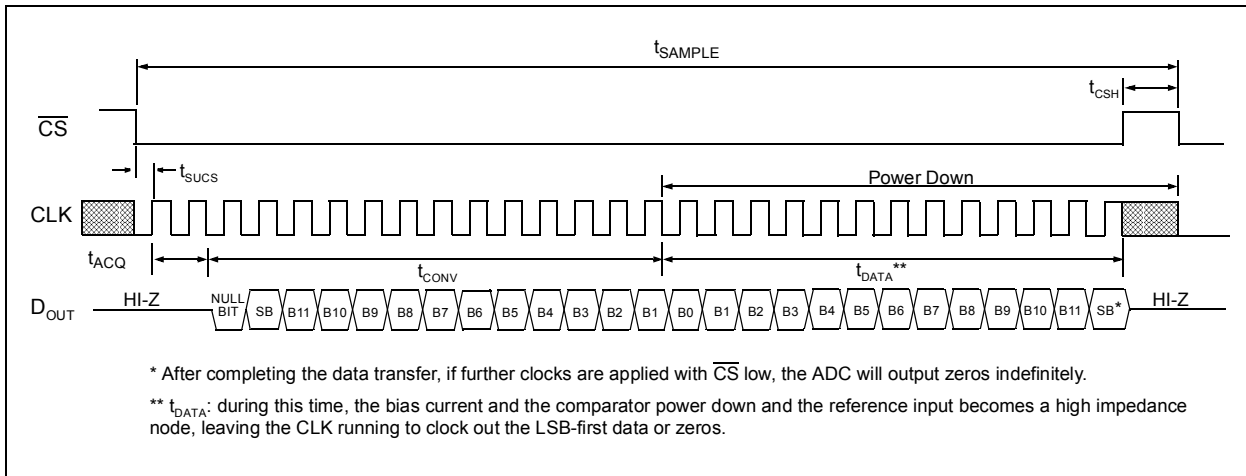


FIGURE 7-3: Communication with MCP3301 (LSB first Format).

7.3 Using the MCP3301 with Microcontroller (MCU) SPI Ports

With most microcontroller SPI ports, it is required to clock out eight bits at a time. Using a hardware SPI port with the MCP3301 is very easy, because each conversion requires 16 clocks. As an example, Figure 7-4 and Figure 7-5 show how the MCP3301 can be interfaced to a microcontroller with a standard SPI port. Since the MCP3301 always clocks data out on the falling edge of clock, the MCU SPI port must be configured to match this operation. SPI Mode 0,0 (clock idles low) and SPI Mode 1,1 (clock idles high) are both compatible with the MCP3301. Figure 7-4 depicts the operation shown in SPI Mode 0,0, which requires that the CLK from the microcontroller idles in the 'low' state. As shown in the diagram, the sign bit is clocked out of the ADC on the falling edge of the third clock pulse, followed by the remaining 12 data bits (MSB first). After the first eight

clocks have been sent to the device, the microcontroller's receive buffer will contain two unknown bits (the output is at high impedance for the first two clocks), the null bit, the sign bit and the highest order four bits of the conversion. After the second eight clocks have been sent to the device, the MCU receive register will contain the lowest order 8 data bits. Notice on the falling edge of clock 16 that the ADC has begun to shift out LSB first data.

Figure 7-5 shows the same scenario in SPI Mode 1,1 which requires that the clock idles in the high state. As with mode 0,0, the ADC outputs data on the falling edge of the clock and the MCU latches data from the ADC in on the rising edge of the clock.

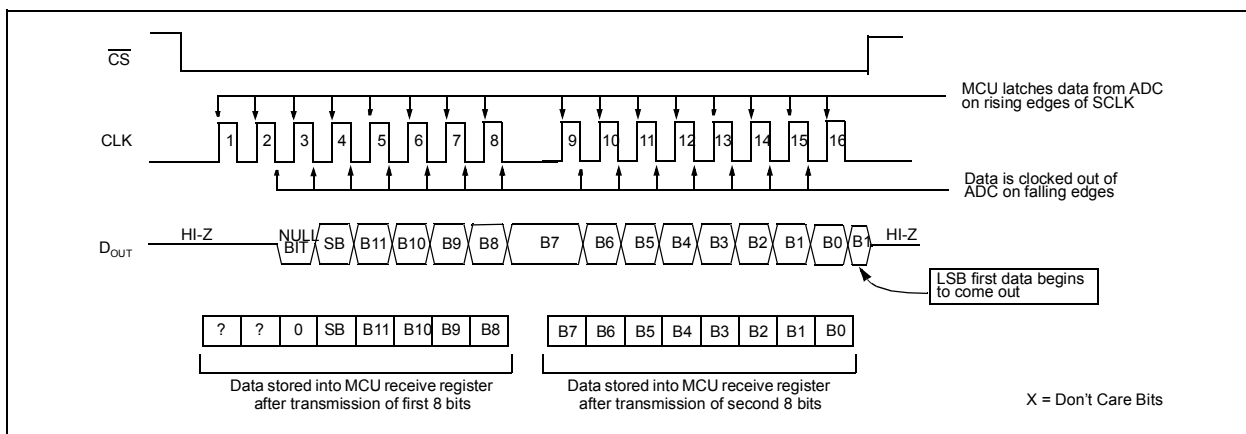


FIGURE 7-4: SPI Communication with the MCP3301 using 8-bit segments (Mode 0,0: SCLK idles low).

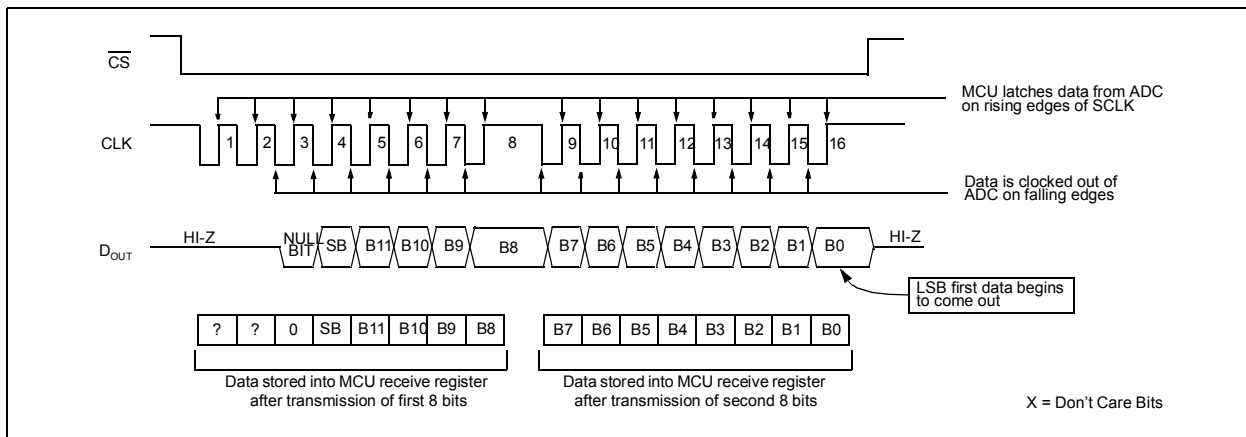


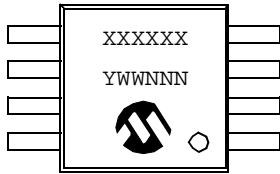
FIGURE 7-5: SPI Communication with the MCP3301 using 8-bit segments (Mode 1,1: SCLK idles high).

MCP3301

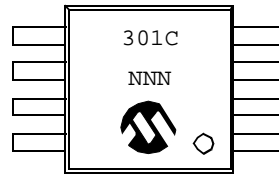
8.0 PACKAGING INFORMATION

8.1 Package Marking Information

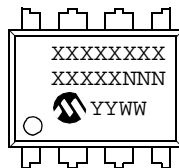
8-Lead MSOP *



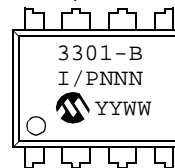
Example:



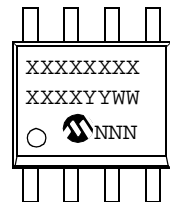
8-Lead PDIP (300 mil)



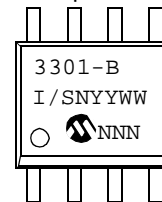
Example:



8-Lead SOIC (150 mil)



Example:

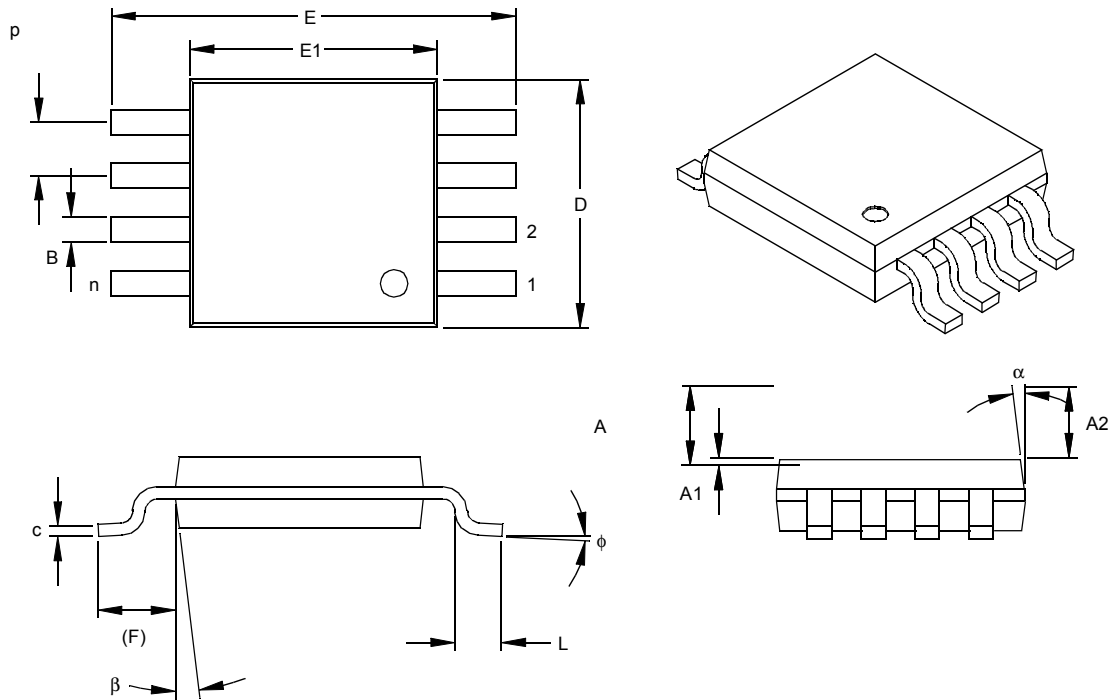


* Please contact Microchip Factory for B-Grade MSOP devices

Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.	

* Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code). For marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

8-Lead Plastic Micro Small Outline Package (MS) (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8				8
Pitch	P	.026			0.65		
Overall Height	A			.044			1.18
Molded Package Thickness	A2	.030	.034	.038	0.76	0.86	0.97
Standoff §	A1	.002		.006	0.05		0.15
Overall Width	E	.184	.193	.200	4.67	4.90	5.08
Molded Package Width	E1	.114	.118	.122	2.90	3.00	3.10
Overall Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.016	.022	.028	0.40	0.55	0.70
Footprint (Reference)	F	.035	.037	.039	0.90	0.95	1.00
Foot Angle	φ	0		6	0		6
Lead Thickness	c	.004	.006	.008	0.10	0.15	0.20
Lead Width	B	.010	.012	.016	0.25	0.30	0.40
Mold Draft Angle Top	α		7			7	
Mold Draft Angle Bottom	β		7			7	

*Controlling Parameter
 § Significant Characteristic

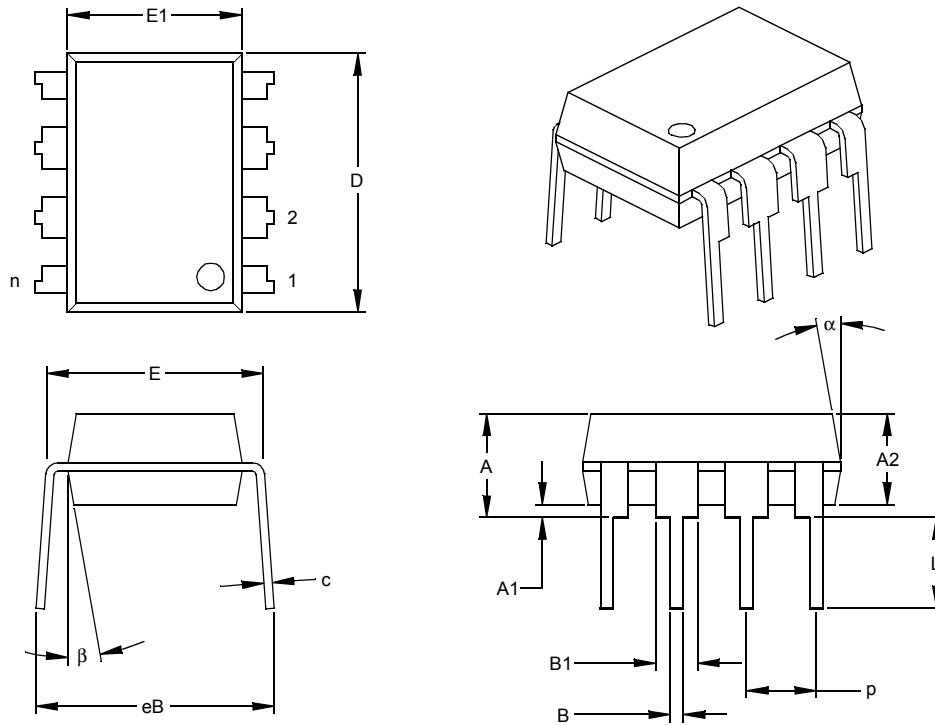
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

Drawing No. C04-111

MCP3301

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Dimension Limits	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter

§ Significant Characteristic

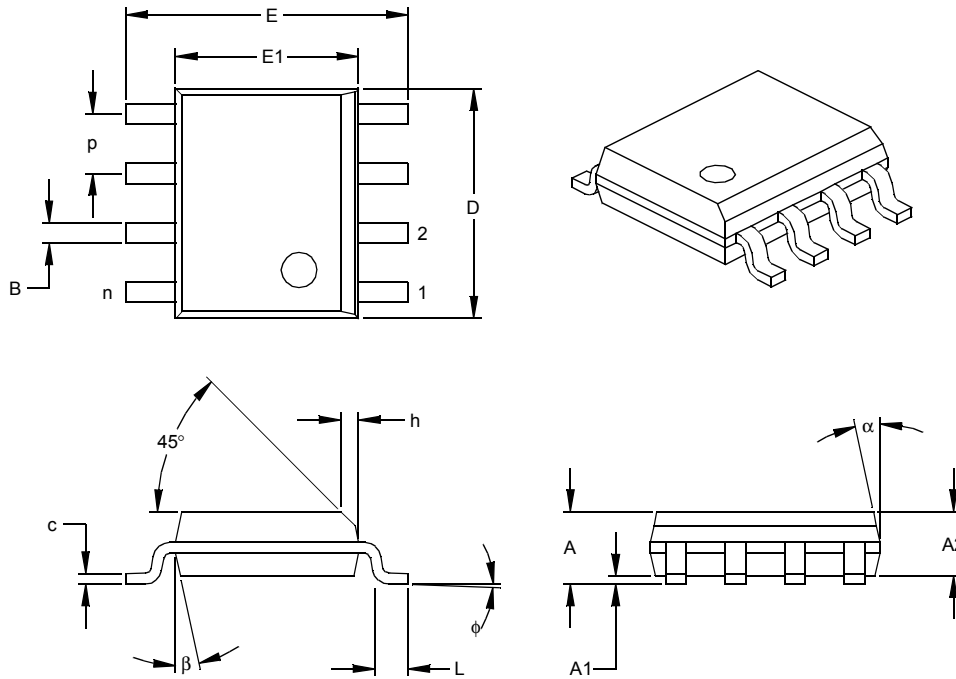
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-001

Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
 § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-012

Drawing No. C04-057

MCP3301

NOTES:

ON-LINE SUPPORT

Microchip provides on-line support on the Microchip World Wide Web (WWW) site.

The web site is used by Microchip as a means to make files and information easily available to customers. To view the site, the user must have access to the Internet and a web browser, such as Netscape or Microsoft Explorer. Files are also available for FTP download from our FTP site.

Connecting to the Microchip Internet Web Site

The Microchip web site is available by using your favorite Internet browser to attach to:

www.microchip.com

The file transfer site is available by using an FTP service to connect to:

<ftp://ftp.microchip.com>

The web site and file transfer site provide a variety of services. Users may download files for the latest Development Tools, Data Sheets, Application Notes, User's Guides, Articles and Sample Programs. A variety of Microchip specific business information is also available, including listings of Microchip sales offices, distributors and factory representatives. Other data available for consideration is:

- Latest Microchip Press Releases
- Technical Support Section with Frequently Asked Questions
- Design Tips
- Device Errata
- Job Postings
- Microchip Consultant Program Member Listing
- Links to other useful web sites related to Microchip Products
- Conferences for products, Development Systems, technical information and more
- Listing of seminars and events

Systems Information and Upgrade Hot Line

The Systems Information and Upgrade Line provides system users a listing of the latest versions of all of Microchip's development systems software products. Plus, this line provides information on how customers can receive any currently available upgrade kits. The Hot Line Numbers are:

1-800-755-2345 for U.S. and most of Canada, and
1-480-792-7302 for the rest of the world.

013001

MCP3301

READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this Data Sheet.

To: Technical Publications Manager Total Pages Sent
RE: Reader Response
From: Name _____
Company _____
Address _____
City / State / ZIP / Country _____
Telephone: (_____) _____ - _____ FAX: (_____) _____ - _____

Application (optional):

Would you like a reply? ___Y ___N

Device: **MCP3301** Literature Number: **DS21700A**

Questions:

1. What are the best features of this document?

2. How does this document meet your hardware and software development needs?

3. Do you find the organization of this data sheet easy to follow? If not, why?

4. What additions to the data sheet do you think would enhance the structure and subject?

5. What deletions from the data sheet could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?

8. How would you improve our software, systems, and silicon products?

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>/XX</u>
Device	Temperature Range	Package
Device:	MCP3301: 13-Bit Serial A/D Converter MCP3301T: 13-Bit Serial A/D Converter (Tape and Reel)	
Temperature Range:	I = -40°C to +85°C	
Package:	MS = Plastic MSOP, 8-lead P = Plastic DIP (300 mil Body), 8-lead SL = Plastic SOIC (150 mil Body), 8-lead	

Examples:

- a) MCP3301-I/P: Industrial Temperature, PDIP package
- b) MCP3301-I/SN: Industrial Temperature, SOIC package
- c) MCP3301-I/ST: Industrial Temperature, SOIC package

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

New Customer Notification System

Register on our web site (www.microchip.com/cn) to receive the most current information on our products.

MCP3301

NOTES:

Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights.

Trademarks


The Microchip name and logo, the Microchip logo, FilterLab, KEELoQ, MPLAB, PIC, PICmicro, PICMASTER, PICSTART, PRO MATE, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

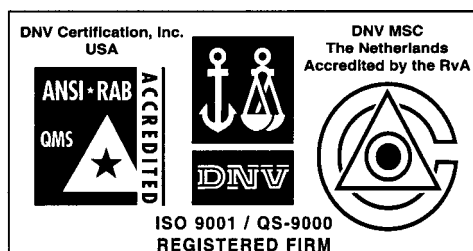
dsPIC, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, microID, microPort, Migratable Memory, MPASM, MPLIB, MPLINK, MPSIM, MXDEV, PICC, PICDEM, PICDEM.net, rPIC, Select Mode and Total Endurance are trademarks of Microchip Technology Incorporated in the U.S.A.

Serialized Quick Term Programming (SQTP) is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2001, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.



Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999. The Company's quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELoQ® code hopping devices, Serial EEPROMs and microperipheral products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001 certified.



MICROCHIP

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200 Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: <http://www.microchip.com>

Rocky Mountain

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966 Fax: 480-792-7456

Atlanta

500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770-640-0034 Fax: 770-640-0307

Boston

2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848 Fax: 978-692-3821

Chicago

333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas

4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423 Fax: 972-818-2924

Dayton

Two Prestige Place, Suite 130
Miamisburg, OH 45342
Tel: 937-291-1654 Fax: 937-291-9175

Detroit

Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250 Fax: 248-538-2260

Kokomo

2767 S. Albright Road
Kokomo, Indiana 46902
Tel: 765-864-8360 Fax: 765-864-8387

Los Angeles

18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

New York

150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

San Jose

Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto

6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Australia

Microchip Technology Australia Pty Ltd
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing

Microchip Technology Consulting (Shanghai)
Co., Ltd., Beijing Liaison Office
Unit 915
Bei Hai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Chengdu

Microchip Technology Consulting (Shanghai)
Co., Ltd., Chengdu Liaison Office
Rm. 2401, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-6766200 Fax: 86-28-6766599

China - Fuzhou

Microchip Technology Consulting (Shanghai)
Co., Ltd., Fuzhou Liaison Office
Rm. 531, North Building
Fujian Foreign Trade Center Hotel
73 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7557563 Fax: 86-591-7557572

China - Shanghai

Microchip Technology Consulting (Shanghai)
Co., Ltd.
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

China - Shenzhen

Microchip Technology Consulting (Shanghai)
Co., Ltd., Shenzhen Liaison Office
Rm. 1315, 13/F, Shenzhen Kerry Centre,
Renminnan Lu
Shenzhen 518001, China
Tel: 86-755-2350361 Fax: 86-755-2366086

Hong Kong

Microchip Technology Hongkong Ltd.
Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

India

Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan

Microchip Technology Japan K.K.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471-6166 Fax: 81-45-471-6122

Korea

Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Singapore

Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-334-8870 Fax: 65-334-8850

Taiwan

Microchip Technology Taiwan
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Denmark

Microchip Technology Nordic ApS
Regus Business Centre
Lautrup høj 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France

Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - 1er Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany

Microchip Technology GmbH
Gustav-Heinemann Ring 125
D-81739 Munich, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Italy

Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom

Arizona Microchip Technology Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

10/01/01

