Si5356

I²C Programmable, Any-Frequency 1–200 MHz, Quad Frequency 8-Output Clock Generator

Features

- Generates any frequency from 1 to 200 MHz on each of the 4 output banks
- Programmable frequency configuration
- Guaranteed 0 ppm frequency synthesis error for any combination of frequencies
- 25 or 27 MHz xtal or 5–200 MHz input clk
- Eight CMOS clock outputs
- Easy to use programming software
- Configurable "triple A" spread spectrum: *any* clock, *any* frequency, and with *any* spread amount
- Programmable output phase adjustment with <20 ps error
- Interrupt pin indicates LOS or LOL
- OEB pin disables all outputs or per bank $\overline{\text{OEB}}$ control via I²C
- Low jitter: 50 ps pk-pk (typ), 100 ps pk-pk period jitter (max)
- Excellent PSRR performance eliminates need for external power supply filtering
- Low power: 45 mA
- Core VDD: 1.8, 2.5, or 3.3 V
- Separate VDDO for each bank of outputs: 1.8, 2.5, or 3.3 V
- Small size: 4x4 mm 24-QFN
- Industrial temperature range: –40 to +85 °C

Ordering Information:

See page 20.

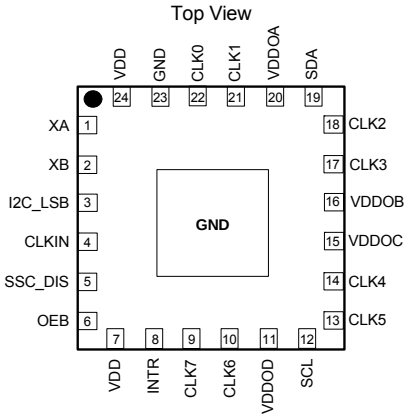
Applications

- Printers
- Audio/video
- DSLAM
- Storage area networks
- Switches/routers
- Servers

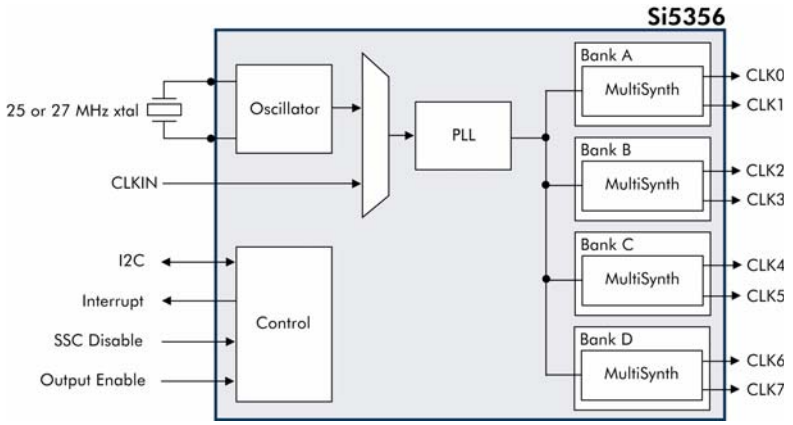
Description

The Si5356 is a highly flexible, I²C programmable clock generator capable of synthesizing four completely non-integer related frequencies up to 200 MHz. The device has four banks of outputs with each bank supporting two CMOS outputs at the same frequency. Using Silicon Laboratories' patented MultiSynth fractional divider technology, all outputs are guaranteed to have 0 ppm frequency synthesis error regardless of configuration, enabling the replacement of multiple clock ICs and crystal oscillators with a single device. Each output bank is independently configurable to support 1.8, 2.5, or 3.3 V. The device is programmable via an I²C/SMBus-compatible serial interface and supports operation from a 1.8, 2.5, or 3.3 V core supply.

Pin Assignments



Functional Block Diagram



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1. Electrical Specifications

Table 1. Recommended Operating Conditions

(V_{DD} = 1.8 V –5% to +10%, 2.5 or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Ambient Temperature	T_A		–40	—	85	°C
Core Supply Voltage	V_{DD}		2.97	3.3	3.63	V
			2.25	2.5	2.75	
			1.71	1.8	1.98	
Output Buffer Supply Voltage	V_{DDO}		1.71	—	3.63	V

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

Table 2. Absolute Maximum Ratings[1]

Parameter	Symbol	Rating	Units
Supply Voltage Range	V_{DD}	–0.5 to +3.8	V
Input Voltage Range (all pins except pins 1,2,5,6)	V_I	–0.5 to 3.8	V
Input Voltage Range (pins 1,2,5,6)	V_{I2}	–0.5 to 1.2	V
Output Voltage Range	V_O	–0.5 to V_{DD} + 0.3	V
Storage Temperature Range	T_S	–55 to +150	°C
ESD Tolerance	HBM	2.5	kV
	CDM	550	V
	MM	175	V
Latch-up Tolerance	LU	JESD78 Compliant	
Soldering Temperature (Pb-free profile)[2]	T_{PEAK}	260	°C

Notes:

1. Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020C.

Table 3. DC Characteristics
(V_{DD} = 1.8 V –5% to +10%, 2.5 or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Current Consumption	I_{DD}	100 MHz on all outputs, 25 MHz refclk	—	45	60	mA
High Level Input Voltage	V_{IH}	CLKIN, I2C_LSB	0.8 x V_{DD}	—	3.63	V
		SSC_DIS, $\overline{OEB}$	0.85	—	1.3	V
Low Level Input Voltage	V_{IL}	CLKIN, I2C_LSB	–0.2	—	0.2 x V_{DD}	V
		SSC_DIS, $\overline{OEB}$	—	—	0.3	V
Clock Output High Level Output Voltage	V_{OH}	Pins: CLK0-7 I_{OH} = –4 mA	V_{DDO} – 0.3	—	—	V
Clock Output Low Level Output Voltage	V_{OL}	Pins: CLK0-7 I_{OH} = +4 mA	—	—	0.3	V
INTR Low Level Output Voltage	V_{OLINTR}	Pin: LOS I_{OH} = +3 mA	0	—	0.4	V
SSC_DIS, $\overline{OEB}$ Input Resistance	R_{IN}		20	—	—	kΩ

Table 4. AC Characteristics

(V_{DD} = 1.8 V –5% to +10%, 2.5 or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input Clock						
Clock Input Frequency	F_{IN}		5	—	200	MHz
Clock Input Rise/Fall Time	T_R/T_F	20 to 80% V_{DD}	—	—	2	ns
Clock Input Duty Cycle	DC	< 2 ns tr/tf	40	—	60	%
Clock Input Capacitance	C_{IN}		—	2	—	pF
Output Clocks						
Clock Output Frequency	F_O		1	—	200	MHz
Clock Output Frequency Synthesis Resolution	F_{RES}	See "3.3. Input and Output Frequency Configuration" on page 10	—	—	0	ppm
Output Load Capacitance	C_L		—	15	—	pF
Clock Output Rise/Fall Time	T_R/T_F	20 to 80% V_{DD}, C_L = 15 pF	—	—	1.7	ns
Clock Output Rise/Fall Time	T_R/T_F	20 to 80% V_{DD}, C_L = 2 pF	—	0.45	0.85	ns
Clock Output Duty Cycle	DC	Measured at $V_{DD}/2$	45	50	55	%
Powerup Time	T_{PU}	POR to output clock valid	—	—	2	ms
Output Enable Time	T_{OE}		—	—	10	µs
Output-Output Skew	T_{SKEW}	Outputs at same frequency, f_{OUT} > 5 MHz	–150	—	+150	ps
Period Jitter	J_{PPKPK}	10000 cycles	—	50	75	ps pk-pk
Cycle-Cycle Jitter	J_{CCPK}	10000 cycles	—	40	70	ps pk
Phase Jitter	J_{PH}	12 kHz to 20 MHz	—	2	—	ps rms
PLL Loop Bandwidth	F_{BW}		—	1.6	—	MHz

Table 5. Crystal Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Crystal Frequency	F_{XTAL}	Option 1	—	25	—	MHz
		Option 2	—	27	—	MHz
Load Capacitance (on-chip differential)	C_L		11	12	13	pF
Crystal Output Capacitance	C_O		—	—	4	pF
Equivalent Series Resistance	ESR	25 MHz	—	—	100	Ω
		27 MHz	—	—	75	Ω
Max Drive Level	d_L		100	—	—	µW

Table 6. Thermal Characteristics

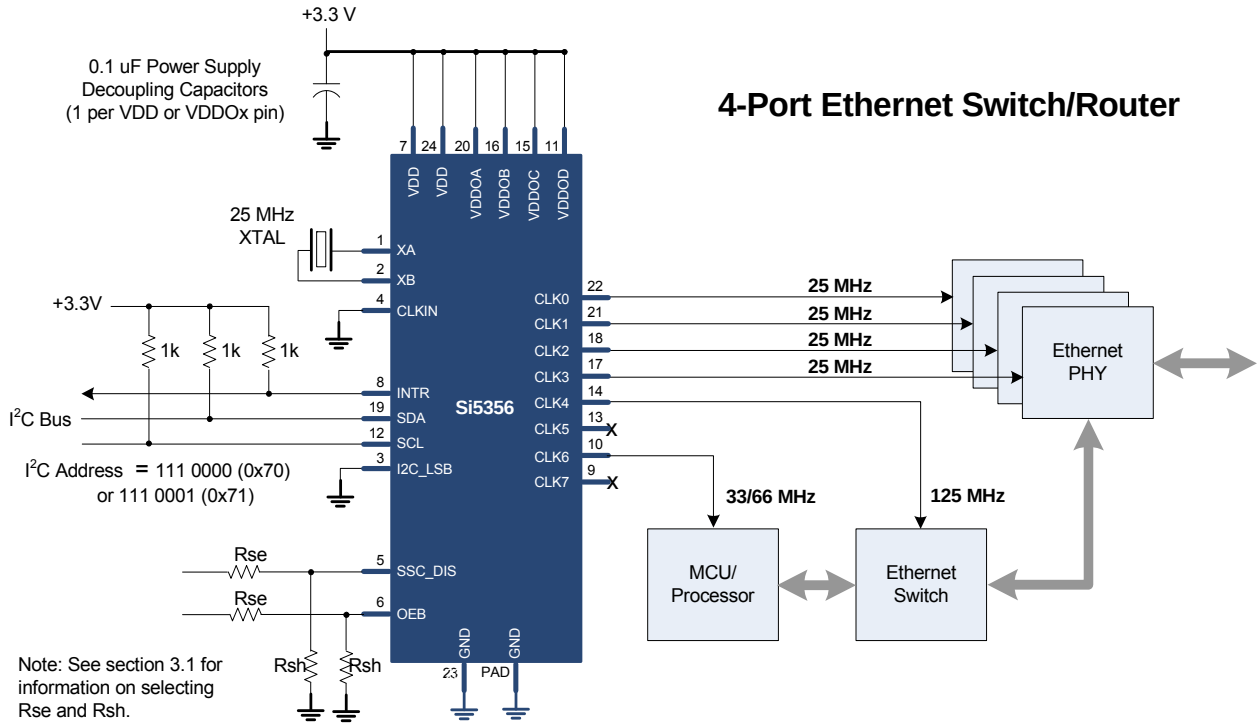
Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	37	°C/W
Thermal Resistance Junction to Case	θ_{JC}	Still Air	25	°C/W

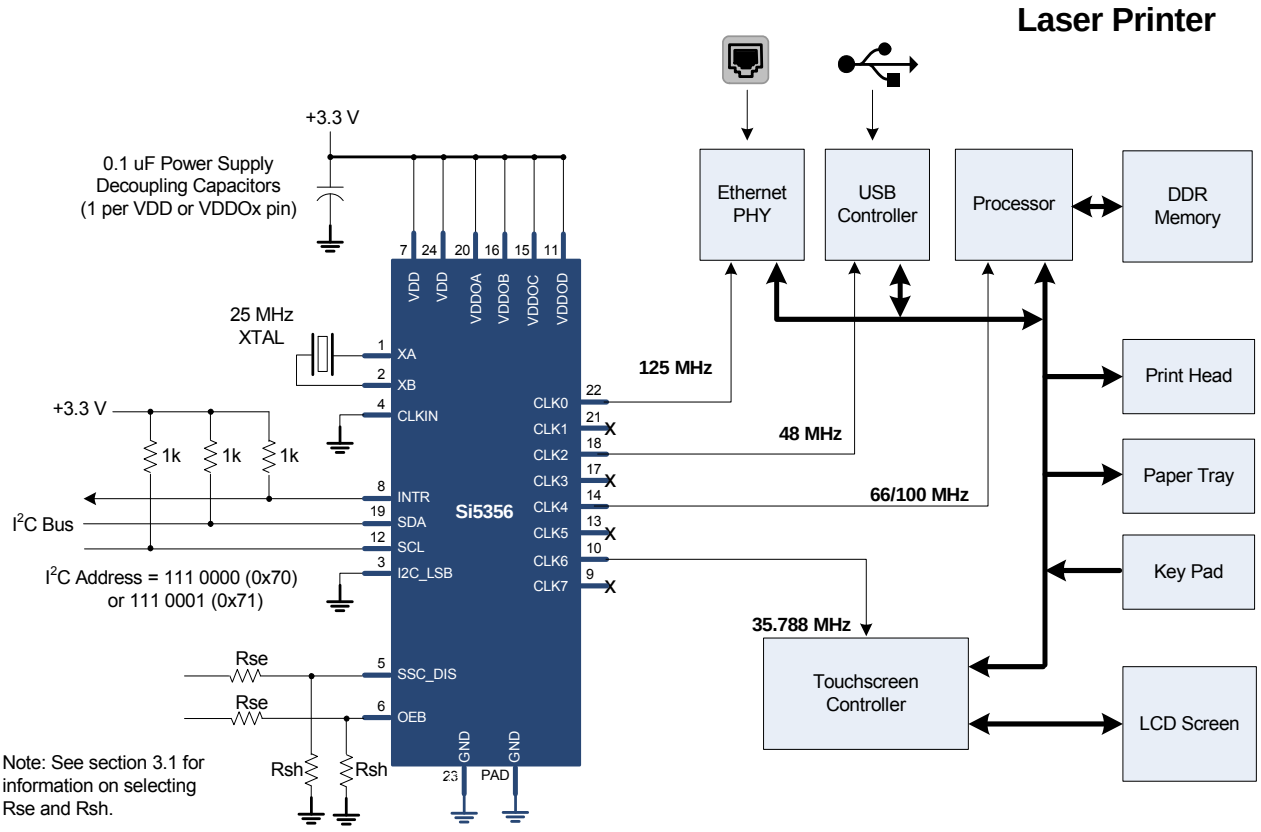
Table 7. I²C Specifications (SCL,SDA)[2]

Parameter	Symbol	Test Condition	Standard Mode		Fast Mode[3]		Unit
			Min	Max	Min	Max	
LOW level input voltage:	V_{ILI2C}		–0.5	$0.3*V_{DDI2C}$	–0.5	$0.3*V_{DDI2C}$[1]	V
HIGH level input voltage:	V_{IHI2C}		$0.7*V_{DDI2C}$	3.63	$0.7*V_{DDI2C}$[1]	3.63	V
Hysteresis of Schmitt trigger inputs	V_{HYS}		N/A	N/A	0.1	—	V
LOW level output voltage (open drain or open collector) at 3 mA sink current	V_{OLI2C}[1]	V_{DDI2C}[1] = 2.5 / 3.3 V	0	0.4	0	0.4	V
		V_{DDI2C}[1] = 1.8 V	N/A	N/A	0	0.2 x V_{DDI2C}	V
Input current	I_{II2C}		–10	10	–10	10	µA
Capacitance for each I/O pin	C_{II2C}	V_{IN} = –0.1 to V_{DDI2C}	—	4	—	4	pF
I²C Bus timeout	—		25	35	25	35	msec

Notes:
1. Only I²C pull up voltages (VDDI2C) of 1.71 to 3.63 V are supported. Must write register 27[7] = 1 if the I²C bus voltage is less than 2.25 V.
2. Refer to NXP's UM10204 I²C-bus specification and user manual, revision 03, for further details: www.nxp.com/acrobat_download/usermanuals/UM10204_3.pdf.
3. Compliant with Fast Mode+ pending characterization.

2. Typical Application Circuits





3. Functional Description

3.1. Input Configuration

The Si5356 input can be driven from either an external crystal or a reference clock. If the crystal input option is used, the Si5356 operates as a free-running clock generator. In this mode of operation the device requires a low cost 25 or 27 MHz fundamental mode crystal connected across XA and XB as shown in Figure 1. Given the Si5356's frequency flexibility, the same crystal can be reused to generate any combination of output frequencies. Custom frequency crystals are not required. The Si5356 integrates the crystal load capacitors on-chip to reduce external component count. The crystal should be placed very close to the device to minimize stray capacitance. To ensure a stable and accurate output frequency, the recommended crystal specifications provided in Table 5 on page 7 must be followed. See AN360 for additional details regarding crystal recommendations.

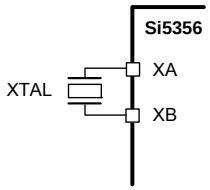


Figure 1. Connecting an XTAL to the Si5356

For synchronous timing applications, the Si5356 can lock to a 5 to 200 MHz CMOS reference clock. A typical interface circuit is shown in Figure 2. A series termination resistor matching the driver's output impedance to the impedance of the transmission line is recommended to reduce reflections.

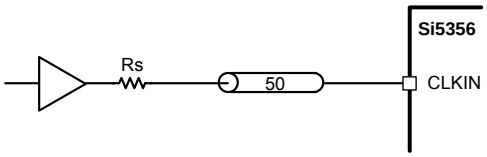


Figure 2. Interfacing CMOS Reference Clocks to the Si5356

Control input signals to SSC_DIS and OEB cannot exceed 1.3 V yet also need to meet the VOH and VOL specifications outlined in Table 3 on page 5. When these inputs are driven from CMOS sources, a resistive attenuator as shown in the Typical Application Circuits must be used. Suggested standard 1% resistor values for RSE and RSH, when using a CMOS source, are given below.

CMOS Level	RSE ohms	RSH ohms
1.8 V	1000	1580
2.5 V	1960	1580
3.3 V	3090	1580

3.2. Breakthrough MultiSynth Technology

Modern timing architectures require a wide range of frequencies which are often non-integer related. Traditional clock architectures address this by using a combination of single PLL ICs, 4-PLL ICs and discrete XOs, often at the expense of BOM complexity and power. The Si5356 use patented MultiSynth technology to dramatically simplify timing architectures by integrating the frequency synthesis capability of 4 phase-locked loops (PLLs) in a single device, greatly minimizing size and power requirements versus traditional solutions. Based on a fractional-N PLL, the heart of the architecture is a low phase noise, high-frequency VCO. The VCO supplies a high frequency output clock to the MultiSynth block on each of the four independent output paths. Each MultiSynth operates as a high-speed fractional divider with Silicon Laboratories' proprietary phase error correction to divide down the VCO clock to the required output frequency with very low jitter.

The first stage of the MultiSynth architecture is a fractional-N divider which switches seamlessly between the two closest integer divider values to produce the exact output clock frequency with 0 ppm error. To eliminate phase error generated by this process, MultiSynth calculates the relative phase difference between the clock produced by the fractional-N divider and the desired output clock and dynamically adjusts the phase to match the ideal clock waveform. This novel approach makes it possible to generate any output clock frequency without sacrificing jitter performance. Based on this architecture, each clock output can produce any frequency from 1 to 200 MHz.

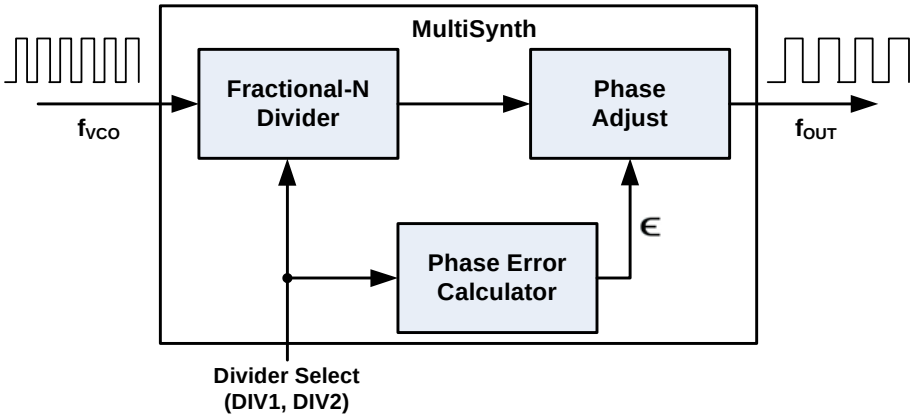


Figure 3. Silicon Labs' MultiSynth Technology

3.3. Input and Output Frequency Configuration

The Si5356 utilizes a single PLL-based architecture, four independent MultiSynth fractional output dividers, and a MultiSynth fractional feedback divider such that a single device provides the clock generation capability of 4 independent PLLs. Unlike competitive multi-PLL solutions, the Si5356 can generate four unique non-integer related output frequencies with 0 ppm frequency error for any combination of output frequencies. In addition, any combination of output frequencies can be generated from a single reference frequency without having to change the crystal or reference clock frequency between frequency configurations.

Frequency configurations are fully programmable by writing to device registers using the I^2C interface. Any combination of output frequencies ranging from 1 to 200 MHz can be configured on each of the device outputs.

The following equation governs how the output frequency is calculated.

$$f_{OUT} = \frac{f_{IN} \times N}{P \times M_i}$$

where f_{IN} is the reference frequency, N is the MultiSynth feedback divider value, P is the reference divider value, M_i is the MultiSynth output divider value and f_{OUT} is the resulting output frequency. The MultiSynth output and feedback dividers are fractional dividers expressed in terms of an integer and a fraction. The integer portion has 10-bit resolution and the fractional portion has 30-bit resolution in both the numerator and denominator, meaning that any output frequency can be defined exactly from the input frequency with exact (0 ppm) frequency synthesis error.

3.4. Output Phase Adjustment

The Si5356 has a digitally-controlled phase adjustment feature that allows the user to adjust the phase of each output clock in relation to the other output clocks. The phase of each output clock can be adjusted with an error of <20 ps over a range of ±45 ns. This feature is available on any clock output that does not have Spread Spectrum enabled.

3.5. CMOS Output Drivers

The Si5356 has 4 banks of outputs with each bank comprised of 2 clocks for a total of 8 CMOS outputs per device. By default, each bank of CMOS output clocks are in-phase. Alternatively, each output clock can be inverted. This feature enables each output pair to operate as a differential CMOS clock. Each of the output banks can operate from a different VDDO supply (1.8 V, 2.5 V, 3.3 V), simplifying usage in mixed supply applications. All clock outputs between 5 and 200 MHz are in-phase to within ±150 ps.

The CMOS output driver has a controlled impedance in the range of 42 to 50 Ω, which includes an internal 22 Ω series resistor. An external series resistor is not needed when driving 50 Ω traces. If higher impedance traces are used then a series resistor may be added. A typical configuration is shown in Figure 4.

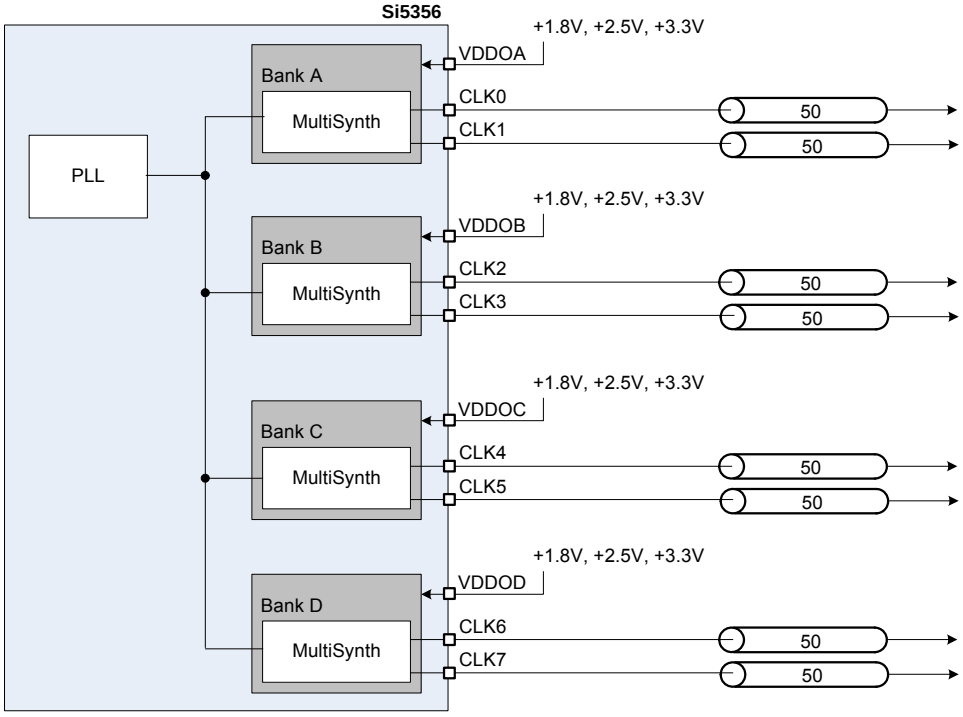


Figure 4. CMOS Output Driver Configuration

3.6. Jitter Performance

The Si5356 provides consistently low jitter for any combination of output frequencies. The device leverages a low phase noise single PLL architecture and Silicon Laboratories' patented MultiSynth fractional output divider technology to deliver period jitter less than 100 ps pk-pk (max) for any frequency configuration. This level of jitter performance is guaranteed across process, temperature and voltage. The Si5356 provides superior performance to traditional multi-PLL solutions which may suffer from degraded jitter performance depending on frequency plan and the number of active PLLs.

3.7. Status Indicators

An interrupt pin (INTR) is available to indicate a loss of signal (LOS) condition, a PLL loss of lock (LOL) condition,or that the PLL is in the process of acquiring lock (SYS_CAL). As shown in Figure 5, a status register at address 218 is available to help identify the exact event that caused the interrupt pin to become active. A LOS condition occurs when there is no input clock input to the Si5356. The loss of lock algorithm works by continuously monitoring the frequency difference between the two inputs of the phase frequency detector. When this frequency difference is greater than 1000 ppm, a loss of lock condition is declared. Note that the VCO will track the input clock frequency for up to ~50000 ppm, which will keep the inputs to the phase frequency detector at the same frequency until the PLL comes out of lock. When a clock input is removed, the interrupt pin will assert, and the clock outputs may drift up to 5%. When the input clock is reapplied with an appropriate frequency, the PLL will again lock.

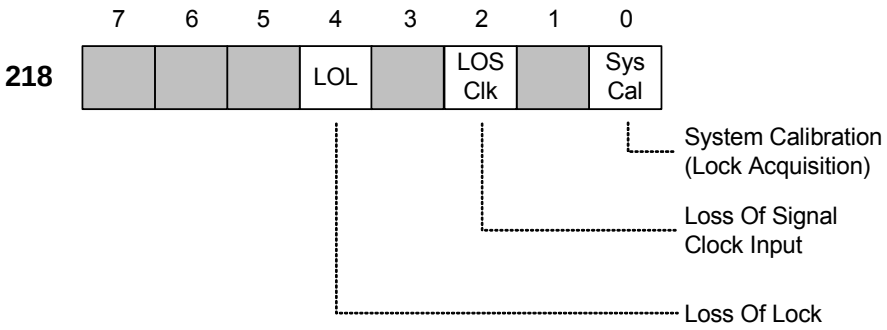


Figure 5. Status Register

3.8. I²C Interface

The Si5356 control interface is a 2-wire bus for bidirectional communication. The bus consists of a bidirectional serial data line (SDA) and a serial clock input (SCL). The device operates as a slave device on the 2-wire bus and is compatible with I²C specifications. Both lines must be connected to the positive supply via an external pull-up. Standard-Mode (100 kbps) and Fast-Mode (400 kbps) operation and 7-bit addressing are supported as specified in the I²C-Bus Specification standard. To accommodate multiple Si5356 devices on the same I²C bus, the Si5356 has pin 3 as I2C_LSB. The complete 7-bit I2C bus address for the device is 70h or 71h depending upon the state of the I2C_LSB pin. In binary, this is written as 111 000[I2C_LSB]. See Figure 6 for the command format for both read and write access.

Data is always sent MSB first. Table 7 includes the AC and DC electrical parameters for the SCL and SDA I/Os, respectively. The timing specifications and timing diagram for the I²C bus can be found in the I²C-Bus Specification standard. SDA timeout support is supported for compatibility with SMBus interfaces. The I²C interface is 3.3 V tolerant.

The I²C bus can be operated at a bus voltage of 1.71 to 3.63 V and should have a pullup resistor as recommended by the I²C-Bus Specification.

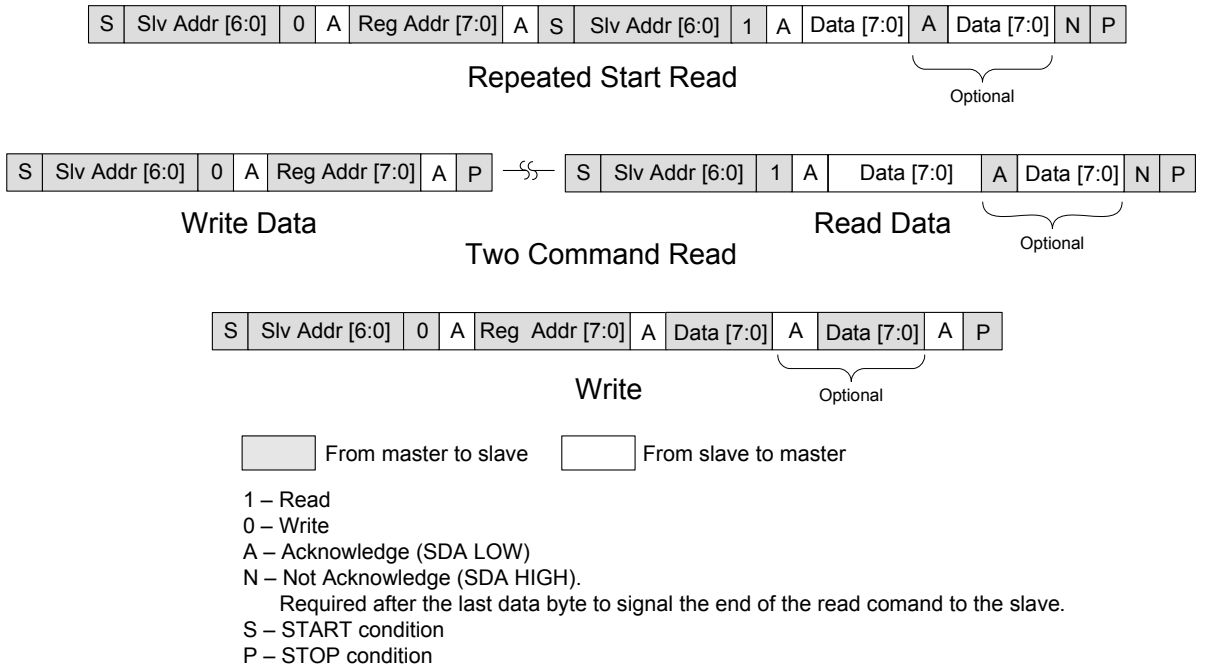


Figure 6. I²C/SMBus-Compatible Command Format

3.9. Custom Device Configurations

The Si5356 is fully configurable by writing to internal registers through the I^2C interface. After each power cycle the register settings are restored to their factory default values. For applications that require a custom configuration at power-up, the Si5356 is orderable with a custom default register setting. See "7. Ordering Guide" on page 20 more for details.

3.10. Spread Spectrum

To reduce electro magnetic interference (EMI), the Si5356 supports spread spectrum modulation. The output clock frequencies can be modulated to spread energy across a broader range of frequencies, lowering system EMI. The modulation rate is the time required to transition from the maximum spread spectrum frequency to the minimum spread spectrum frequency and then back to the maximum frequency. The Si5356 implements spread spectrum using patented MultiSynth technology to achieve previously unattainable precision in both modulation rate and spreading magnitude as shown in Figure 7. This enables the Si5356 to provide “triple A” spread spectrum. Spread spectrum can be applied to *any* output clock, *any* clock frequency, and *any* spread amount. Spread spectrum can be enabled or disabled on a per-bank basis. The device supports center spread (±0.1% to ±5%) and down spread (–0.1% to –5%). In addition, the device has extensive on-chip voltage regulation such that power supply variation does not influence the device’s spread spectrum clock waveforms.

The programming of Spread Spectrum is made easy by using the Si5356 Programmer. Spread spectrum on all the outputs can be enabled or disabled using the SSC_DIS pin, or independently for each output bank through the I^2C interface.

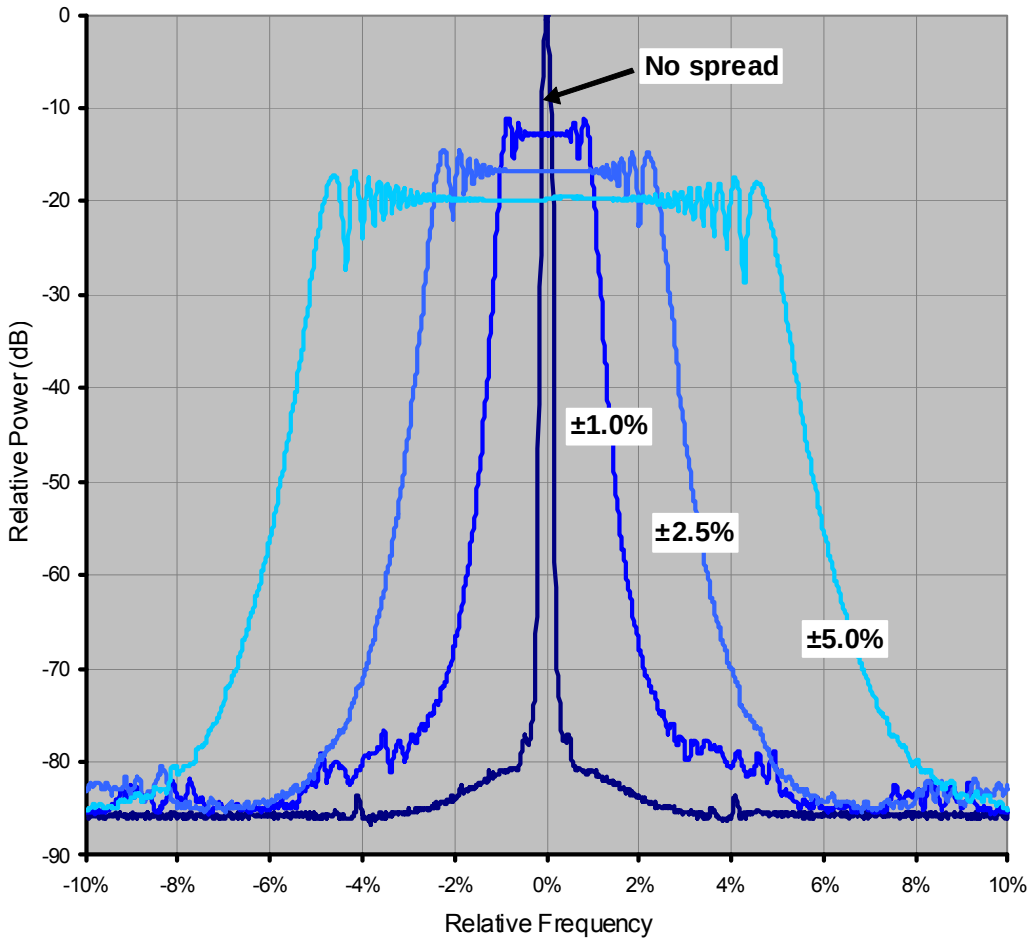


Figure 7. Configurable Spread Spectrum

3.11. Power Supply Considerations

The Si5356 has two core supply voltage pins (V_{DD}) and four clock output bank supply voltage pins (V_{DDOA}–V_{DDOD}), enabling the device to be used in mixed supply applications. The Si5356 does not require ferrite beads for power supply filtering. The device has extensive on-chip power supply regulation to minimize the impact of power supply noise on output jitter. Figure 8 shows that the additive jitter created when a significant amount of noise is applied to the device power supply is very small.

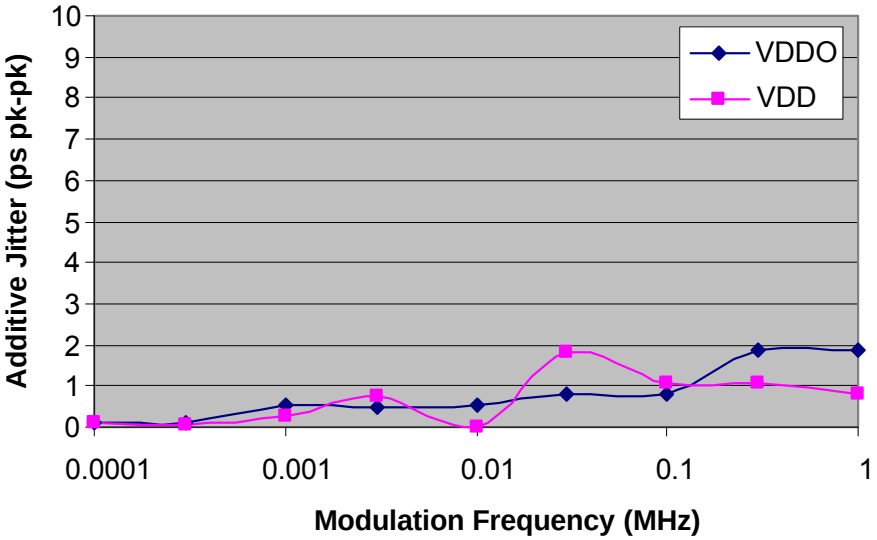
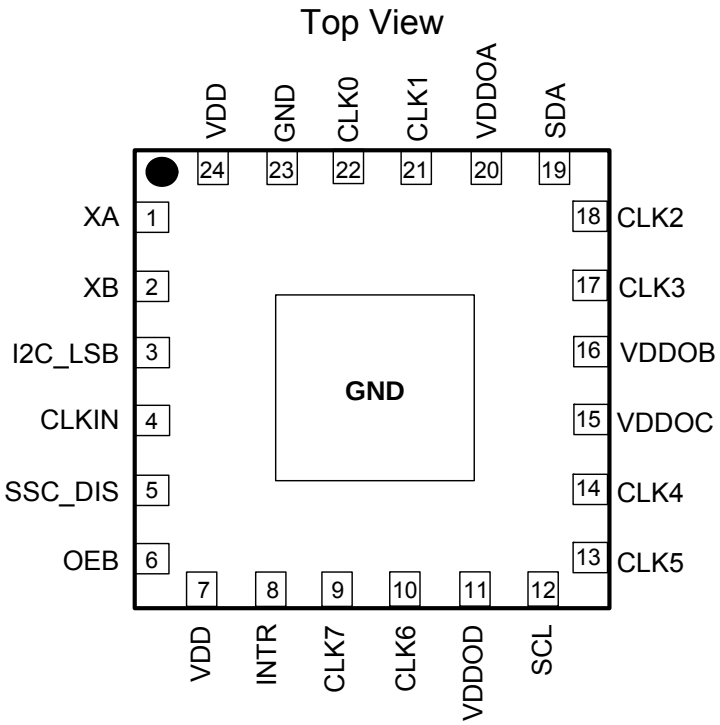


Figure 8. Peak-to-Peak Additive Jitter from 100 mV Sine Wave on Supply

4. Pin Descriptions—Si5356



Note: Center pad must be tied to GND for normal operation.

Table 8. Si5356 Pin Descriptions

Pin #	Pin Name	I/O	Description
1	XA	I	**External Crystal.** If a 25 or 27 MHz crystal is used as the device frequency reference, connect it across XA and XB. If no input clock is used, this pin should be tied to GND.
2	XB	I	**External Crystal.** If a 25 or 27 MHz crystal is used as the device frequency reference, connect it across XA and XB. If no input clock is used, this pin should be tied to GND.
3	I2C_LSB	I	**I^2C LSB Address Bit** This pin is the least significant bit of the Si5356 I^2C address allowing up to two Si5356 devices to occupy the same I^2C bus.
4	CLKIN	I	**Single-Ended Input Clock.** If a single-ended clock is used as the device frequency reference, connect it to this pin. This pin functions as a high-impedance input for CMOS clock signals. The input should be dc coupled. If a crystal is used as the device frequency reference, this pin should be tied to GND.

Table 8. Si5356 Pin Descriptions (Continued)

5	SSC_DIS	I	**Spread Spectrum Disable.** This pin allows disabling of the spread spectrum feature on the output clocks. Connect to 1.2 V to disable spread spectrum on all outputs. Connect to GND to enable spread spectrum. Note that the maximum voltage level on this pin must not exceed 1.2 V. A resistor voltage divider is recommended when controlled by a signal greater than 1.2 V. See the Typical Application Circuit for details.
6	OEB	I	**Output Enable (Active Low)** This pin allows disabling the output clocks. Connect to 1.2 V to disable all outputs. Connect to GND to enable all outputs. Note that the maximum voltage level on this pin must not exceed 1.2 V. A resistor voltage divider is recommended when controlled by a signal greater than 1.2 V. See the Typical Application Circuit for details.
7	VDD	VDD	**Core Supply Voltage.** The device operates from a 1.8, 2.5, or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin.
8	INTR	O	**Interrupt** This pin functions as an maskable interrupt output. 0 = No interrupt 1 = Interrupt present This pin is open drain and requires an external $\geq$1 kΩ pullup resistor.
9	CLK7	O	**Output Clock 7.** CMOS output clock. If unused, this pin must be left floating.
10	CLK6	O	**Output Clock 6.** CMOS output clock. If unused, this pin must be left floating.
11	VDDOD	VDD	**Clock Output Bank D Supply Voltage.** Power supply for clock outputs 6 and 7. May be operated from a 1.8, 2.5, or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin. If CLK6/7 are not used, this pin must be tied to pin 7 and/or pin 24.
12	SCL	I	**I^2C Serial Clock Input.**
13	CLK5	O	**Output Clock 5.** CMOS output clock. If unused, this pin must be left floating.
14	CLK4	O	**Output Clock 4.** CMOS output clock. If unused, this pin must be left floating.
15	VDDOC	VDD	**Clock Output Bank C Supply Voltage.** Power supply for clock outputs 4 and 5. May be operated from a 1.8, 2.5 or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin. If CLK4/5 are not used, this pin must be tied to pin 7 and/or pin 24.
16	VDDOB	VDD	**Clock Output Bank B Supply Voltage.** Power supply for clock outputs 2 and 3. May be operated from a 1.8, 2.5, or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin. If CLK2/3 are not used, this pin must be tied to pin 7 and/or pin 24.
17	CLK3	O	**Output Clock 3.** CMOS output clock. If unused, this pin must be left floating.
18	CLK2	O	**Output Clock 2.** CMOS output clock. If unused, this pin must be left floating.

Table 8. Si5356 Pin Descriptions (Continued)

19	SDA	I/O	**I^2C Serial Data.**
20	VDDOA	VDD	**Clock Output Bank A Supply Voltage.** Power supply for clock outputs 0 and 1. May be operated from a 1.8, 2.5, or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin. If CLK0/1 are not used, this pin must be tied to pin 7 and/or pin 24.
21	CLK1	O	**Output Clock 1.** CMOS output clock. If unused, this pin must be left floating.
22	CLK0	O	**Output Clock 0.** CMOS output clock. If unused, this pin must be left floating.
23	GND	GND	**Ground.** Must be connected to system ground. Minimize the ground path impedance for optimal performance of the device.
24	VDD	VDD	**Core Supply Voltage.** The device operates from a 1.8, 2.5, or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin.
GND PAD	GND	GND	**Ground Pad.** This is the large pad in the center of the package. Device specifications cannot be guaranteed unless the ground pad is properly connected to a ground plane on the PCB. See "6. Recommended PCB Layout" on page 19 for the PCB pad sizes and ground via requirements.

5. Package Outline: 24-Lead QFN

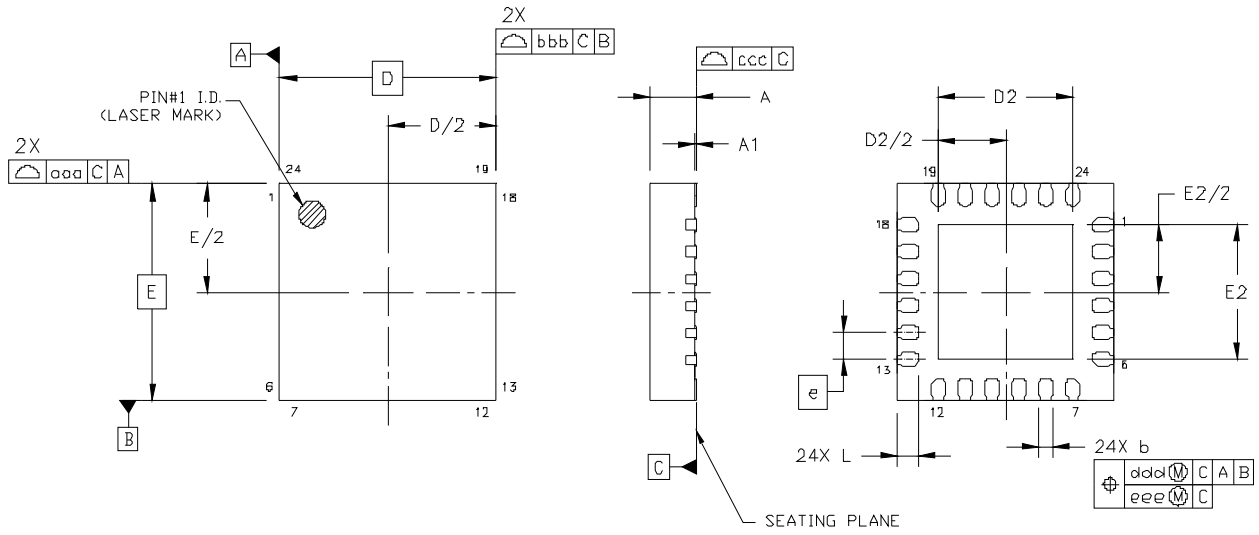


Figure 9. 24-Lead Quad Flat No-Lead (QFN)

Table 9. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		4.00 BSC.	
D2	2.35	2.50	2.65
e		0.50 BSC.	
E		4.00 BSC.	
E2	2.35	2.50	2.65
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Outline MO-220, variation VGGD-8.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

6. Recommended PCB Layout

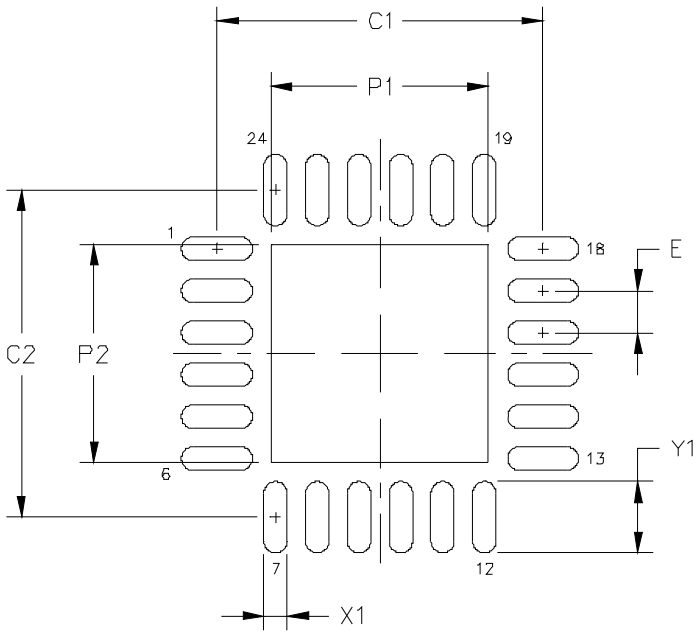


Table 10. PCB Land Pattern

Dimension	Min	Nom	Max
P1	2.50	2.55	2.60
P2	2.50	2.55	2.60
X1	0.20	0.25	0.30
Y1	0.75	0.80	0.85
C1	3.90		
C2	3.90		
E	0.50		

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. Connect the center ground pad to a ground plane with no less than five vias. These 5 vias should have a length of no more than 20 mils to the ground plane. Via drill size should be no smaller than 10 mils. A longer distance to the ground plane is allowed if more vias are used to keep the inductance from increasing.

Solder Mask Design

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

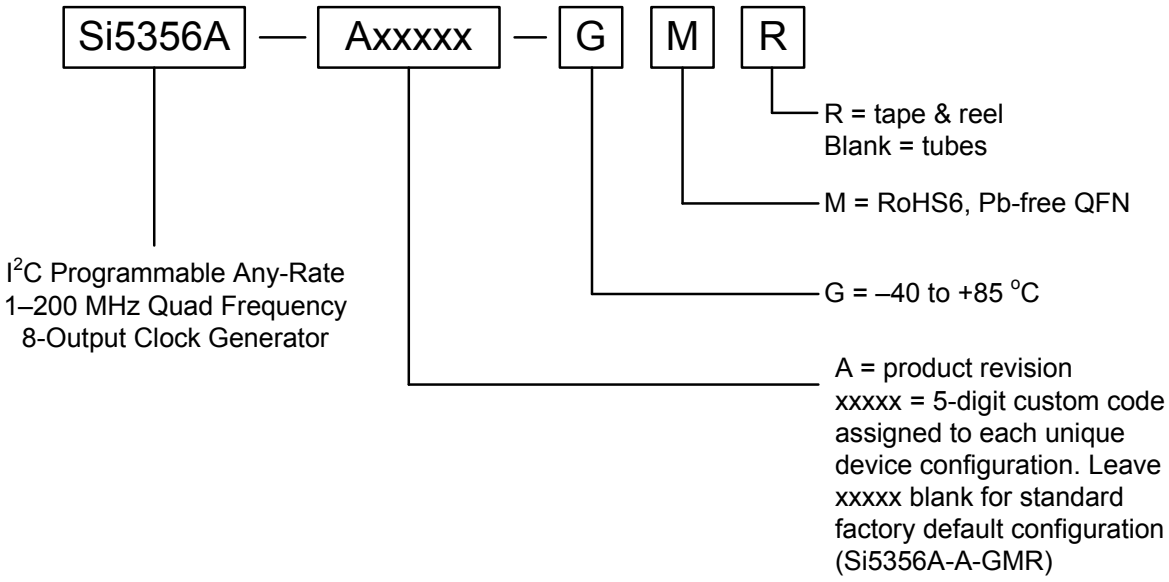
Stencil Design

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
9. A 2x2 array of 1.0 mm square openings on 1.25 mm pitch should be used for the center ground pad.

Card Assembly

10. A No-Clean, Type-3 solder paste is recommended.
11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

7. Ordering Guide



DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Improved specification details on input signals.
- Added phase and cycle-cycle jitter specifications.
- Added thermal resistance junction to case.
- Improved application circuits.
- Added gnd via requirement details.
- Added differential CMOS capability.

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