

# SN54ABT843, SN74ABT843 9-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS197D – FEBRUARY 1991 – REVISED MAY 1997

- State-of-the-Art *EPIC-IIB™* BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- High-Drive Outputs ( $-32\text{-mA } I_{OH}$ ,  $64\text{-mA } I_{OL}$ )
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Plastic (NT) and Ceramic (JT) DIPs

## description

The 'ABT843 9-bit latches are designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The nine transparent D-type latches provide true data at the outputs.

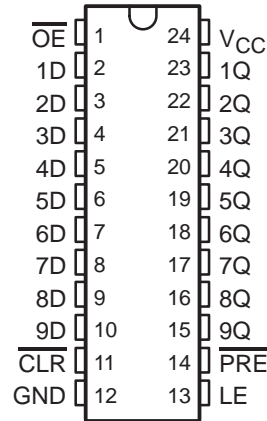
A buffered output-enable ( $\overline{OE}$ ) input can be used to place the nine outputs in either a normal logic state (high or low logic levels) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$  does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

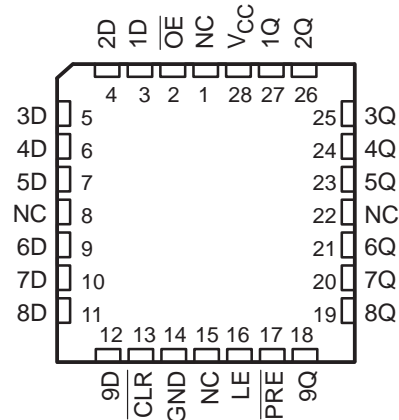
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT843 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT843 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

SN54ABT843 . . . JT OR W PACKAGE  
SN74ABT843 . . . DB, DW, OR NT PACKAGE  
(TOP VIEW)



SN54ABT843 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection



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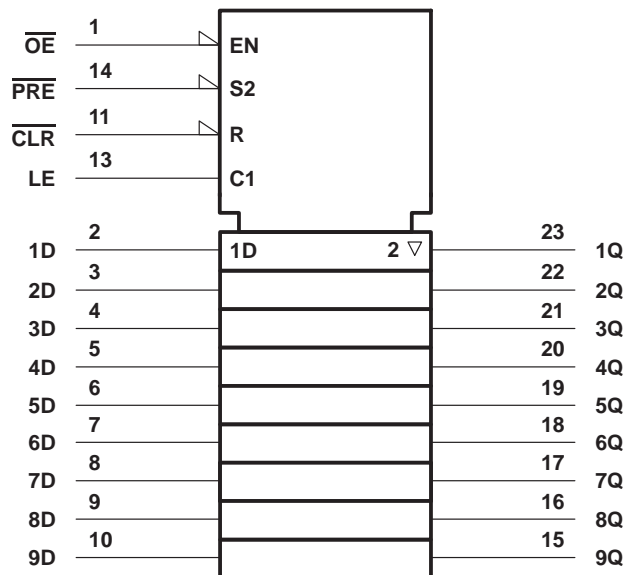
# SN54ABT843, SN74ABT843 9-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

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FUNCTION TABLE

INPUTS					OUTPUT
PRE	CLR	OE	LE	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q <sub>0</sub>
X	X	H	X	X	Z

## logic symbol†

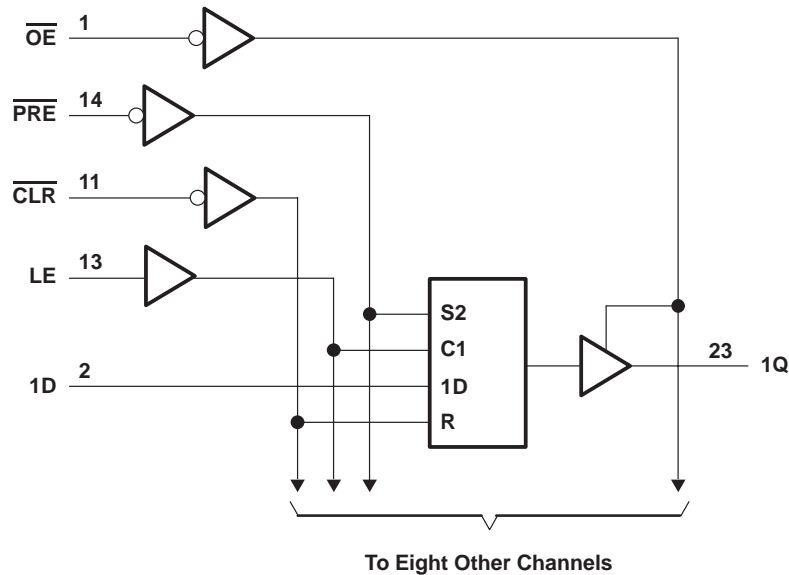


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DW, JT, NT, and W packages.

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**logic diagram (positive logic)**



Pin numbers shown are for the DB, DW, JT, NT, and W packages.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$ .....	-0.5 V to 5.5 V
Current into any output in the low state, $I_O$ : SN54ABT843 .....	96 mA
SN74ABT843 .....	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package .....	104°C/W
DW package .....	81°C/W
NT package .....	67°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.



# SN54ABT843, SN74ABT843

## 9-BIT BUS-INTERFACE D-TYPE LATCHES

### WITH 3-STATE OUTPUTS

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#### recommended operating conditions (see Note 3)

		SN54ABT843		SN74ABT843		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		-24		-32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
$T_A$	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54ABT843		SN74ABT843		UNIT
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$			-1.2		-1.2		-1.2	V
$V_{OH}$	$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -3\text{ mA}$	2.5			2.5		2.5		V
	$V_{CC} = 5\text{ V}$ , $I_{OH} = -3\text{ mA}$	3			3		3		
	$V_{CC} = 4.5\text{ V}$				2			2	
$V_{OL}$	$V_{CC} = 4.5\text{ V}$					0.55			V
					0.55*			0.55	
$V_{hys}$			100						mV
$I_I$	$V_{CC} = 5.5\text{ V}$ , $V_I = V_{CC}$ or GND			$\pm 1$		$\pm 1$		$\pm 1$	$\mu\text{A}$
$I_{OZH}^\ddagger$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.7\text{ V}$			10		10		10	$\mu\text{A}$
$I_{OZL}^\ddagger$	$V_{CC} = 5.5\text{ V}$ , $V_O = 0.5\text{ V}$			-10		-10		-10	$\mu\text{A}$
$I_{off}$	$V_{CC} = 0$ , $V_I$ or $V_O \leq 4.5\text{ V}$			$\pm 100$				$\pm 100$	$\mu\text{A}$
$I_{CEX}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 5.5\text{ V}$			50		50		50	$\mu\text{A}$
$I_{O\S}^\S$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.5\text{ V}$	-50	-140	-180	-50	-180	-50	-180	mA
$I_{CC}$	$V_{CC} = 5.5\text{ V}$ , $I_O = \text{Open}$ , $V_I = V_{CC}$ or GND	Outputs high	1	250		250		250	$\mu\text{A}$
		Outputs low	24	34		34		34	mA
		Outputs disabled	0.5	250		250		250	$\mu\text{A}$
$\Delta I_{CC}^\parallel$	$V_{CC} = 5.5\text{ V}$ , One input at 3.4 V, Other inputs at $V_{CC}$ or GND			1.5		1.5		1.5	mA
$C_i$	$V_I = 2.5\text{ V}$ or $0.5\text{ V}$			4					pF
$C_o$	$V_O = 2.5\text{ V}$ or $0.5\text{ V}$			7					pF

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at  $V_{CC} = 5\text{ V}$ .

‡ The parameters  $I_{OZH}$  and  $I_{OZL}$  include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.



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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figures 1 and 2)

		$V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$		SN54ABT843		SN74ABT843		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	$\overline{\text{CLR}}$ low		5.5	5.5	5.5	5.5	ns
		$\overline{\text{PRE}}$ low		4.5	4.5	4.5	4.5	
		LE low		3.3	3.3	3.4	3.4	
$t_{su}$	Setup time	Data before LE $\downarrow$	Low	2.5	2.5	2.5	2.5	ns
			High	3	3	3	3	
		$\overline{\text{PRE}}$ inactive		1.6	1.6	1.6	1.6	
		$\overline{\text{CLR}}$ inactive		2	2	2	2	
$t_h$	Hold time, data after LE $\downarrow$	High		1	1	1	1	ns
		Low		1.5 $\dagger$	2.3 $\dagger$	1.5 $\dagger$	1.5 $\dagger$	

$\dagger$  This data sheet limit may vary among suppliers.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figures 1 and 2)

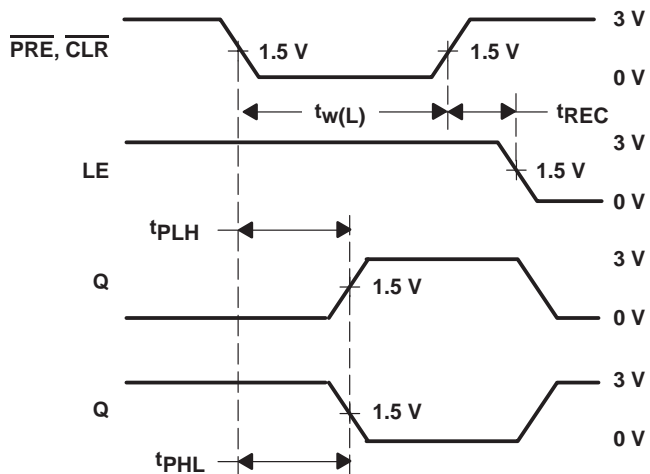
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$			SN54ABT843		SN74ABT843		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	D	Q	1.2 $\dagger$	3.8	5.2	1.2 $\dagger$	7.8	1.2 $\dagger$	6.7 $\dagger$	ns
$t_{PHL}$			1.5 $\dagger$	3.4	6.3	1.5 $\dagger$	7.3	1.5 $\dagger$	7.2	
$t_{PLH}$	LE	Q	1.7 $\dagger$	4.4	5.6	1.7 $\dagger$	8.3	1.7 $\dagger$	7.2 $\dagger$	ns
$t_{PHL}$			1.9 $\dagger$	4.1	6.3	1.3 $\dagger$	7.2	1.9 $\dagger$	6.9	
$t_{PLH}$	$\overline{\text{PRE}}$	Q	2.2	5	6.2	2.2	8.3	2.2	7.4	ns
$t_{PHL}$			2.1 $\dagger$	4.1	6.5	2.1 $\dagger$	7.5	2.1 $\dagger$	7.2	
$t_{PLH}$	$\overline{\text{CLR}}$	Q	2 $\dagger$	4.4	6.3	2 $\dagger$	7.6	2 $\dagger$	7.1	ns
$t_{PHL}$			1.9 $\dagger$	4.5	6.8	1.9 $\dagger$	8.1	1.9 $\dagger$	8	
$t_{PZH}$	$\overline{\text{OE}}$	Q	1	3.4	4.5 $\dagger$	1	6.4	1	5.7 $\dagger$	ns
$t_{PZL}$			2	4.3	5.7 $\dagger$	2	6.6	2	6.5	
$t_{PHZ}$	$\overline{\text{OE}}$	Q	2.4 $\dagger$	4.9	6.2	2.4 $\dagger$	7.3	2.4 $\dagger$	6.8	ns
$t_{PLZ}$			1.5 $\dagger$	4.2	6.3	1.5 $\dagger$	7	1.5 $\dagger$	5.9 $\dagger$	

$\dagger$  This data sheet limit may vary among suppliers.

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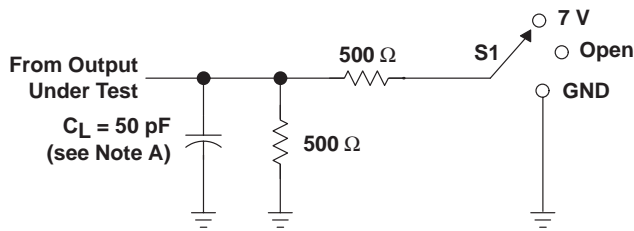
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**recovery-time waveform**



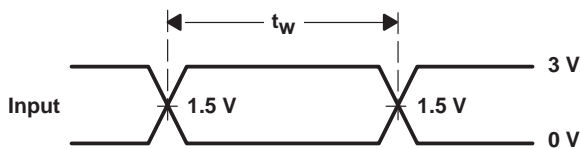
**Figure 1.  $\overline{\text{CLR}}$  and  $\overline{\text{PRE}}$  Pulse Duration,  $\overline{\text{CLR}}$  and  $\overline{\text{PRE}}$  to Output Delay, and  $\overline{\text{CLR}}$  and  $\overline{\text{PRE}}$  to Latch-Enable Recovery Time**

PARAMETER MEASUREMENT INFORMATION

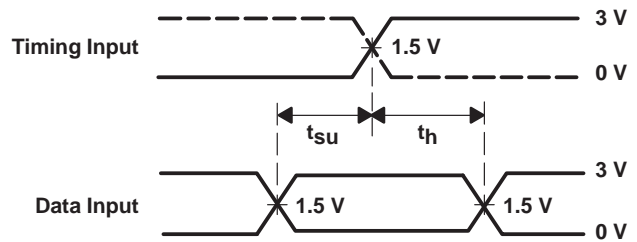


LOAD CIRCUIT

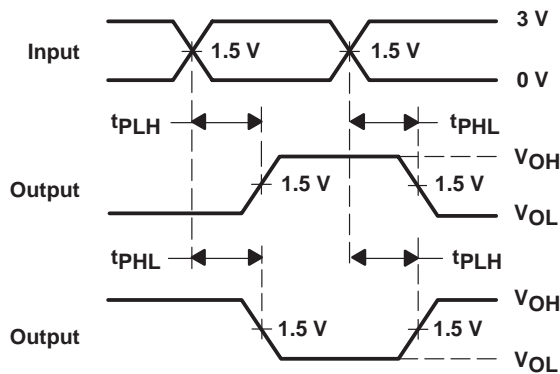
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



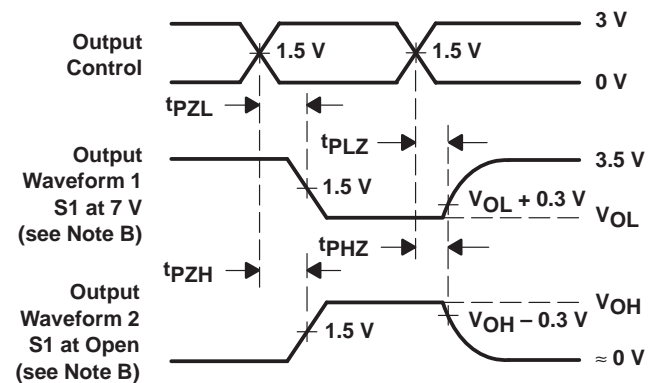
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9571201Q3A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9571201QKA	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type
5962-9571201QLA	ACTIVE	CDIP	JT	24	1	TBD	A42 SNPB	N / A for Pkg Type
SN74ABT843DBLE	OBSOLETE	SSOP	DB	24		TBD	Call TI	Call TI
SN74ABT843DBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPD	Level-1-260C-UNLIM
SN74ABT843DBRE4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPD	Level-1-260C-UNLIM
SN74ABT843DBRG4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPD	Level-1-260C-UNLIM
SN74ABT843DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT843DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT843DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT843DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT843DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT843DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT843NSR	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT843NSRE4	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT843NSRG4	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT843NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ABT843NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SNJ54ABT843FK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54ABT843JT	ACTIVE	CDIP	JT	24	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54ABT843W	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and



package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT843DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74ABT843DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74ABT843NSR	SO	NS	24	2000	330.0	24.4	8.2	15.4	2.5	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT843DBR	SSOP	DB	24	2000	346.0	346.0	33.0
SN74ABT843DWR	SOIC	DW	24	2000	346.0	346.0	41.0
SN74ABT843NSR	SO	NS	24	2000	346.0	346.0	41.0

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 10/96

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

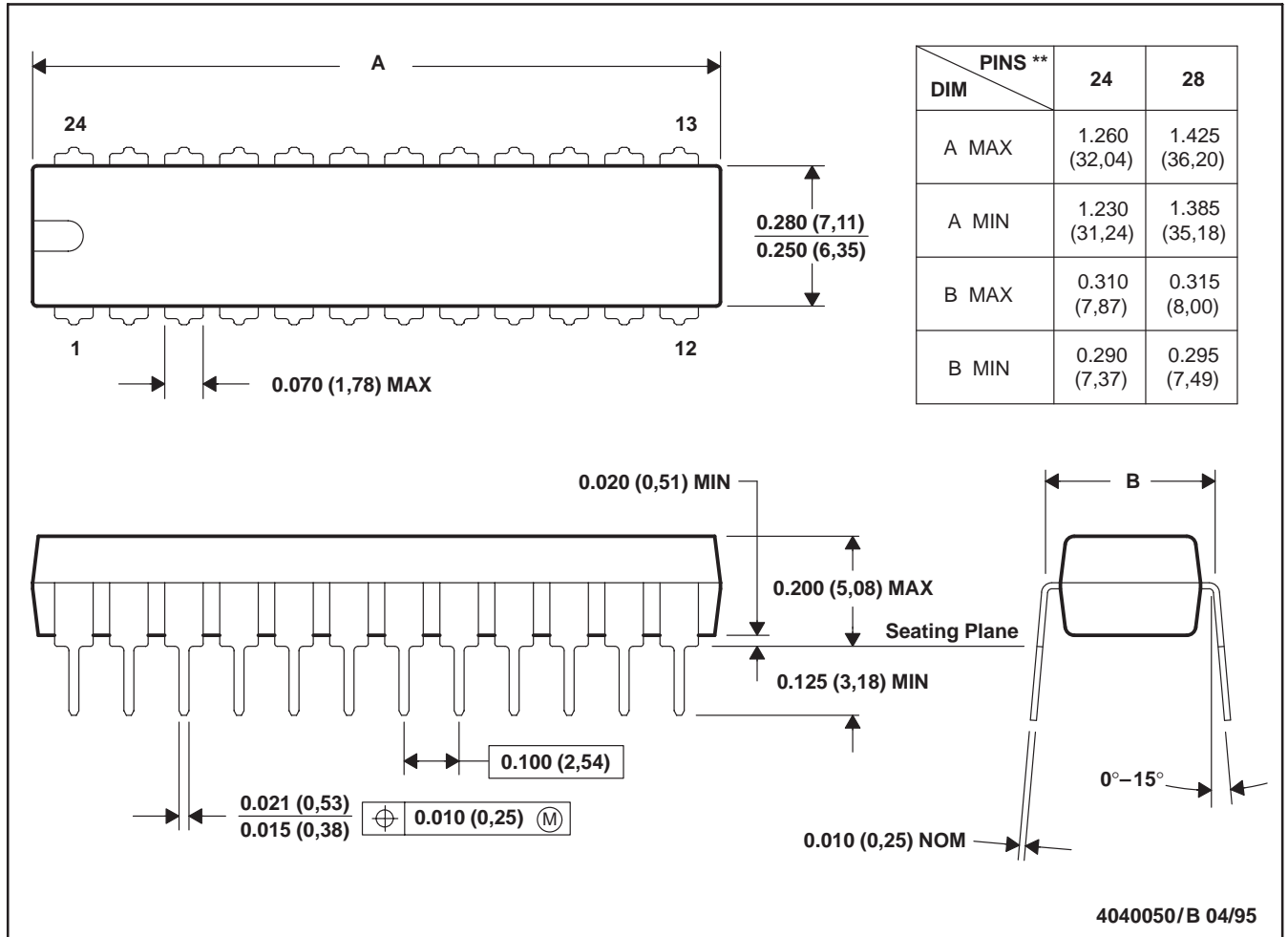


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

NT (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

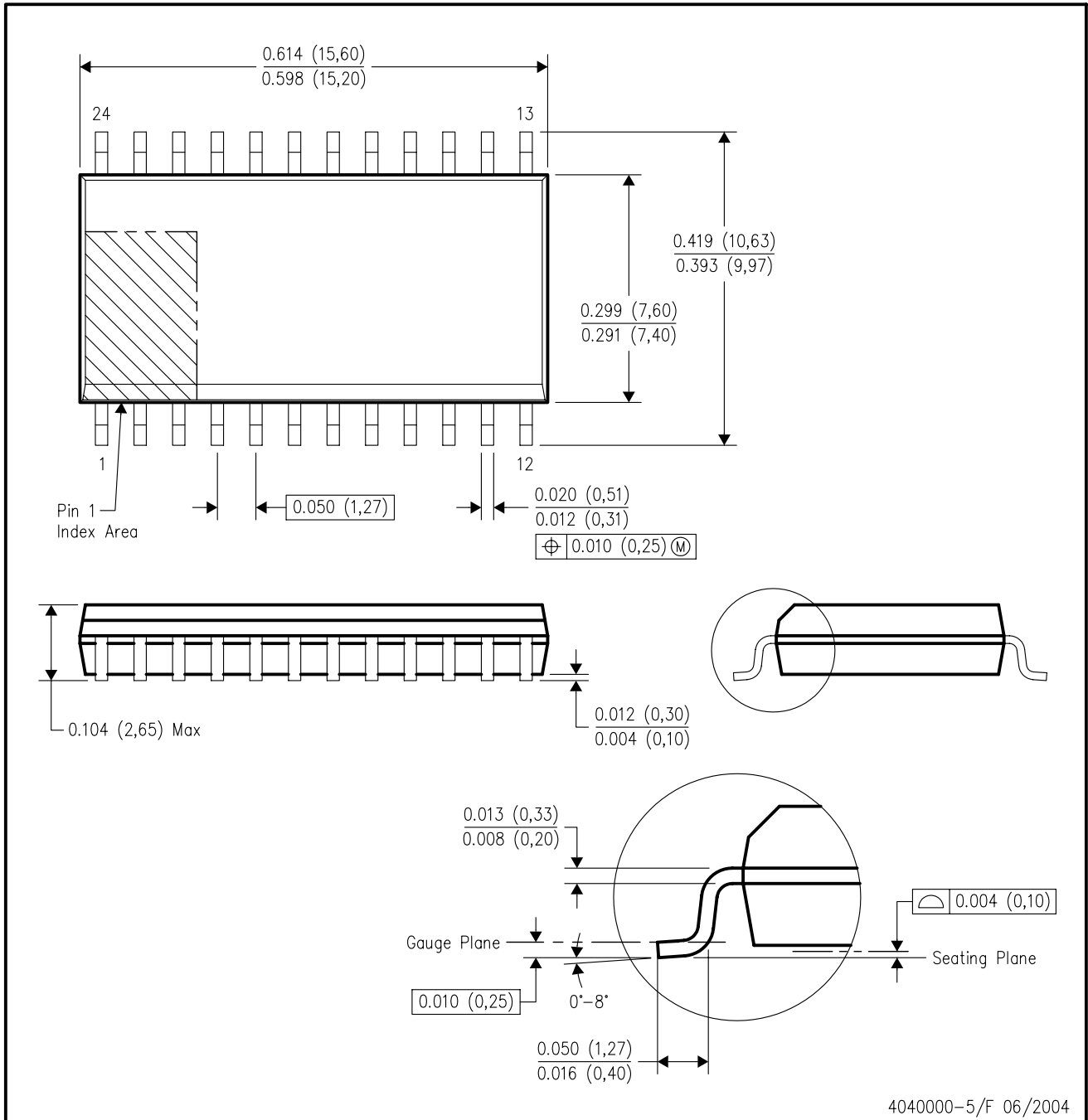
24 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

DW (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE

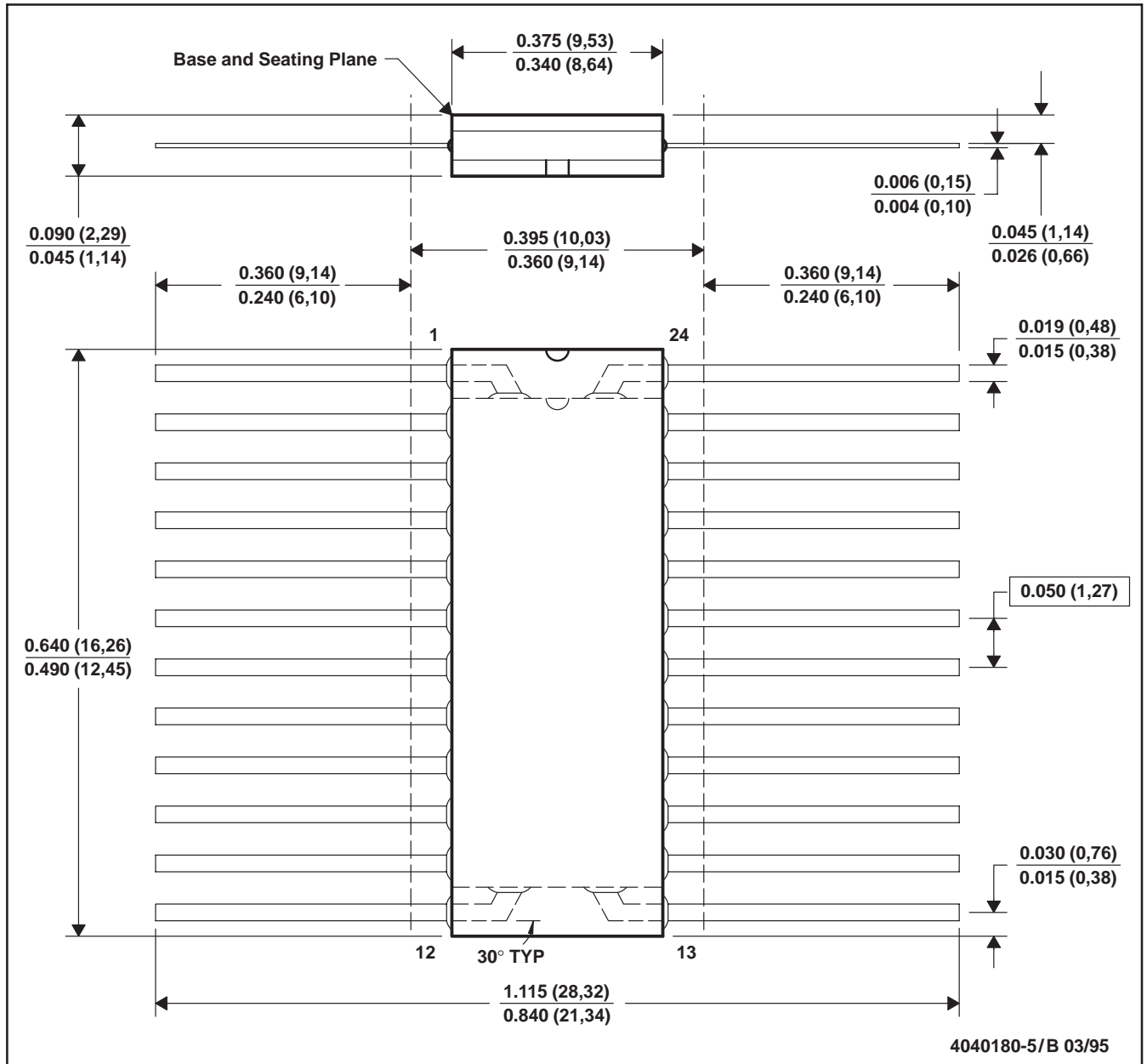


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.



W (R-GDFP-F24)

CERAMIC DUAL FLATPACK

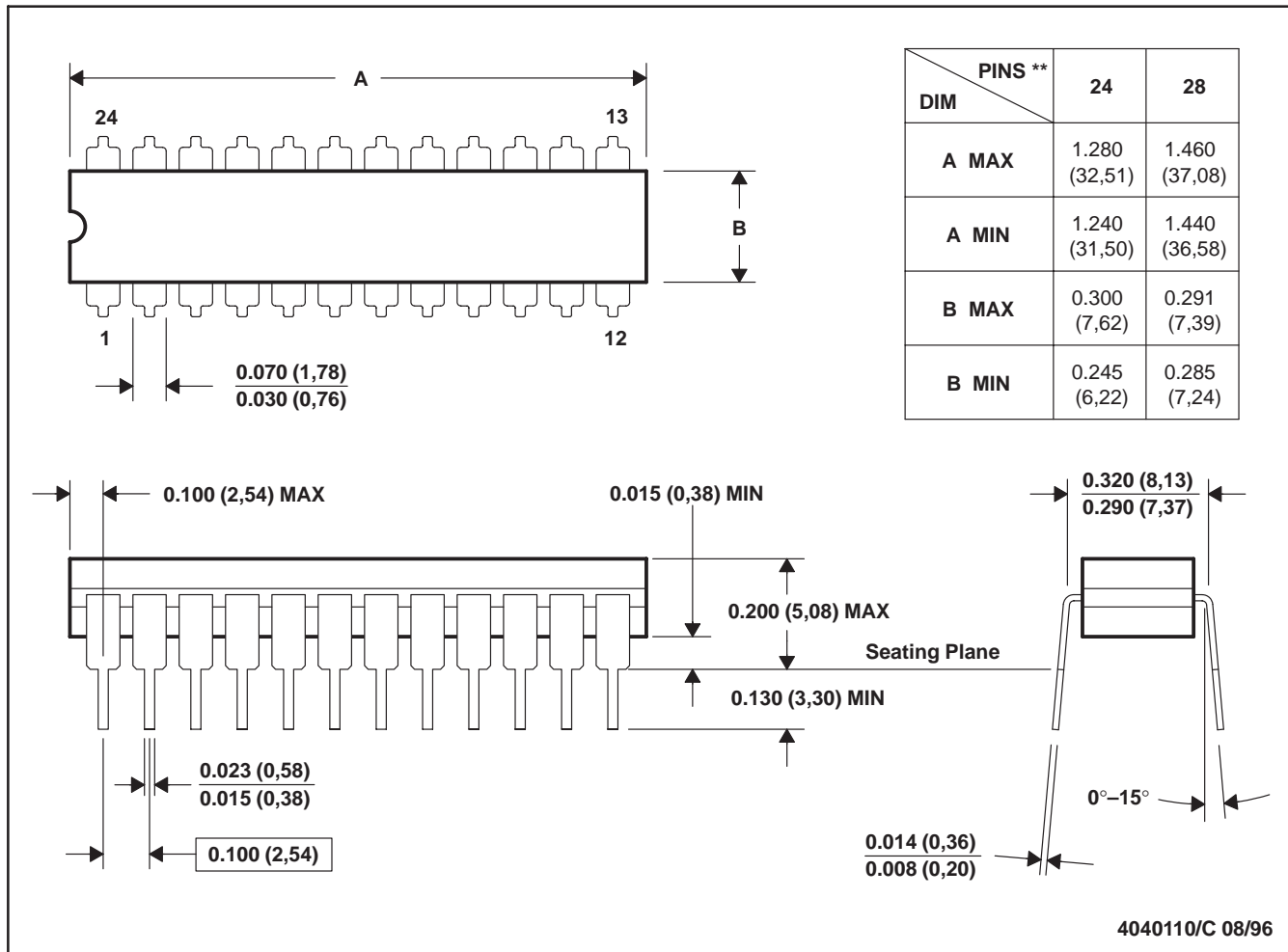


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD  
 E. Index point is provided on cap for terminal identification only.

JT (R-GDIP-T\*\*)

CERAMIC DUAL-IN-LINE

24 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification.  
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

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