18-Bit SoftSpan I_{OUT} DAC with Parallel I/O

FEATURES

- **Maximum 18-Bit INL Error: ±1 LSB Over Temperature**
- **Program or Pin-Strap Six Output Ranges: 0V to 5V, 0V to 10V, –2.5V to 7.5V, ±2.5V, ±5V, ±10V**
- **Guaranteed Monotonic Over Temperature**
- **Low Glitch Impulse 1.4nV•s (3V), 3nV•s (5V)**
- **18-Bit Settling Time: 2.1µs**
- 2.7V to 5.5V Single Supply Operation
- Reference Current Constant for All Codes
- Voltage-Controlled Offset and Gain Trims
- Parallel Interface with Readback of All Registers
- Clear and Power-On-Reset to 0V Regardless of Output Range
- 48-Pin 7mm × 7mm LQFP Package

APPLICATIONS

- Instrumentation
- Medical Devices
- Automatic Test Equipment
- Process Control and Industrial Automation

DESCRIPTION

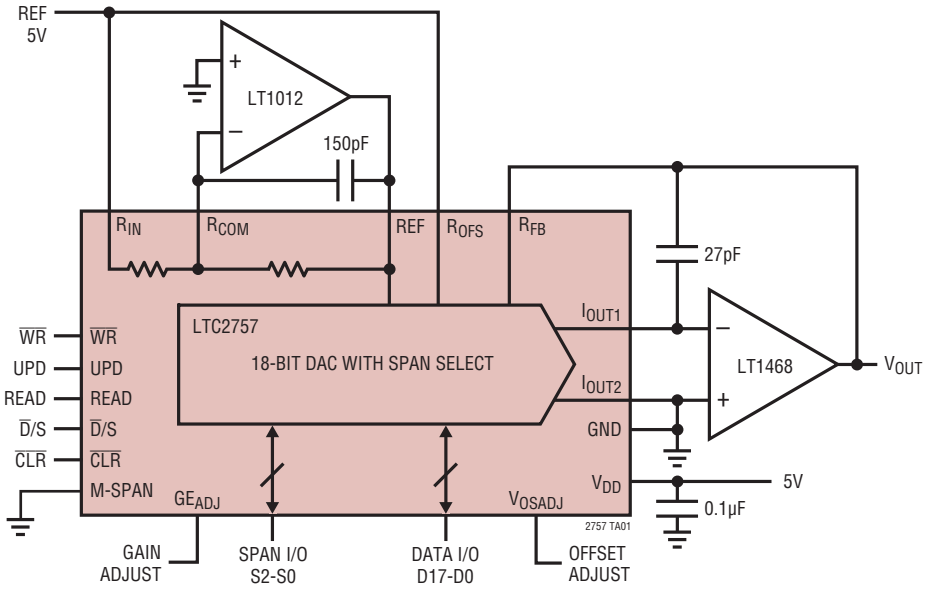
The LTC®2757 is an 18-bit multiplying parallel-input, current-output digital-to-analog converter that provides full 18-bit performance—INL and DNL of ±1LSB maximum—over temperature without any adjustments. 18-bit monotonicity is guaranteed in all performance grades. This SoftSpan™ DAC operates from a single 3V to 5V supply and offers six output ranges (up to ±10V) that can be programmed through the parallel interface or pin-strapped for operation in a single range.

In addition to its precision DC specifications, the LTC2757 also offers excellent AC specifications, including 2.1µs full-scale settling to 1LSB and 1.4nV•s glitch impulse.

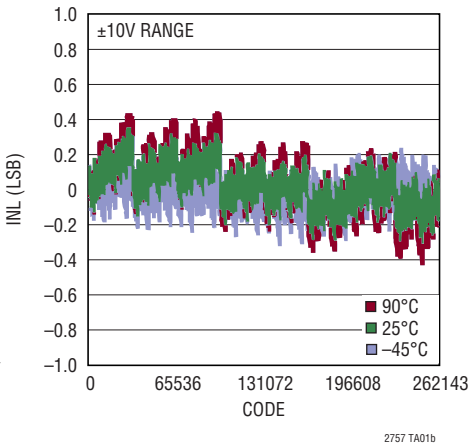
The LTC2757 uses a bidirectional input/output parallel interface that allows readback of any on-chip register, including DAC output-range settings; and a $\overline{CLR}$ pin and power-on reset circuit that each reset the DAC output to 0V regardless of output range.

TYPICAL APPLICATION

18-Bit Voltage Output DAC with Software-Selectable Ranges



LTC2757 Integral Nonlinearity

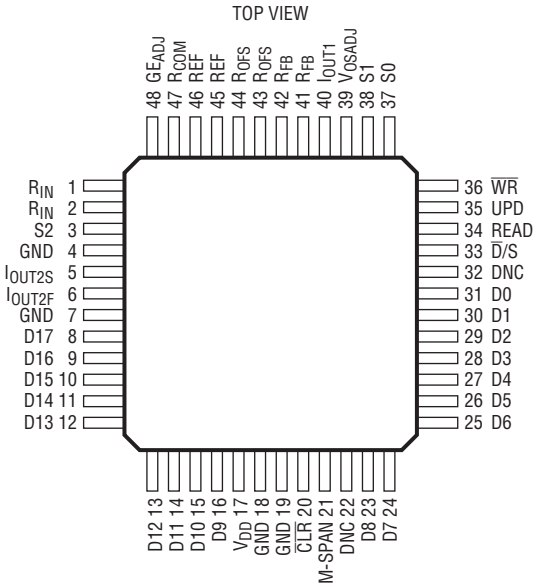


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

I_{OUT1}, I_{OUT2}, R_{COM} to GND ..... ±0.3V
R_{FB}, R_{OFS}, R_{IN}, REF, V_{OSADJ}, GE_{ADJ} to GND ..... ±15V
V_{DD} to GND ..... –0.3V to 7V
S2, S1, S0,
D17-D0 to GND ..... –0.3V to V_{DD} + 0.3V (7V Max)
$\overline{WR}$, UPD, $\overline{D}$/S, READ,
M-SPAN, $\overline{CLR}$ to GND ..... –0.3V to 7V
Operating Temperature Range
LTC2757C ..... 0°C to 70°C
LTC2757I ..... –40°C to 85°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



LX PACKAGE
48-LEAD (7mm × 7mm) PLASTIC LQFP

T_{JMAX} = 150°C, θ_{JA} = 53°C/W

ORDER INFORMATION

LEAD FREE FINISH	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2757BCLX#PBF	LTC2757LX	48-Lead (7mm × 7mm) Plastic LQFP	0°C to 70°C
LTC2757BILX#PBF	LTC2757LX	48-Lead (7mm × 7mm) Plastic LQFP	–40°C to 85°C
LTC2757ACLX#PBF	LTC2757LX	48-Lead (7mm × 7mm) Plastic LQFP	0°C to 70°C
LTC2757AILX#PBF	LTC2757LX	48-Lead (7mm × 7mm) Plastic LQFP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, V(R_{IN}) = 5V unless otherwise specified. The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		LTC2757B MIN	LTC2757B TYP	LTC2757B MAX	LTC2757A MIN	LTC2757A TYP	LTC2757A MAX	UNITS
Static Performance										
	Resolution		●	18			18			Bits
	Monotonicity		●	18			18			Bits
DNL	Differential Nonlinearity		●			±1		±0.4	±1	LSB
INL	Integral Nonlinearity		●			±2		±0.4	±1	LSB
GE	Gain Error	GE_{ADJ}: 0V, All Output Ranges	●			±48		±5	±32	LSB
GE_{TC}	Gain Error Temperature Coefficient	(Note 3)			±0.25			±0.25		ppm/°C
BZE	Bipolar Zero Error	All Bipolar Ranges	●			±36		±3	±24	LSB
BZS_{TC}	Bipolar Zero Temperature Coefficient	(Note 3)			±0.15			±0.15		ppm/°C
PSR	Power Supply Rejection	V_{DD} = 5V, ±10% V_{DD} = 3V, ±10%	● ●			±1.6 ±4		±0.15 ±0.4	±0.8 ±2	LSB/V
I_{LKG}	I_{OUT1} Leakage Current	T_A = 25°C T_{MIN} to T_{MAX}	 ●		±0.05	±2 ±5		±0.05	±2 ±5	nA

V_{DD} = 5V, V(R_{IN}) = 5V unless otherwise specified. The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Analog Pins							
R1, R2	Reference Inverting Resistors	(Note 4)	●	16	20		kΩ
R_{REF}	DAC Input Resistance	(Note 5)	●	8	10		kΩ
R_{FB}	Feedback Resistor	(Note 6)	●	8	10		kΩ
R_{OFS}	Bipolar Offset Resistor	(Note 6)	●	16	20		kΩ
R_{VOSADJ}	Offset Adjust Resistor		●	1024	1280		kΩ
R_{GEADJ}	Gain Adjust Resistor		●	2048	2560		kΩ
C_{IOUT1}	Output Capacitance	Full-Scale Zero-Scale			90 40		pF pF
Dynamic Performance							
	Output Settling Time	Span Code = 000, 10V Step (Note 7) To ±0.0004% FS			2.1		µs
	Glitch Impulse	V_{DD} = 5V (Note 8) V_{DD} = 3V (Note 8)			3 1.4		nV•s nV•s
	Digital-to-Analog Glitch Impulse	V_{DD} = 5V (Note 9) V_{DD} = 3V (Note 9)			4 1.8		nV•s nV•s
	Reference Multiplying Bandwidth	0V to 5V Range, Code = Full-Scale, –3dB Bandwidth			1		MHz
	Multiplying Feedthrough Error	0V to 5V Range, V_{REF} = ±10V, 10kHz Sine Wave			0.4		mV
THD	Total Harmonic Distortion	(Note 10) Multiplying			–110		dB
	Output Noise Voltage Density	(Note 11) at I_{OUT1}			13		nV/√Hz

ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, V(R_{IN}) = 5V unless otherwise specified. The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
V_{DD}	Supply Voltage		●	2.7		5.5	V
I_{DD}	Supply Current, V_{DD}	Digital Inputs = 0V or V_{DD}	●		0.5	1	µA
Digital Inputs							
V_{IH}	Digital Input High Voltage	3.3V ≤ V_{DD} ≤ 5.5V 2.7V ≤ V_{DD} < 3.3V	● ●	2.4 2			V V
V_{IL}	Digital Input Low Voltage	4.5V < V_{DD} ≤ 5.5V 2.7V ≤ V_{DD} ≤ 4.5V	● ●			0.8 0.6	V V
	Hysteresis Voltage				0.1		V
I_{IN}	Digital Input Current	V_{IN} = GND to V_{DD}	●			±1	µA
C_{IN}	Digital Input Capacitance	V_{IN} = 0V (Note 12)	●			6	pF
Digital Outputs							
V_{OH}	I_{OH} = 200µA		●	V_{DD} – 0.4			V
V_{OL}	I_{OL} = 200µA		●			0.4	V

TIMING CHARACTERISTICS

V_{DD} = 5V, V(R_{IN}) = 5V unless otherwise specified. The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} = 4.5V to 5.5V							
Write and Update Timing							
t_1	I/O Valid to $\overline{WR}$ Rising Edge Set-Up		●	9			ns
t_2	I/O Valid to $\overline{WR}$ Rising Edge Hold		●	9			ns
t_3	$\overline{WR}$ Pulse Width		●	20			ns
t_4	UPD Pulse Width		●	20			ns
t_5	UPD Falling Edge to $\overline{WR}$ Falling Edge	No Data Shoot-Through	●	0			ns
t_6	$\overline{WR}$ Rising Edge to UPD Rising Edge	(Note 12)	●	0			ns
t_7	$\overline{D}$/S Valid to $\overline{WR}$ Falling Edge Set-Up Time		●	9			ns
t_8	$\overline{WR}$ Rising Edge to $\overline{D}$/S Valid Hold Time		●	9			ns
Readback Timing							
t_{13}	$\overline{WR}$ Rising Edge to READ Rising Edge		●	9			ns
t_{14}	READ Falling Edge to $\overline{WR}$ Falling Edge	(Note 12)	●	20			ns
t_{15}	READ Rising Edge to I/O Propagation Delay	C_L = 10pF	●			30	ns
t_{17}	UPD Valid to I/O Propagation Delay	C_L = 10pF	●			30	ns
t_{18}	$\overline{D}$/S Valid to READ Rising Edge	(Note 12)	●	9			ns
t_{19}	READ Rising Edge to UPD Rising Edge	No Update	●	9			ns
t_{20}	UPD Falling Edge to READ Falling Edge	No Update	●	9			ns
t_{22}	READ Falling Edge to UPD Rising Edge	(Note 12)	●	9			ns
t_{23}	I/O Bus Hi-Z to READ Rising Edge	(Note 12)	●	0			ns
t_{24}	READ Falling Edge to I/O Bus Active	(Note 12)	●	20			ns

TIMING CHARACTERISTICS

V_{DD} = 5V, V(R_{IN}) = 5V unless otherwise specified. The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{CLR}$ Timing							
t_{25}	$\overline{CLR}$ Pulse Width Low		●	20			ns
V_{DD} = 2.7V to 3.3V							
Write and Update Timing							
t_1	I/O Valid to $\overline{WR}$ Rising Edge Set-Up		●	18			ns
t_2	I/O Valid to $\overline{WR}$ Rising Edge Hold		●	18			ns
t_3	$\overline{WR}$ Pulse Width		●	30			ns
t_4	UPD Pulse Width		●	30			ns
t_5	UPD Falling Edge to $\overline{WR}$ Falling Edge	No Data Shoot-Through	●	0			ns
t_6	$\overline{WR}$ Rising Edge to UPD Rising Edge	(Note 12)	●	0			ns
t_7	$\overline{D}$/S Valid to $\overline{WR}$ Falling Edge Set-Up Time		●	18			ns
t_8	$\overline{WR}$ Rising Edge to $\overline{D}$/S Valid Hold Time		●	18			ns
Readback Timing							
t_{13}	$\overline{WR}$ Rising Edge to Read Rising Edge		●	18			ns
t_{14}	Read Falling Edge to $\overline{WR}$ Falling Edge	(Note 12)	●	40			ns
t_{15}	Read Rising Edge to I/O Propagation Delay	C_L = 10pF	●			48	ns
t_{17}	UPD Valid to I/O Propagation Delay	C_L = 10pF	●			48	ns
t_{18}	$\overline{D}$/S Valid to Read Rising Edge	(Note 12)	●	18			ns
t_{19}	Read Rising Edge to UPD Rising Edge	No Update	●	9			ns
t_{20}	UPD Falling Edge to Read Falling Edge	No Update	●	9			ns
t_{22}	READ Falling Edge to UPD Rising Edge	(Note 12)	●	18			ns
t_{23}	I/O Bus Hi-Z to Read Rising Edge	(Note 12)	●	0			ns
t_{24}	Read Falling Edge to I/O Bus Active	(Note 12)	●	40			ns
$\overline{CLR}$ Timing							
t_{25}	$\overline{CLR}$ Pulse Width Low		●	30			ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 3: Temperature Coefficient is calculated by dividing the maximum change in the parameter by the specified temperature range.

Note 4: R1 is measured from R_{IN} to R_{COM}; R2 is measured from REF to R_{COM}.

Note 5: Parallel combination of the resistances from REF to I_{OUT1} and from REF to I_{OUT2}. DAC input resistance is independent of code.

Note 6: Because of the proprietary SoftSpan switching architecture, the measured resistance looking into each of the specified pins is constant for all output ranges if the I_{OUT1} and I_{OUT2} pins are held at ground.

Note 7: Using LT1468 with $C_{FEEDBACK}$ = 27pF. A ±0.0004% settling time of 1.8µs can be achieved by optimizing the time constant on an individual basis. See Application Note 120, *1ppm Settling Time Measurement for a Monolithic 18-Bit DAC*.

Note 8: Measured at the major carry transition, 0V to 5V range. Output amplifier: LT1468; C_{FB} = 50pF.

Note 9: Zero-code to full-code transition; REF = 0V. Falling transition is similar or better.

Note 10: REF = $6V_{RMS}$ at 1kHz. 0V to 5V range. DAC code = FS. Output amplifier = LT1468.

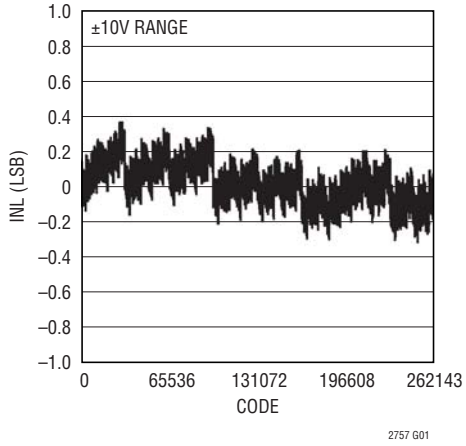
Note 11: Calculation from $V_n = \sqrt{4kTRB}$, where k = 1.38E-23 J/°K (Boltzmann constant), R = resistance (Ω), T = temperature (°K), and B = bandwidth (Hz).

Note 12: Guaranteed by design. Not production tested.

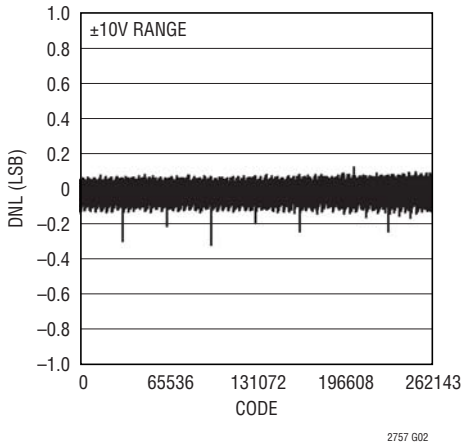
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 5V, V(R_{IN}) = 5V, T_A = 25°C, unless otherwise noted.

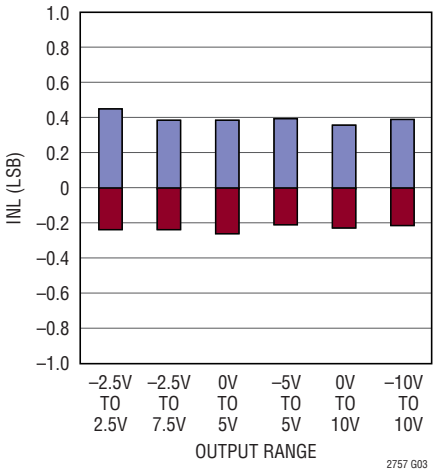
Integral Nonlinearity (INL)



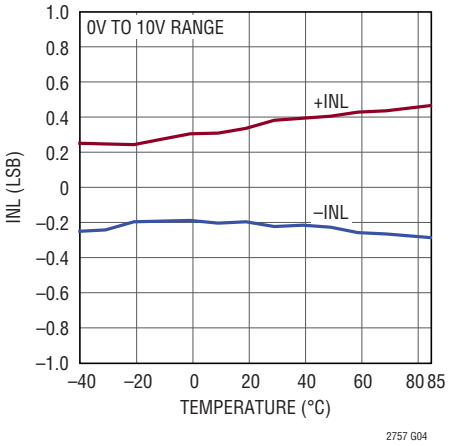
Differential Nonlinearity (DNL)



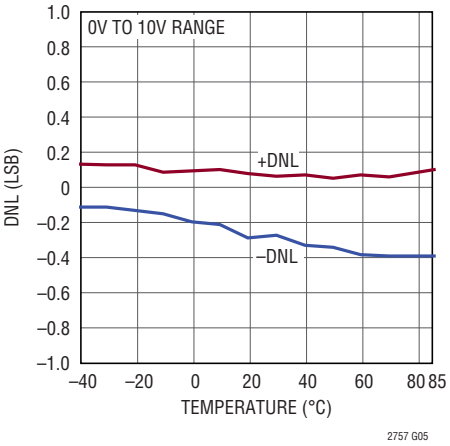
INL vs Output Range



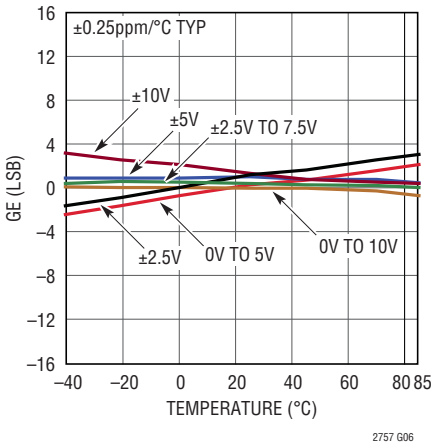
INL vs Temperature



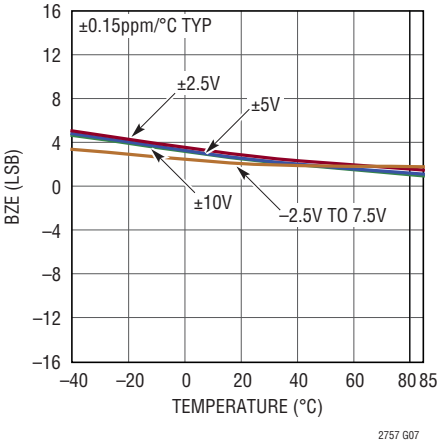
DNL vs Temperature



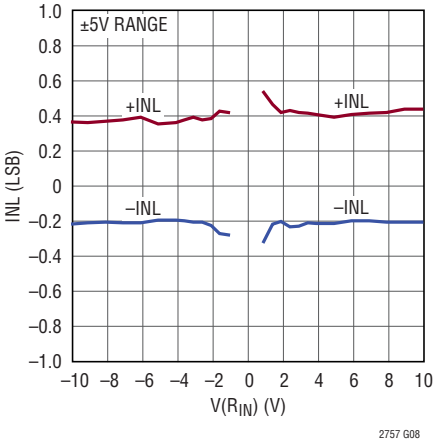
Gain Error vs Temperature



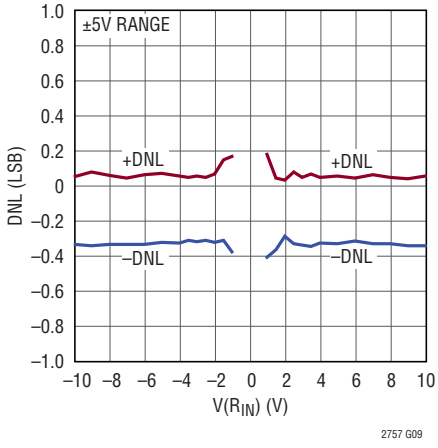
Bipolar Zero Error vs Temperature



INL vs Reference Voltage



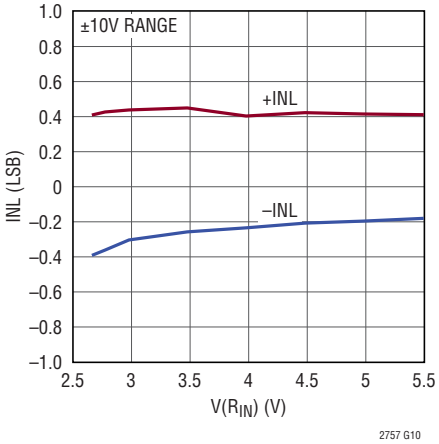
DNL vs Reference Voltage



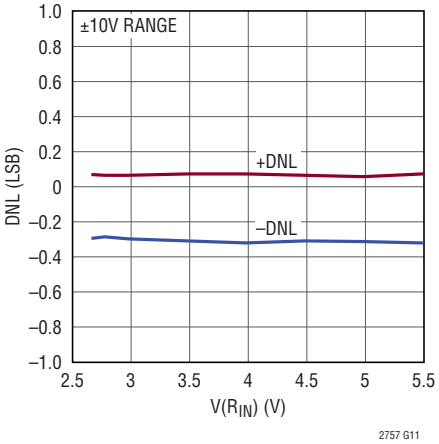
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 5V, V(R_{IN}) = 5V, T_A = 25°C, unless otherwise noted.

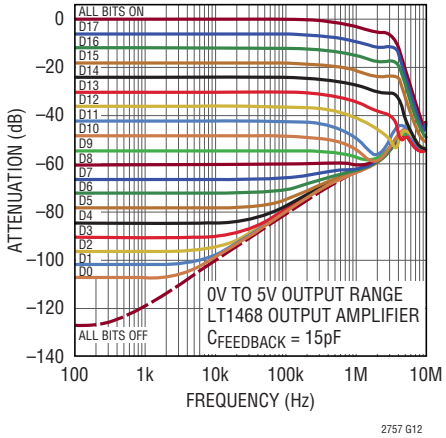
INL vs V_{DD}



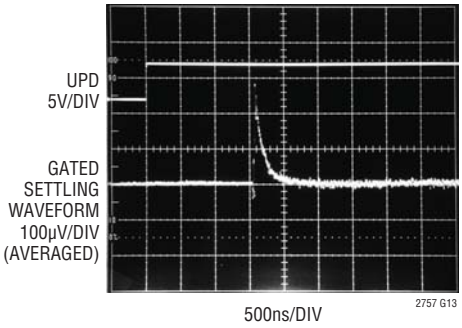
DNL vs V_{DD}



Multiplying Frequency Response vs Digital Code

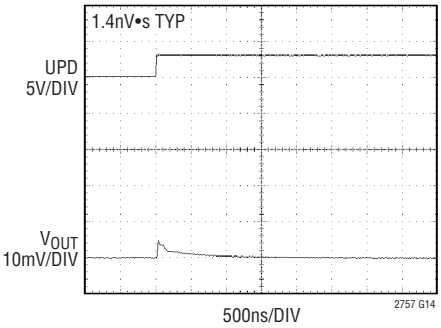


Settling Full-Scale Step



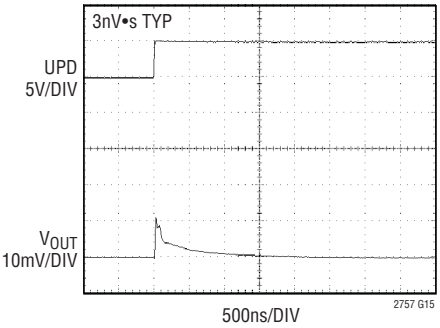
LT1468 AMP; $C_{FEEDBACK}$ = 20pF
0V TO 10V STEP
V_{REF} = –10V; SPAN CODE = 000
t_{SETTLE} = 1.8µs to 0.0004% (18 BITS)

Mid-Scale Glitch (V_{DD} = 3V)



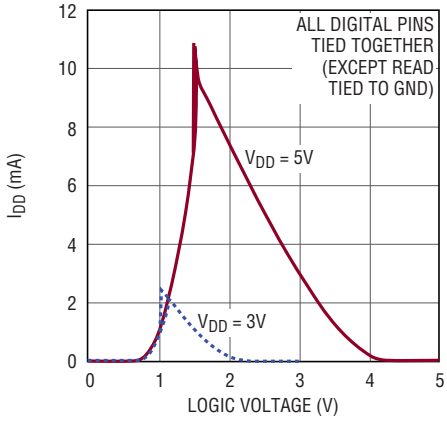
0V TO 5V RANGE
LT1468 OUTPUT AMPLIFIER
$C_{FEEDBACK}$ = 50pF
RISING MAJOR CARRY TRANSITION.
FALLING TRANSITION IS SIMILAR OR BETTER.

Mid-Scale Glitch (V_{DD} = 5V)

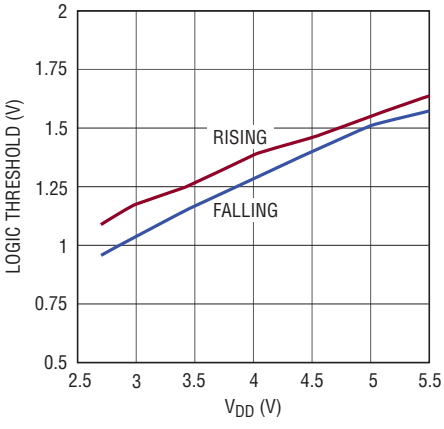


0V TO 5V RANGE
LT1468 OUTPUT AMPLIFIER
$C_{FEEDBACK}$ = 50pF
RISING MAJOR CARRY TRANSITION.
FALLING TRANSITION IS SIMILAR OR BETTER.

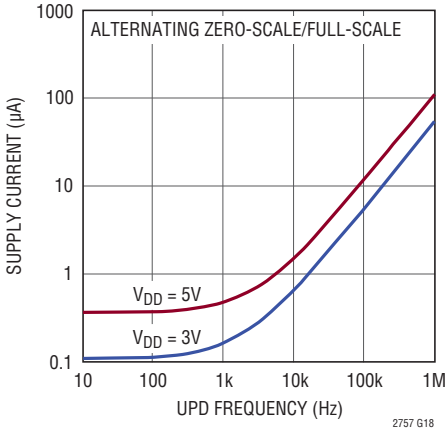
Supply Current vs Logic Input Voltage



Logic Threshold vs Supply Voltage



Supply Current vs Update Frequency



PIN FUNCTIONS

R_{IN} (Pins 1, 2): Input Resistor for External Reference Inverting Amplifier. Normally tied to the external reference voltage. Typically 5V; accepts up to ±15V. These pins are internally shorted together.

S2 (Pin 3): Span I/O Bit 2. Pins S0, S1 and S2 are used to program and to read back the output range of the DAC. See Table 2.

GND (Pins 4, 7, 18, 19): Ground. Tie to ground.

I_{OUT2S}, I_{OUT2F} (Pins 5, 6): DAC Output Current Complement Sense and Force Pins. Tie to ground via a clean, low-impedance path. These pins may also be used with a precision ground buffer amp as a Kelvin sensing pair (see the Typical Applications section).

D17-D9 (Pins 8-16): DAC Input/Output Data Bits. These I/O pins set and read back the DAC code. D17 (Pin 8) is the MSB.

V_{DD} (Pin 17): Positive Supply Input. $2.7V \leq V_{DD} \leq 5.5V$. Requires a 0.1µF bypass capacitor to GND.

$\overline{CLR}$ (Pin 20): Asynchronous Clear Input. When $\overline{CLR}$ is asserted low, the DAC output resets to V_{OUT} = 0V. The LTC2757 selects the appropriate reset code according to the active output range—zero-scale for 0V to 5V and 0V to 10V spans, half scale for ±2.5V, ±5V and ±10V spans, or quarter scale for –2.5V to 7.5V span.

M-SPAN (Pin 21): Manual Span Control Input. M-SPAN can be pin-strapped to configure the LTC2757 for operation in a single, fixed output range.

To configure the part for single-span use, tie M-SPAN directly to V_{DD}. The output range is then set via hardware pin strapping; and the Span I/O port ignores Write, Update and Read commands.

If M-SPAN is instead connected to ground (SoftSpan configuration), the output ranges are set and verified by using Write, Update and Read operations. See *Manual Span Configuration* in the Operation section. M-SPAN must be connected either directly to GND (for SoftSpan operation) or V_{DD} (for single-span operation).

DNC (Pins 22, 32): Do Not Connect.

D8-D0 (Pins 23-31): DAC Input/Output Data Bits. These I/O pins set and read back the DAC code. D0 is the LSB.

$\overline{D}$/S (Pin 33): Data/Span Select Input. This pin is used to select activation of the Data ($\overline{D}$/S = 0) or Span ($\overline{D}$/S = 1) Input I/O pins (D0 to D17 or S0 to S2, respectively), along with their respective dedicated registers, for Write or Read operations. Update operations are unaffected by $\overline{D}$/S, since all updates affect both Data and Span registers. For single-span operation, tie $\overline{D}$/S to GND.

READ (Pin 34): Read Input. When READ is asserted high, the Data I/O pins (D0-D17) or Span I/O pins (S0-S2) output the contents of a selected Input or DAC register (see Table 1). Data/Span ports are selected for readback with the $\overline{D}$/S pin; the Input/DAC registers within those ports are selected for readback with the UPD pin. The readback function of the Span I/O pins is disabled when M-SPAN is tied to V_{DD}.

UPD (Pin 35): Update/Register Select Input.

READ = low: Update function. When UPD is asserted high, the contents of the Input registers are copied into their respective DAC registers. The output of the DAC is updated, reflecting the new DAC register values.

READ = high: Register selector function. The Update function is disabled and the UPD pin functions as a register selector. UPD = low selects Input registers for readback, high selects DAC registers. See *Readback* in the Operation section.

$\overline{WR}$ (Pin 36): Active-Low Write Input. A Write operation copies the data present on the Data or Span I/O pins (D0-D17 or S0-S2, respectively) into the Input register. The Write function is disabled when READ is high.

S0 (Pin 37): Span I/O Bit 0. Pins S0, S1 and S2 are used to program and to read back the output range of the DAC. See Table 2.

S1 (Pin 38): Span I/O Bit 1. Pins S0, S1 and S2 are used to program and to read back the output range of the DAC. See Table 2.

PIN FUNCTIONS

V_{OSADJ} (Pin 39): DAC Offset Adjust Pin. This voltage-control pin can be used to null unipolar offset or bipolar zero error. The offset change expressed in LSB is the same for any output range. See *System Offset and Gain Adjustments* in the Operation section. Tie to ground if not used.

I_{OUT1} (Pin 40): DAC current output; normally tied to the negative input (summing junction) of the I/V converter amplifier.

R_{FB} (Pins 41, 42): DAC Feedback Resistor. Normally tied to the output of the I/V converter amplifier. The DAC output current from I_{OUT1} flows through the feedback resistor to the R_{FB} pins. These pins are internally shorted together.

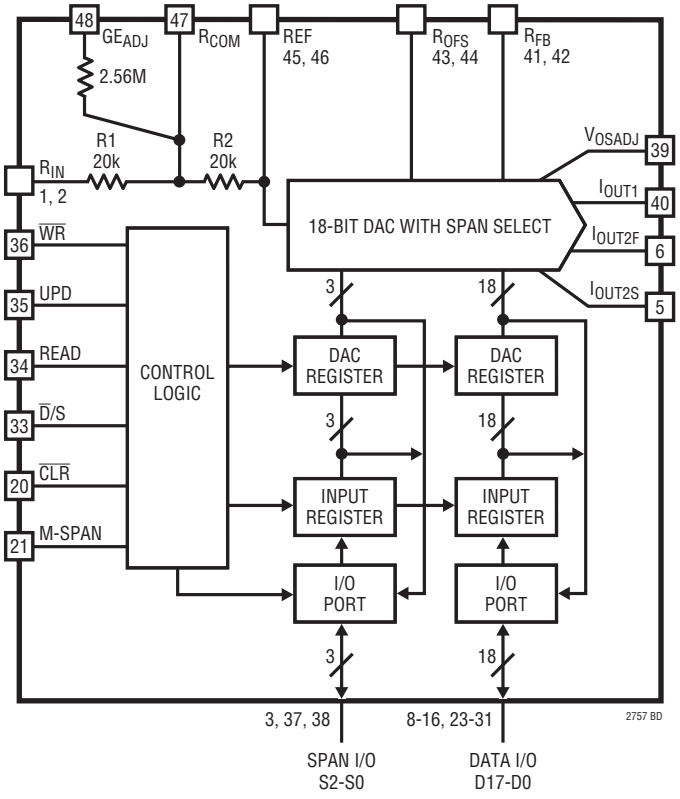
R_{OFS} (Pins 43, 44): Bipolar Offset Network. These pins provide the translation of the output voltage range for bipolar spans. Accepts up to ±15V; normally tied to the positive reference voltage. These pins are internally shorted together.

REF (Pins 45, 46): Feedback Resistor for the Reference Inverting Amplifier, and Reference Input for the DAC. Normally tied to the output of the reference inverting amplifier. Typically –5V; accepts up to ±15V. These pins are internally shorted together.

R_{COM} (Pin 47): Center Tap Point of R_{IN} and REF. Normally tied to the negative input of the external reference inverting amplifier.

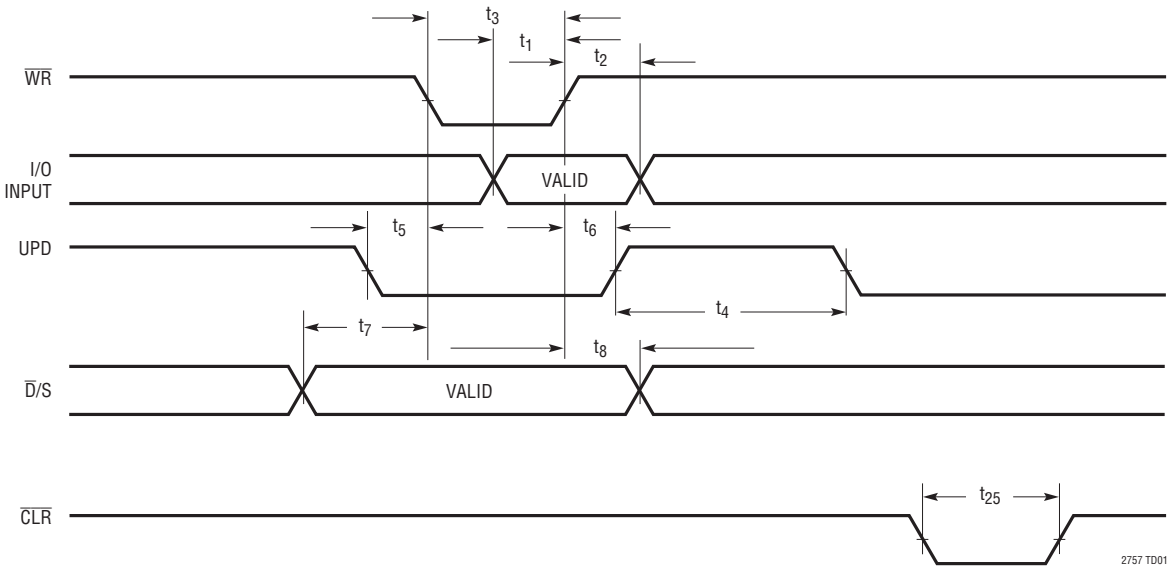
GE_{ADJ} (Pin 48): Gain Adjust Pin. This voltage-control pin can be used to null gain error or to compensate for reference errors. The gain error change expressed in LSB is the same for any output range. See *System Offset and Gain Adjustments* in the Operation section. Tie to ground if not used.

BLOCK DIAGRAM

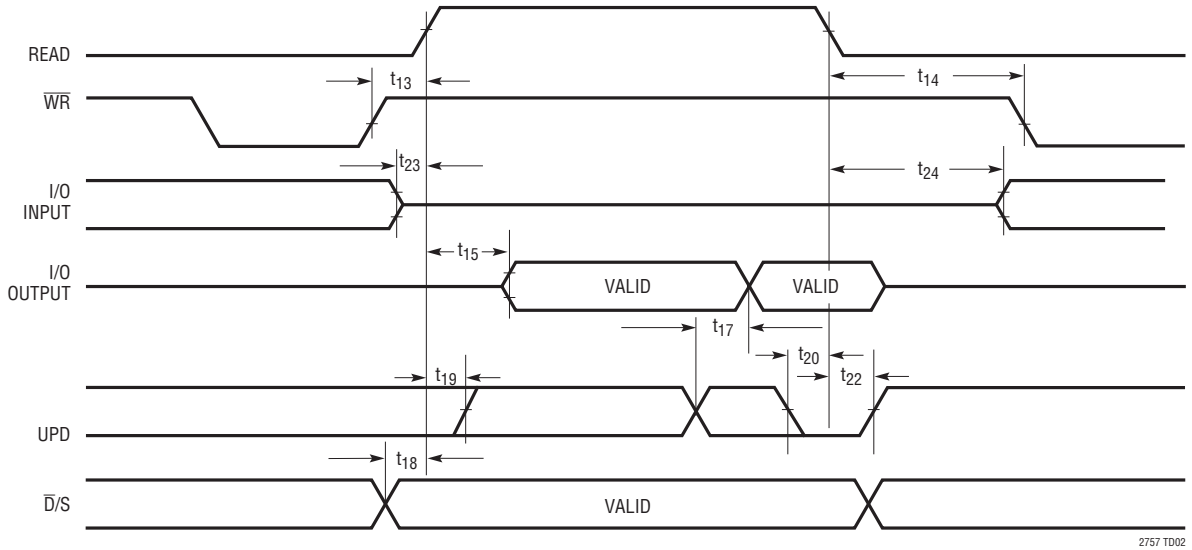


TIMING DIAGRAMS

Write, Update and Clear Timing



Readback Timing



OPERATION

Output Ranges

The LTC2757 is a current-output, parallel-input precision multiplying DAC offering ±1LSB INL and DNL over six software-selectable output ranges. Ranges can either be programmed in software for maximum flexibility or hardwired through pin-strapping. Two unipolar ranges are available (0V to 5V and 0V to 10V), and four bipolar ranges (±2.5V, ±5V, ±10V and –2.5V to 7.5V). These ranges are obtained when an external precision 5V reference is used. The output ranges for other reference voltages are easy to calculate by observing that each range is a multiple of the external reference voltage. The ranges can then be expressed: 0 to 1×, 0 to 2×, ±0.5×, ±1×, ±2×, and –0.5× to 1.5×.

Digital Section

The LTC2757 has four internal interface registers (see Block Diagram). Two of these—one Input and one DAC register—are dedicated to the Data I/O port, and two to the Span I/O port. Each port is thus double buffered. Double buffering provides the capability to simultaneously update the Span and Code registers, which allows smooth voltage transitions when changing output ranges. It also permits the simultaneous updating of multiple DACs or other parts on the data bus.

Write and Update Operations

Load the data input register directly from an 18-bit bus by holding the $\overline{D}$/S pin low and then pulsing the $\overline{WR}$ pin low (Write operation).

Load the Span Input register by holding the $\overline{D}$/S pin high and then pulsing the $\overline{WR}$ pin low (Write operation). The Span and Data register structures are the same except for the number of parallel bits—the Span registers have three bits, while the Data registers have 18 bits.

The DAC registers are loaded by pulsing the UPD pin high (Update operation), which copies the data held in the Input registers of both ports into the DAC registers. Note that Update operations always include both Data and Span registers; but the DAC register values will not change unless the Input register values have previously been changed by a Write operation.

To make both registers transparent for flowthrough mode, tie $\overline{WR}$ low and UPD high. However, this defeats the deglitcher operation and output glitch impulse may increase. The deglitcher is activated on the rising edge of the UPD pin.

The interface also allows the use of the Input and DAC registers in a master-slave, or edge-triggered, configuration. This mode of operation occurs when $\overline{WR}$ and UPD are tied together and driven by a single clock signal. The data bits are loaded into the Input register on the falling edge of the clock and then loaded into the DAC register on the rising edge.

It is possible to control both ports on one 18-bit wide data bus by allowing Span pins S2 to S0 to share bus lines with the Data LSBs (D2 to D0). No Write or Read operation acts on both span and data, so there cannot be a signal conflict.

The asynchronous clear pin ($\overline{CLR}$) resets the LTC2757 to 0V (zero-, half- or quarter-scale code) in any output range. $\overline{CLR}$ resets both the Input and DAC data registers, but leaves the Span registers unchanged.

The device also has a power-on reset that initializes the DAC to V_{OUT} = 0V in any output range. The DAC powers up in the 0V to 5V range at zero-scale if the part is in SoftSpan configuration. For manual span (M-SPAN tied to V_{DD}; see *Manual Span Configuration*), the DACs power-up in the manually-chosen range at the appropriate code.

Manual Span Configuration

Multiple output ranges are not needed in some applications. To configure the LTC2757 for single-span operation, tie the M-SPAN pin to V_{DD} and the $\overline{D}$/S pin to GND. The desired output range is programmed by tying S0, S1 and S2 to GND or V_{DD} (see Figure 1 and Table 2). In this configuration, no range-setting software routine is needed; the part will initialize to the chosen output range at power-up, with V_{OUT} = 0V.

When configured for manual span operation, Span port readback is disabled.

OPERATION

Readback

The contents of any one of the four interface registers can be read back from the I/O ports by using the READ pin in conjunction with the $\overline{D}$/S and UPD pins.

The I/O pins and registers are grouped into two ports—Data and Span. The Data I/O port consists of pins D0-D17, and the Span I/O port consists of pins S0, S1 and S2.

Each I/O port has one dedicated Input register and one dedicated DAC register. The register structure is shown in the Block Diagram.

A Readback operation is initiated by asserting READ to logic high after selecting the desired I/O port.

Select the I/O port (Data or Span) to be read back with the $\overline{D}$/S pin. The selected I/O port's pins become logic outputs during readback, while the unselected I/O port's pins remain high-impedance digital inputs.

With the I/O port selected, assert READ high and select the desired Input or DAC register using the UPD pin. Note that UPD is a two function pin—the Update function is only available when READ is low. If READ is high, the Update function is disabled and the UPD pin instead functions as a register selector, selecting an Input or DAC register for readback. Table 1 shows the readback functions for the LTC2757.

Table 1. Write, Update and Read Functions

READ	D/S	WR	UPD	SPAN I/O	DATA I/O
0	0	0	0	-	Write to Input Register
0	0	0	1	-	Write/Update (Transparent)
0	0	1	0	-	-
0	0	1	1	Update DAC Register	Update DAC Register
0	1	0	0	Write to Input Register	-
0	1	0	1	Write/Update (Transparent)	-
0	1	1	0	-	-
0	1	1	1	Update DAC register	Update DAC Register
1	0	X	0	-	Read Input Register
1	0	X	1	-	Read DAC Register
1	1	X	0	Read Input Register	-
1	1	X	1	Read DAC Register	-

X = Don't Care

The most common readback task is to check the contents of an Input register after writing to it, and before updating the new data to the DAC register. To do this, hold UPD low and assert READ high. The contents of the selected port's Input register are output to its I/O pins.

To read back the contents of a DAC register, hold UPD low and assert READ high, then bring UPD high to select the DAC register. The contents of the selected DAC register are output by the selected port's I/O pins. Note: if no update is desired after the readback operation, UPD must be returned low before bringing READ low, otherwise the UPD pin will revert to its primary function and update the DAC.

Table 2. Span Codes

S2	S1	S0	SPAN
0	0	0	Unipolar 0V to 5V
0	0	1	Unipolar 0V to 10V
0	1	0	Bipolar –5V to 5V
0	1	1	Bipolar –10V to 10V
1	0	0	Bipolar –2.5V to 2.5V
1	0	1	Bipolar –2.5V to 7.5V

Codes not shown are reserved and should not be used.

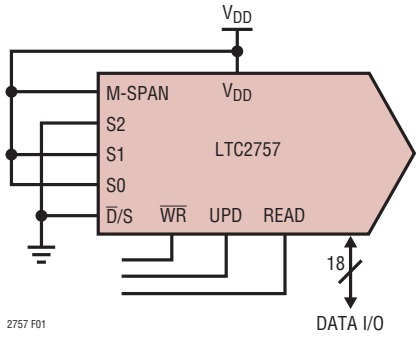


Figure 1. Configuring the LTC2757 for Single-Span Operation (±10V Range)

System Offset and Gain Adjustments

Many systems require compensation for overall system offset. This may be an order of magnitude or more greater than the offset of the LTC2757, which is so low as to be dominated by external output amplifier errors even when using the most precise op amps.

OPERATION

The offset adjust pin V_{OSADJ} can be used to null unipolar offset or bipolar zero error. The offset change expressed in LSB is the same for any output range:

$$\Delta V_{OS}[LSB] = \frac{-V(V_{OSADJ})}{V(R_{IN})} \bullet 2048$$

A 5V control voltage applied to V_{OSADJ} produces ΔV_{OS} = –2048 LSB in any output range, assuming a 5V reference voltage at R_{IN}.

In voltage terms, the offset delta is attenuated by a factor of 32, 64 or 128, depending on the output range. (These functions hold regardless of reference voltage.)

$\Delta V_{OS} = -(1/128)V_{OSADJ}$ [0V to 5V, ±2.5V spans]

$\Delta V_{OS} = -(1/64)V_{OSADJ}$ [0V to 10V, ±5V, –2.5V to 7.5V spans]

$\Delta V_{OS} = -(1/32)V_{OSADJ}$ [±10V span]

The gain error adjust pin GE_{ADJ} can be used to null gain error or to compensate for reference errors. The gain error change expressed in LSB is the same for any output range:

$$\Delta GE = \frac{V(GE_{ADJ})}{V(R_{IN})} \bullet 2048$$

The gain-error delta is non-inverting for positive reference voltages.

Note that this pin compensates the gain by altering the inverted reference voltage V(REF). In voltage terms, the V(REF) delta is inverted and attenuated by a factor of 128.

$$\Delta V(REF) = -(1/128)GE_{ADJ}$$

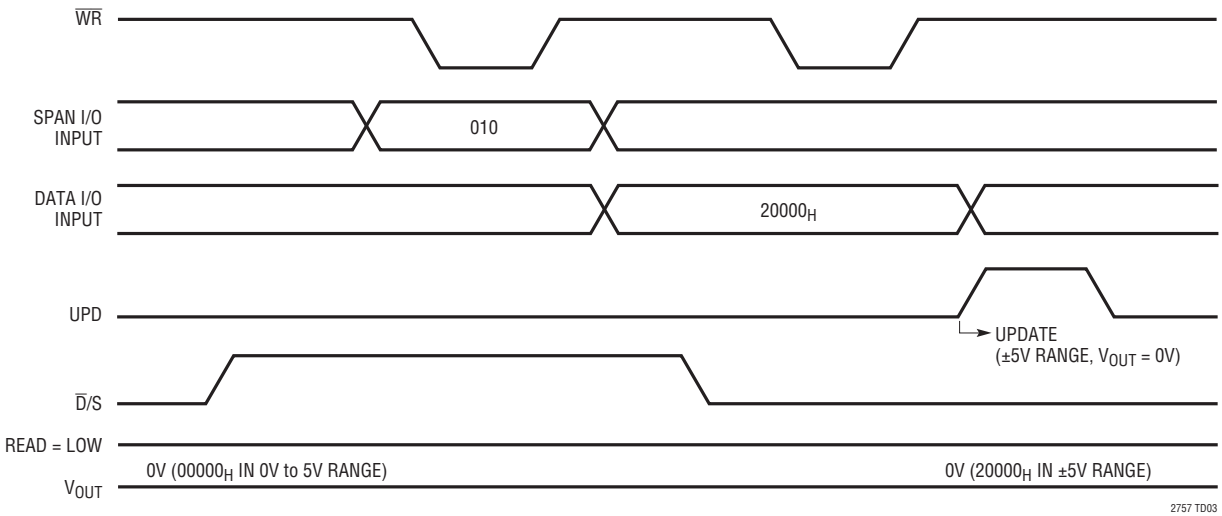
The nominal input range of these pins is ±5V; other voltages of up to ±15V may be used if needed. However, do not use voltages divided down from power supplies; reference-quality, low-noise inputs are required to maintain the best DAC performance.

The V_{OSADJ} pin has an input impedance of 1.28MΩ. This pin should be driven with a Thevenin-equivalent impedance of 10k or less to preserve the settling performance of the LTC2757. It should be shorted to GND if not used.

The GE_{ADJ} pin has an input impedance of 2.56MΩ, and is intended for use with fixed reference voltages only. It should be shorted to GND if not used.

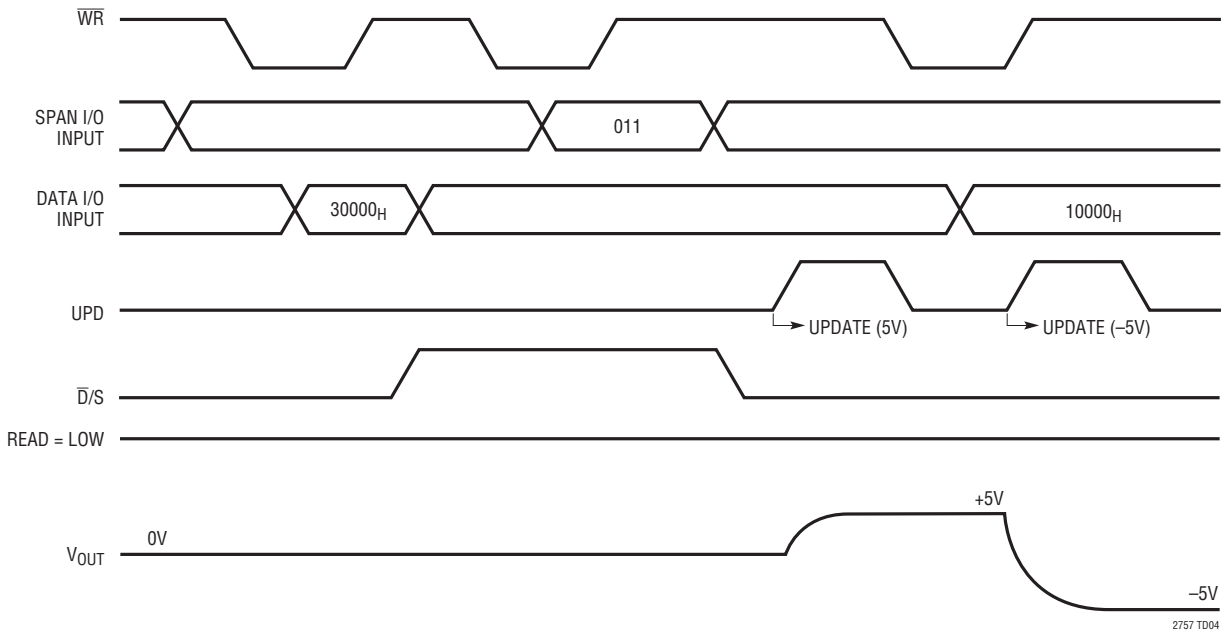
OPERATION—EXAMPLES

1. Load ±5V range with the output at 0V. Note that since span and code are updated together, the output, if started at 0V, will stay there. The 18-bit DAC code is shown in hex for compactness.

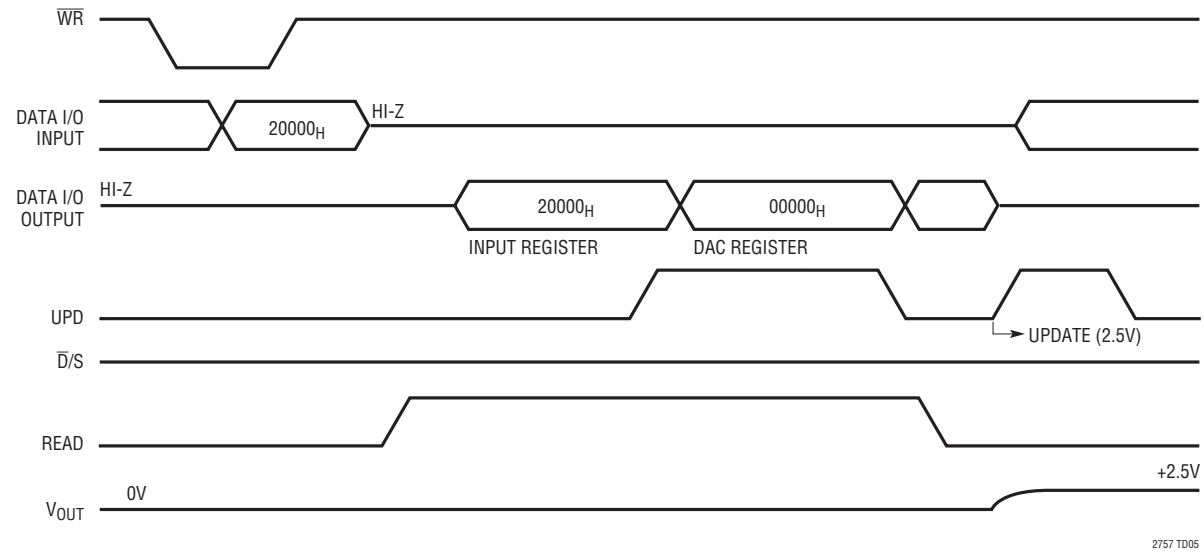


OPERATION—EXAMPLES

2. Load ±10V range with the output at 5V, changing to –5V.



3. Write and update mid-scale code in 0V to 5V range (V_{OUT} = 2.5V) using readback to check the contents of the input and DAC registers before updating.



APPLICATIONS INFORMATION

Op Amp Selection

Because of the extremely high accuracy of the 18-bit LTC2757, careful thought should be given to op amp selection in order to achieve the exceptional performance of which the part is capable. Fortunately, the sensitivity of INL and DNL to op amp offset has been greatly reduced compared to previous generations of multiplying DACs.

Tables 3 and 4 contain equations for evaluating the effects of op amp parameters on the LTC2757's accuracy. These are the changes the op amp can cause to the INL, DNL, unipolar offset, unipolar gain error, bipolar zero and bipolar gain error.

Table 3. Coefficients for the Equations of Table 4

OUTPUT RANGE	A1	A2	A3	A4	A5
5V	1.1	2	1		1
10V	2.2	3	0.5		1.5
±5V	2	2	1	1	1.5
±10V	4	4	0.83	1	2.5
±2.5V	1	1	1.4	1	1
–2.5V to 7.5V	1.9	3	0.7	0.5	1.5

Table 4. Easy-to-Use Equations Determine Op Amp Effects on DAC Accuracy in All Output Ranges (Circuit of Page 1). Subscript 1 Refers to Output Amp, Subscript 2 Refers to Reference Inverting Amp.

OP AMP	INL (LSB)	DNL (LSB)	UNIPOLAR OFFSET (LSB)	BIPOLAR ZERO ERROR (LSB)	UNIPOLAR GAIN ERROR (LSB)	BIPOLAR GAIN ERROR (LSB)
V_{OS1} (mV)	$V_{OS1} \bullet 12.1 \bullet \left(\frac{5V}{V_{REF}}\right)$	$V_{OS1} \bullet 3.1 \bullet \left(\frac{5V}{V_{REF}}\right)$	$A3 \bullet V_{OS1} \bullet 52.4 \bullet \left(\frac{5V}{V_{REF}}\right)$	$A3 \bullet V_{OS1} \bullet 78.6 \bullet \left(\frac{5V}{V_{REF}}\right)$	$V_{OS1} \bullet 52.4 \bullet \left(\frac{5V}{V_{REF}}\right)$	$V_{OS1} \bullet 52.4 \bullet \left(\frac{5V}{V_{REF}}\right)$
I_{B1} (nA)	$I_{B1} \bullet 0.0012 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B1} \bullet 0.00032 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B1} \bullet 0.524 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B1} \bullet 0.524 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B1} \bullet 0.0072 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B1} \bullet 0.0072 \bullet \left(\frac{5V}{V_{REF}}\right)$
A_{VOL1} (V/mV)	$A1 \bullet \left(\frac{66}{A_{VOL1}}\right)$	$A2 \bullet \left(\frac{6}{A_{VOL1}}\right)$	0	0	$A5 \bullet \left(\frac{524}{A_{VOL1}}\right)$	$A5 \bullet \left(\frac{524}{A_{VOL1}}\right)$
V_{OS2} (mV)	0	0	0	$A4 \bullet V_{OS2} \bullet 52.4 \bullet \left(\frac{5V}{V_{REF}}\right)$	$V_{OS2} \bullet 104.8 \bullet \left(\frac{5V}{V_{REF}}\right)$	$V_{OS2} \bullet 104.8 \bullet \left(\frac{5V}{V_{REF}}\right)$
I_{B2} (nA)	0	0	0	$A4 \bullet I_{B2} \bullet 0.524 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B2} \bullet 1.048 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B2} \bullet 1.048 \bullet \left(\frac{5V}{V_{REF}}\right)$
A_{VOL2} (V/mV)	0	0	0	$A4 \bullet \left(\frac{262}{A_{VOL2}}\right)$	$\left(\frac{524}{A_{VOL2}}\right)$	$\left(\frac{524}{A_{VOL2}}\right)$

APPLICATIONS INFORMATION

Table 5. Partial List of LTC Precision Amplifiers Recommended for Use with the LTC2757 with Relevant Specifications

	AMPLIFIER SPECIFICATIONS								
AMPLIFIER	V_{OS} µV	I_B nA	A_{VOL} V/mV	VOLTAGE NOISE nV/√Hz	CURRENT NOISE pA/√Hz	SLEW RATE V/µs	GAIN BANDWIDTH PRODUCT MHz	$t_{SETTLING}$ with LTC2757 µs	POWER DISSIPATION mW
LTC1150	10	0.05	5600	90	0.0018	3	2.5	10ms	24
LT1001	25	2	800	10	0.12	0.25	0.8	120	46
LT1012	25	0.1	2000	14	0.02	0.2	1	120	11.4
LT1097	50	0.35	2500	14	0.008	0.2	0.7	120	11
LT1468	75	10	5000	5	0.6	22	90	2.1	117

Table 5 contains a partial list of LTC precision op amps recommended for use with the LTC2757. The easy-to-use design equations simplify the selection of op amps to meet the system's specified error budget. Select the amplifier from Table 5 and insert the specified op amp parameters in Table 4. Add up all the errors for each category to determine the effect the op amp has on the accuracy of the part. Arithmetic summation gives an (unlikely) worst-case effect. A root-sum-square (RMS) summation produces a more realistic estimate.

Op amp offset contributes mostly to DAC output offset and gain error, and has minimal effect on INL and DNL. For example, consider the LTC2757 in unipolar 5V output range. (Note that for this example, the LSB size is 19µV.) An op amp offset of 35µV will cause 1.8LSB of output offset, and 1.8LSB of gain error; but 0.4LSB of INL, and just 0.1LSB of DNL.

While not directly addressed by the simple equations in Tables 3 and 4, temperature effects can be handled just as easily for unipolar and bipolar applications. First, consult an op amp's data sheet to find the worst-case V_{OS} and I_B over temperature. Then, plug these numbers in the V_{OS} and I_B equations from Table 4 and calculate the temperature-induced effects.

For applications where fast settling time is important, Application Note 120, *1ppm Settling Time Measurement for a Monolithic 18-Bit DAC*, offers a thorough discussion of 18-bit DAC settling time and op amp selection.

Recommendations

To achieve the full specified static and dynamic performance of the LTC2757, the LT1468 amplifier is recommended; it offers a unique combination of fast settling and excellent DC precision. When using the LT1468 as an output amp, however, the offset voltage (75µV max) must be nulled to avoid degrading the linearity of the LTC2757. The LT1468 datasheet shows how to do this with a digital potentiometer.

For DC or low-frequency applications, the LTC1150 is the simplest 18-bit accurate output amplifier. An auto-zero amp, its exceptionally low offset (10µV max) and offset drift (0.01µV/°C) make nulling unnecessary. Note: for swings above 8V, use an LT1010 buffer to boost the load current capability of the LTC1150. The settling of auto-zero amps is a special case; see Application Note 120, *1ppm Settling Time Measurement for a Monolithic 18-Bit DAC*, Appendix E, for details.

The LT1012 and LT1001 are good intermediate output-amp solutions that achieve moderate speed and good accuracy. They are also excellent choices for the reference inverting amplifier in fixed-reference applications.

Figure 3 shows a composite output amplifier that achieves fast settling (8µs) and very low offset (3µV max) without offset nulling. This circuit offers high open-loop gain (1000V/mV min), low input bias current (0.15nA max), fast slew rate (25V/µs min), and a high gain-bandwidth product (30MHz typ). The high speed path consists of an LTC6240, which is an 18MHz ultra-low bias current amplifier, followed by an LT1360, a 50MHz fast-slewing amplifier which provides additional gain and the ability to

APPLICATIONS INFORMATION

swing to ±10V at the output. Compensation is taken from the output of the LTC6240, allowing the use of a much larger compensation capacitor than if taken after the gain-of-five stage. An LTC2054 auto-zero amplifier senses the voltage at I_{OUT1} and drives the non-inverting input of the LTC6240 to eliminate the offset of the high speed path. The 100:1 attenuator and input filter reduce the low frequency noise in this stage while maintaining low DC offset.

Precision Voltage Reference Considerations

Much in the same way selecting an operational amplifier for use with the LTC2757 is critical to the performance of the system, selecting a precision voltage reference also requires due diligence. The output voltage of the LTC2757 is directly affected by the voltage reference; thus, any voltage reference error will appear as a DAC output voltage error.

There are three primary error sources to consider when selecting a precision voltage reference for 18-bit applications: output voltage initial tolerance, output voltage temperature coefficient and output voltage noise.

Initial reference output voltage tolerance, if uncorrected, generates a full-scale error term. Choosing a reference with low output voltage initial tolerance, like the LT1236 (±0.05%), minimizes the gain error caused by the reference; however, a calibration sequence that corrects for system zero- and full-scale error is always recommended.

A reference's output voltage temperature coefficient affects not only the full-scale error, but can also affect the circuit's INL and DNL performance. If a reference is chosen with a loose output voltage temperature coefficient, then the DAC output voltage along its transfer characteristic will be very dependent on ambient conditions. Minimizing the error due to reference temperature coefficient can be achieved by choosing a precision reference with a low output voltage temperature coefficient and/or tightly controlling the ambient temperature of the circuit to minimize temperature gradients.

As precision DAC applications move to 18-bit performance, reference output voltage noise may contribute a dominant share of the system's noise floor. This in turn can degrade system dynamic range and signal-to-noise ratio. Care should be exercised in selecting a voltage reference with as low an output noise voltage as practical for the system resolution desired. Precision voltage references like the LT1236 produce low output noise in the 0.1Hz to 10Hz region, well below the 18-bit LSB level in 5V or 10V full-scale systems. However, as the circuit bandwidths increase, filtering the output of the reference may be required to minimize output noise.

Table 6. Partial List of LTC Precision References Recommended for Use with the LTC2757 with Relevant Specifications

REFERENCE	INITIAL TOLERANCE	TEMPERATURE DRIFT	0.1Hz to 10Hz NOISE
LT1019A-5, LT1019A-10	±0.05% Max	5ppm/°C Max	$12\mu V_{P-P}$
LT1236A-5, LT1236A-10	±0.05% Max	5ppm/°C Max	$3\mu V_{P-P}$
LT1460A-5, LT1460A-10	±0.075% Max	10ppm/°C Max	$20\mu V_{P-P}$
LT1790A-2.5	±0.05% Max	10ppm/°C Max	$12\mu V_{P-P}$
LTC6655-2.5 LTC6655-5	±0.025% Max	2ppm/°C Max	$0.62\mu V_{P-P}$

Grounding

As with any high-resolution converter, clean grounding is important. A low-impedance analog ground plane is necessary, as are star grounding techniques. Keep the board layer used for star ground continuous to minimize ground resistances; that is, use the star-ground concept without using separate star traces. The I_{OUT2} pins are of particular concern; INL will be degraded by the code-dependent currents carried by the I_{OUT2F} and I_{OUT2S} pins if voltage drops to ground are allowed to develop. The best strategy here is to tie the pins to the star ground plane by multiple vias located directly underneath the part. Alternatively, the pins may be routed to the star ground point if necessary; join them together at the part and route a single trace of no more than 30 squares of 1oz copper.

In the rare case in which neither of these alternatives is practicable, a force/sense amplifier should be used as a ground buffer (see the Typical Applications section). Note, however, that the voltage offset of the ground buffer amp directly contributes to the effects on accuracy specified in Table 4 under 'V_{OS1}'. The combined effects of the offsets can be calculated by substituting the total offset from I_{OUT1} to I_{OUT2S} for V_{OS1} in the equations.

TYPICAL APPLICATIONS

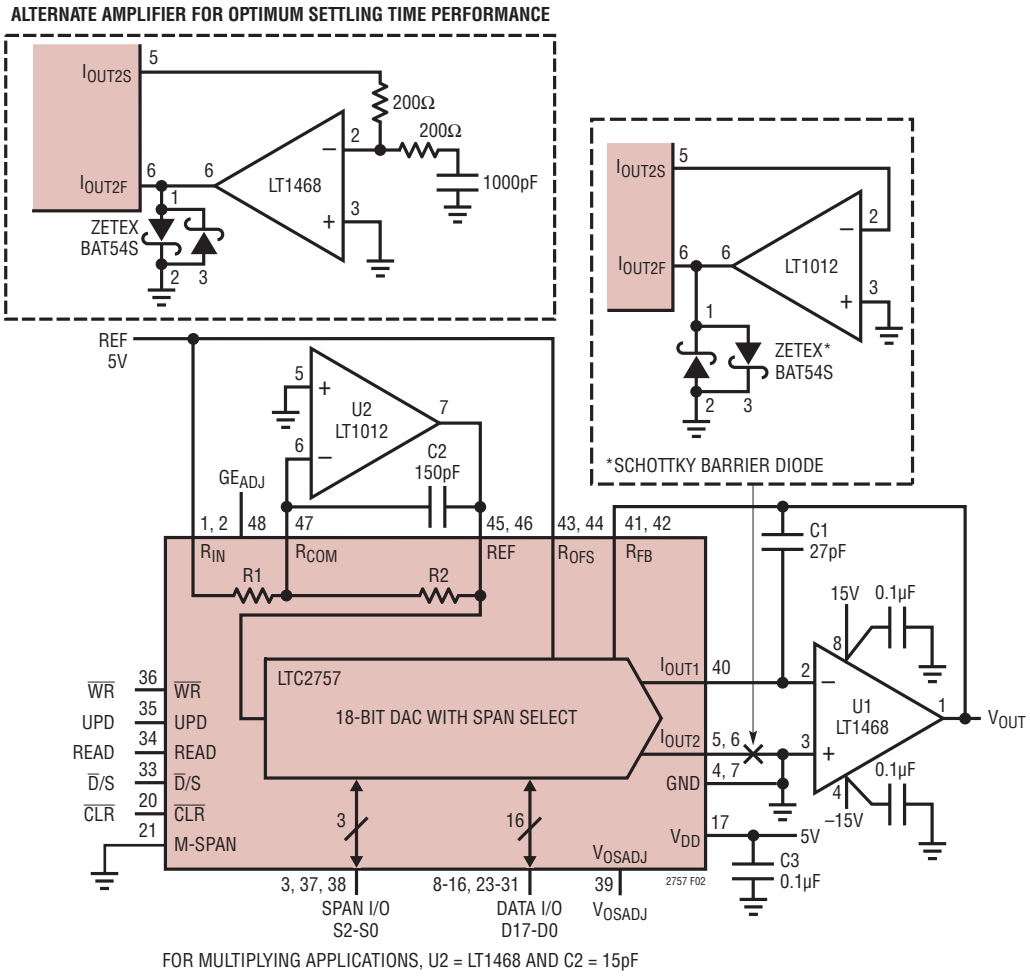
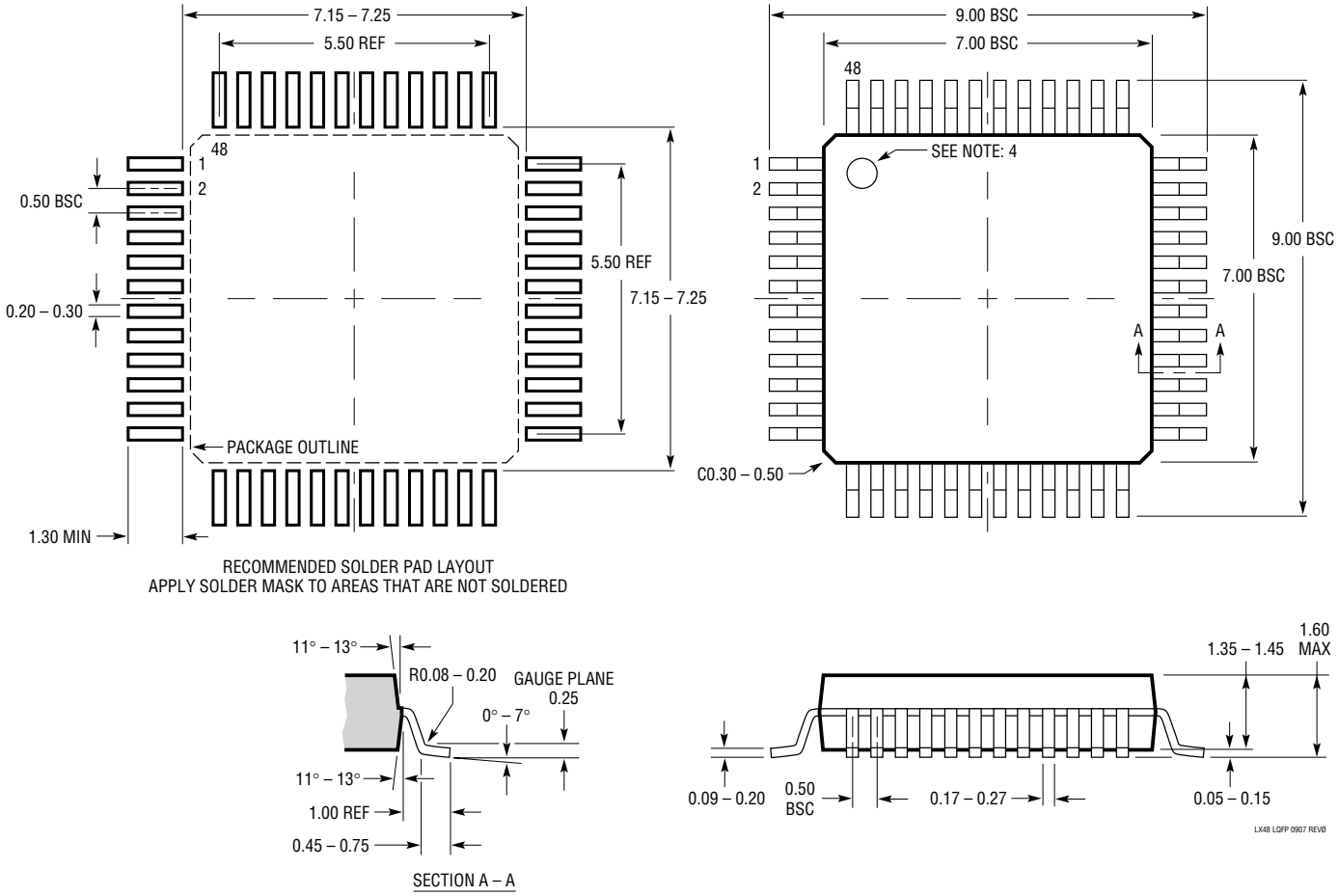


Figure 2. Basic Connections for SoftSpan V_{OUT} DAC with Two Optional Circuits for Driving I_{OUT2} from GND with a Force/Sense Amplifier

PACKAGE DESCRIPTION

LX Package
48-Lead Plastic LQFP (7mm × 7mm)
(Reference LTC DWG # 05-08-1760 Rev Ø)



NOTE:
1. PACKAGE DIMENSIONS CONFORM TO JEDEC #MS-026 PACKAGE OUTLINE
2. DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.25mm ON ANY SIDE, IF PRESENT
4. PIN-1 INDENTIFIER IS A MOLDED INDENTATION, 0.50mm DIAMETER
5. DRAWING IS NOT TO SCALE

TYPICAL APPLICATION

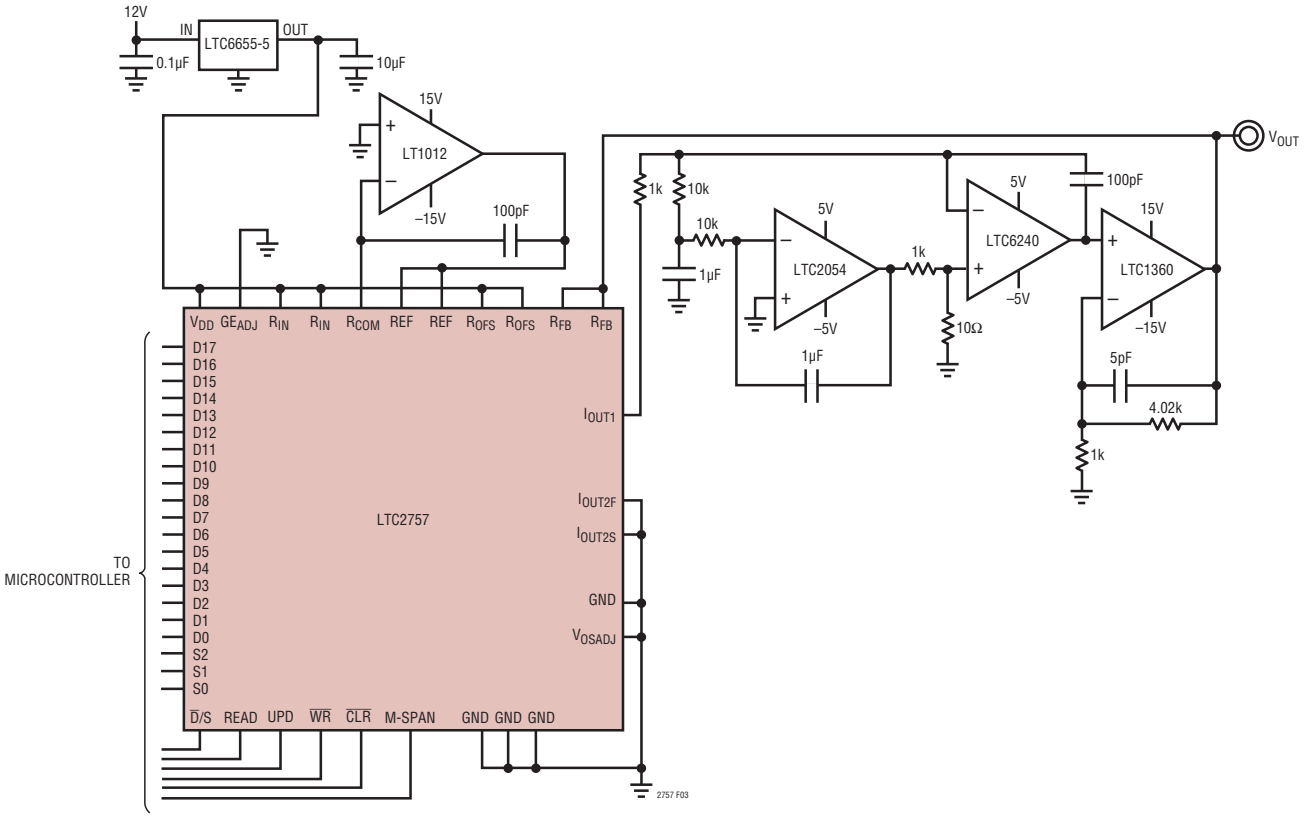


Figure 3. Composite Amplifier Provides 18-Bit Precision and Fast Settling

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1591/ LTC1597	Parallel 14-/16-Bit I_{OUT} Single DAC	Integrated 4-Quadrant Resistors
LTC1592	Serial 16-Bit I_{OUT} Single DAC	Software-Selectable (SoftSpan) Ranges, ±1LSB INL, DNL, 16-Lead SSOP Package
LTC1821	Parallel 16-Bit V_{OUT} Single DAC	±1LSB INL, DNL, 0V to 10V, 0V to –10V, ±10V Output Ranges
LTC2641/ LTC2642	Serial 12-/14-/16-Bit Unbuffered V_{OUT} Single DACs	±1LSB INL, ±1LSB DNL, 1µs Settling, Tiny MSOP-10, 3mm × 3mm DFN-10 Packages
LTC2704	Serial 12-/14-/16-Bit V_{OUT} SoftSpan Quad DACs	Software-Selectable Ranges, Integrated Amplifiers
LTC2751	Parallel 12-/14-/16-Bit I_{OUT} SoftSpan Single DAC	±1LSB INL, DNL, Software-Selectable Ranges, 5mm × 7mm QFN-38 Package
LTC2753	Parallel 12-/14-/16-Bit I_{OUT} SoftSpan Dual DACs	±1LSB INL, DNL, Software-Selectable Ranges, 7mm × 7mm QFN-48 Package
LTC2754	Serial 12-/16-Bit I_{OUT} SoftSpan Quad DACs	±1LSB INL, DNL, Software-Selectable Ranges, 7mm × 8mm QFN-52 Package
LTC2755	Parallel 12-/14-/16-Bit I_{OUT} SoftSpan Quad DACs	±1LSB INL, DNL, Software-Selectable Ranges, 9mm × 9mm QFN-64 Package
LT1027	Precision Reference	1ppm/°C Maximum Drift
LT1236A-5	Precision Reference	0.05% Maximum Tolerance, 1ppm 0.1Hz to 10Hz Noise
LTC1150	±15V Zero-Drift Op Amp	10µV Maximum Offset Voltage, 1.8µV_{P-P} (0.1Hz to 10Hz) Noise, 0.8mA Supply Current
LT1468	16-Bit Accurate Op Amp	90MHz GBW, 22V/µs Slew Rate

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
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