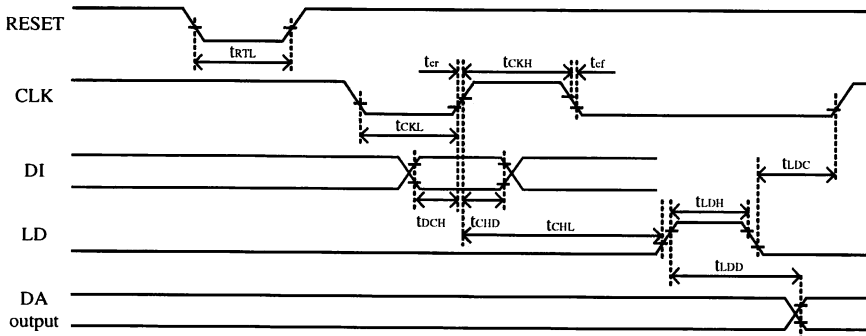


◇Electrical Characteristics (VCC=5V,VrefH=5V,VrefL=0V,Ta=25°C, unless otherwise noted)

Parameter	Symbol	Limits			Unit	Test conditions
		MIN.	TYP.	MAX.		
<<Digital part>>						
Circuit current	ICC	-	0.85	2.8	mA	CLK=10MHz operation, VCC=5V, IAO=0μA
Input leak current	IILK	-5	-	5	μA	VIN=0~VCC
Input low voltage	VIL	-	-	0.8	V	
Input high voltage	VIH	2.0	-	-	V	
Output low voltage	VOL	0	-	0.4	V	IOL=2.5mA
Output high voltage	VOH	4.6	-	5	V	IOH=2.5mA
<< Analog part >>						
Current dissipation	IrefH	-	4.5	7.5	mA	VrefH =5V, VrefL=0V Data condition:Maximum Current
D/A converter upper reference voltage range	VrefH	3.0	-	5	V	Reference voltage can not always be set to any value in this range, because it is restricted to the buffer amplifier output voltage range
D/A converter lower reference voltage range	VrefL	0	-	1.5	V	
Buffer amplifier output driver voltage range	VO	0.1	-	4.9	V	IO=±100μA
		0.2	-	4.75		IO=±1.0mA
Buffer amplifier output voltage range	IO	-2	-	2	mA	Upper saturation voltage=0.35V Lower saturation voltage=0.23V
Accuracy	Differential nonlinearity error	SDL	-1.0	-	1.0	LSB
	Nonlinearity error	SL	-3.5	-	3.5	
	Zero code error	SZERO	-25	-	25	mV
	Full scale error	SFULL	-25	-	25	
Buffer amplifier output impedance	RO	-	5	15	Ω	
Pull-up I/O-cell internal R value	Rup	12.5	25	37.5	kΩ	Vin:0V (Resistance value alters by the applied voltage.)

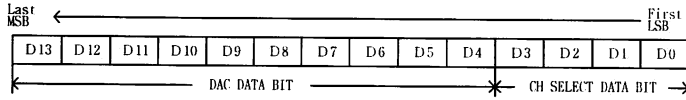
◇Timing characteristic (VCC=5V,VrefH=5V,VrefL=0V,Ta=25°C, unless otherwise noted)

Parameter	Symbol	Limits			Unit	Test conditions
		MIN.	TYP.	MAX.		
Reset "L" pulse width	tRTL	50	-	-	nS	The threshold voltage is 80% * 20% of VCC
Clock "L" pulse width	tCKL	50	-	-		
Clock "H" pulse width	tCKH	50	-	-		
Clock rise time	ter	-	-	50		
Clock fall time	tcf	-	-	50		
Data set up time	tDCH	20	-	-		
Data hold time	tCHD	40	-	-		
LD set up time	tCHL	50	-	-		
LD hold time	tLDC	50	-	-		
LD "H" pulse duration	tLDH	50	-	-		
D/A output setting time	tLDD	-	7	20		

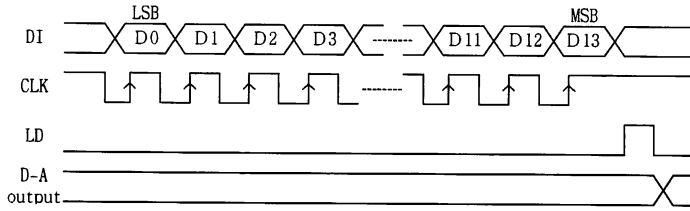


◇Command transmission

○ DIGITAL DATA FORMAT [data : LSBfirst]



○ TIMING CHART(MODEL)



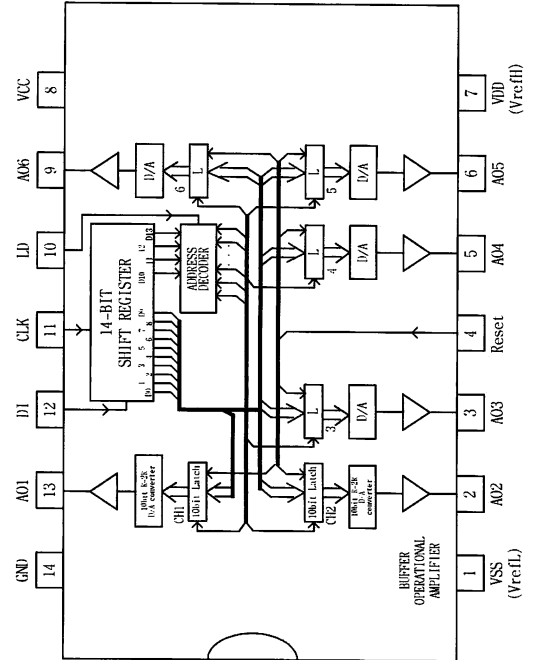
D3	D2	D1	D0	DAC selection
0	0	0	0	Don't Care
0	0	0	1	Don't Care
0	0	1	0	AO1 selection
0	0	1	1	AO2 selection
0	1	0	0	Don't Care
0	1	0	1	AO3 selection
0	1	1	0	AO4 selection
0	1	1	1	Don't Care
1	0	0	0	AO5 selection
1	0	0	1	AO6 selection
1	0	1	0	Don't Care
1	0	1	1	Don't Care
1	1	0	0	Don't Care
1	1	0	1	Don't Care
1	1	1	0	Don't Care
1	1	1	1	Don't Care

D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D/A output (VrefH=VDD, VrefL=VSS)
0	0	0	0	0	0	0	0	0	0	VrefL
0	0	0	0	0	0	0	0	0	1	$(VrefH-VrefL)/1024 \times 1 + VrefL$
0	0	0	0	0	0	0	0	1	0	$(VrefH-VrefL)/1024 \times 2 + VrefL$
0	0	0	0	0	0	0	0	1	1	$(VrefH-VrefL)/1024 \times 3 + VrefL$
:	:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	1	0	$(VrefH-VrefL)/1024 \times 1022 + VrefL$
1	1	1	1	1	1	1	1	1	1	$(VrefH-VrefL)/1024 \times 1023 + VrefL$

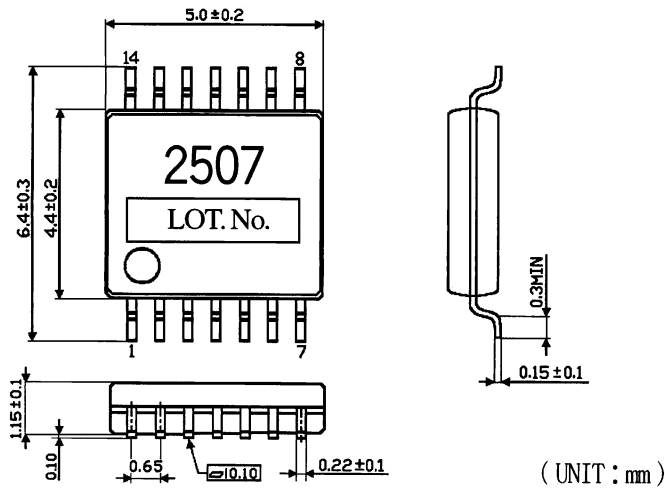
◇Explanation Of Terminals / Block Diagram

Pin No.	Symbol	Function
1	VSS	D/A converter lower reference voltage input terminal
2	AO2	10bit D/A converter output terminal (CH 2)
3	AO3	10bit D/A converter output terminal (CH 3)
4	Reset	The analog output of all channels is fixed for "L".
5	AO4	10bit D/A converter output terminal (CH 4)
6	AO5	10bit D/A converter output terminal (CH 5)
7	VDD	D/A converter upper reference voltage input terminal
8	VCC	Power supply terminal
9	AO6	10bit D/A converter output terminal (CH 6)
10	LD	When H-level signal is input to this terminal, the value stored in 14-bit shift register is loaded in decoder and D/A converter output register
11	CLK	Shift clock input terminal. Input signal at DI pin is input to 14-bit shift register at rise of shift clock pulse
12	DI	Serial data input terminal to input 14-bit long serial data
13	AO1	10bit D/A converter output terminal (CH 1)
14	GND	GND terminal

Please refer to directions also when using it.



◇External Dimensions



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