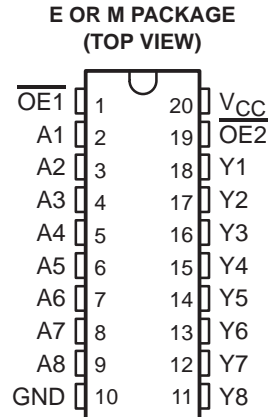


# CD74FCT540 BiCMOS OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCBS740 – JULY 2000

- BiCMOS Technology With Low Quiescent Power
- Buffered Inputs
- Inverted Outputs
- Input/Output Isolation From  $V_{CC}$
- Controlled Output Edge Rates
- 64-mA Output Sink Current
- Output Voltage Swing Limited to 3.7 V
- SCR Latch-Up-Resistant BiCMOS Process and Circuit Design
- Package Options Include Plastic Small-Outline (M) Package and Standard Plastic (E) DIP



## description

The CD74FCT540 is an octal buffer/driver with 3-state outputs that is ideal for driving bus lines or buffer memory address registers and uses a small-geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output high level to two diode drops below  $V_{CC}$ . This resultant lowering of output swing (0 V to 3.7 V) reduces power-bus ringing [a source of electromagnetic interference (EMI)] and minimizes  $V_{CC}$  bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 64 mA.

The 3-state control gate is a two-input AND gate with active-low inputs, so that if either output-enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all corresponding outputs are in the high-impedance state. The outputs provide inverted data when they are not in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The CD74FCT540 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE  
(each buffer/driver)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z



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 **TEXAS  
INSTRUMENTS**

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**recommended operating conditions (see Note 2)**

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.75	5.25	V
V <sub>IH</sub>	High-level input voltage	2		V
V <sub>IL</sub>	Low-level input voltage		0.8	V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		-15	mA
I <sub>OL</sub>	Low-level output current		64	mA
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T <sub>A</sub>	Operating free-air temperature	0	70	°C

NOTE 2: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C		MIN	MAX	UNIT
			MIN	MAX			
V <sub>IK</sub>	I <sub>I</sub> = -18 mA	4.75 V		-1.2		-1.2	V
V <sub>OH</sub>	I <sub>OH</sub> = -15 mA	4.75 V	2.4		2.4		V
V <sub>OL</sub>	I <sub>OL</sub> = 64 mA	4.75 V		0.55	0.55		V
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.25 V		±0.1		±1	μA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.25 V		±0.5		±10	μA
I <sub>OS</sub> <sup>†</sup>	V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>O</sub> = 0	5.25 V		-60		-60	mA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.25 V		8		80	μA
ΔI <sub>CC</sub> <sup>‡</sup>	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.25 V		1.6		1.6	mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND			10		10	pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND			15		15	pF

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 100 ms.

<sup>‡</sup> This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

**switching characteristics over recommended operating conditions, V<sub>CC</sub> = 5 V ± 0.25 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C	MIN	MAX	UNIT
			TYP			
t <sub>pd</sub>	A	Y	6.4	2	8.5	ns
t <sub>en</sub>	$\overline{OE}$	Y	7.5	2	10	ns
t <sub>dis</sub>	$\overline{OE}$	Y	7.1	2	9.5	ns

**noise characteristics, V<sub>CC</sub> = 5 V, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C**

PARAMETER	MIN	TYP	MAX	UNIT
V <sub>OL(P)</sub> Quiet output, maximum dynamic V <sub>OL</sub>		1		V
V <sub>OH(V)</sub> Quiet output, minimum dynamic V <sub>OH</sub>		0.5		V
V <sub>IH(D)</sub> High-level dynamic input voltage	2			V
V <sub>IL(D)</sub> Low-level dynamic input voltage			0.8	V

**CD74FCT540**  
**BiCMOS OCTAL BUFFER/DRIVER**  
**WITH 3-STATE OUTPUTS**

SCBS740 – JULY 2000

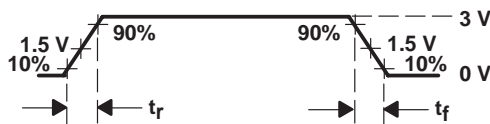
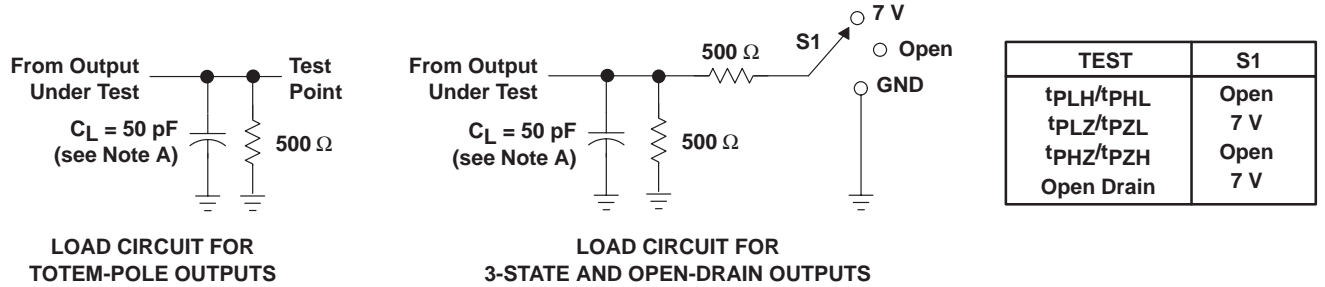
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**operating characteristics,  $T_A = 25^\circ\text{C}$**

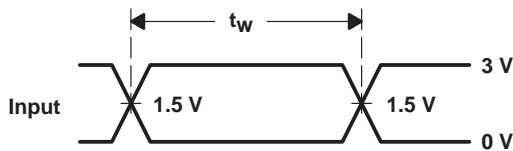
PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load, $f = 1\text{ MHz}$	37	pF



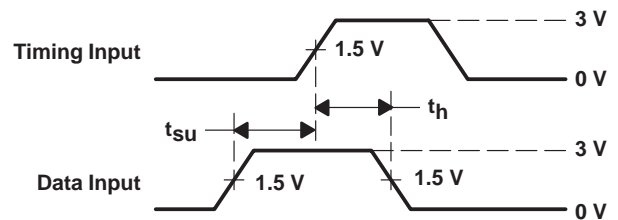
PARAMETER MEASUREMENT INFORMATION



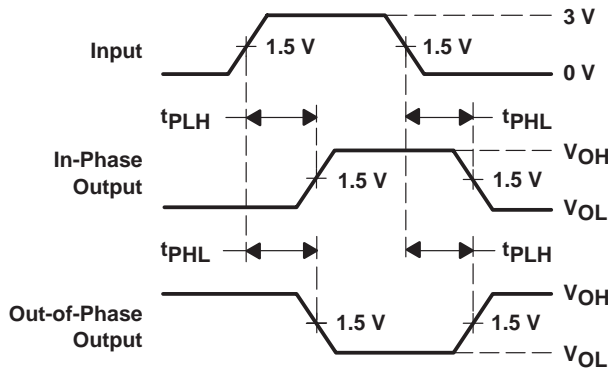
VOLTAGE WAVEFORM  
INPUT RISE AND FALL TIMES



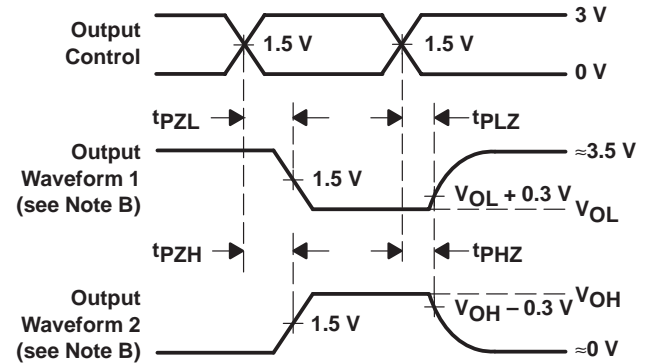
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r$  and  $t_f = 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one input transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
CD74FCT540E	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	Samples Not Available
CD74FCT540M	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	Samples Not Available
CD74FCT540M96	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	Samples Not Available

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

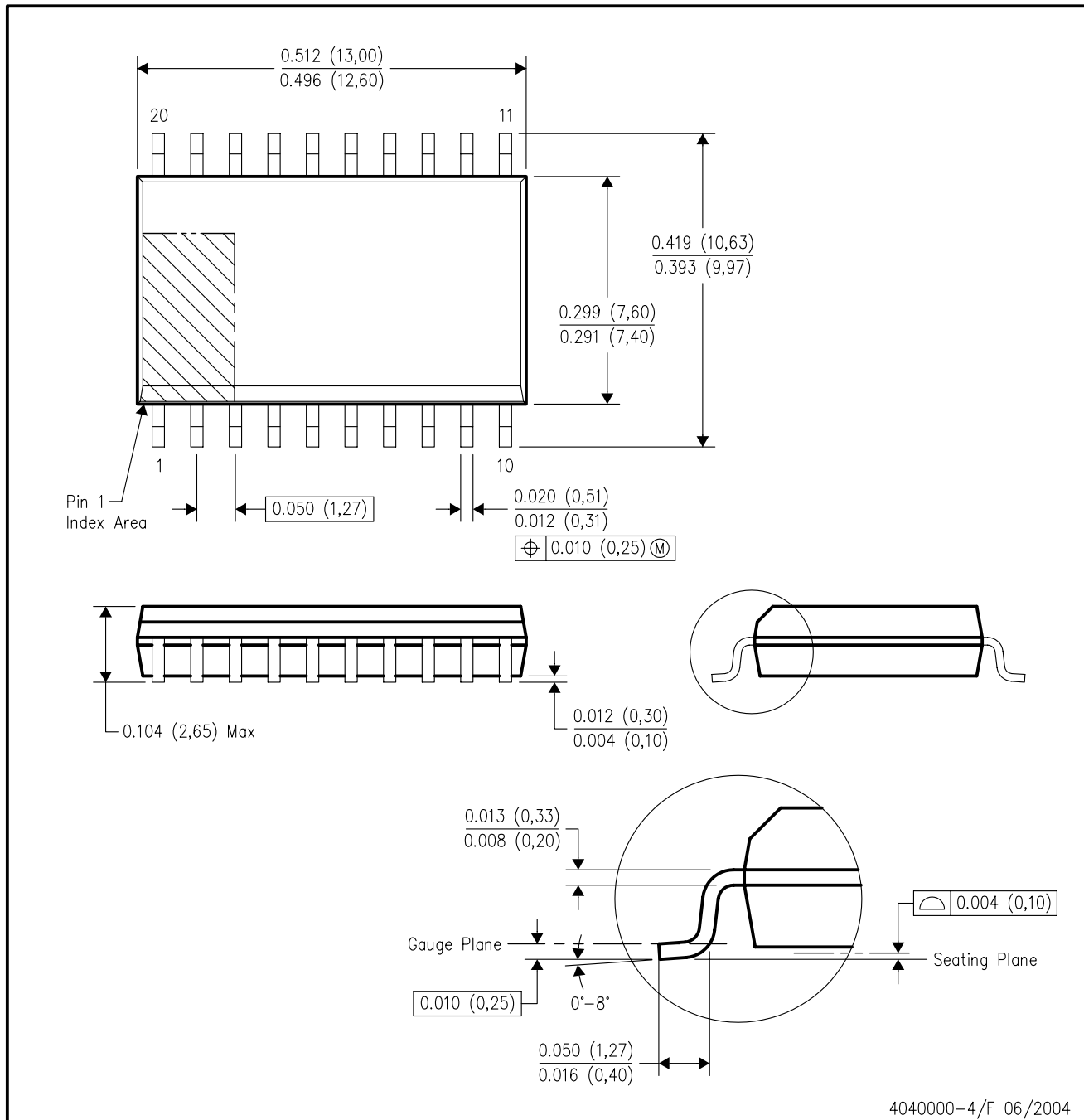
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DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.



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