![Texas Instruments logo] **TEXAS INSTRUMENTS**

Data sheet acquired from Harris Semiconductor
SCHS193A

January 1998 - Revised May 2003

NOT RECOMMENDED FOR NEW DESIGNS

CD74HC646

High-Speed CMOS Logic
Octal Bus Transceiver/Register, Three-State

Features

- **Independent Registers for A and B Buses**
- **Non-Inverting**
- **Three-State Outputs**
- **Drives 15 LSTTL Loads**
- **Typical Propagation Delay = 12ns (A to B, B to A) at V_{CC} = 5V, C_L = 15pF, T_A = 25°C**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55°C to 125°C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**

Description

The CD74HC646 is an octal bus transceiver/register with three-state non-inverting outputs. This device is a bus transceiver with D-type flip-flops which act as internal storage registers. Data on the A bus or the B bus can be clocked into the registers on the Low-to-High transition of either CAB or CBA clock inputs. Outputs enable ($\overline{OE}$) and direction (DIR) inputs control the transceiver functions. Data present at the high impedance output can be stored in either register or both but only one of the two buses can be enabled as outputs at any one time. The select controls (SAB and SBA) can multiplex stored and transparent (real time) data. The direction control determines which data bus will receive data when the output enable ($\overline{OE}$) is Low. In the high impedance mode (output enable High), A data can be stored in one register and B data can be stored in the other register. The clocks are not gated with the direction (DIR) and output enable ($\overline{OE}$) terminals; data at the A or B terminals can be clocked into the storage flip-flops at any time.
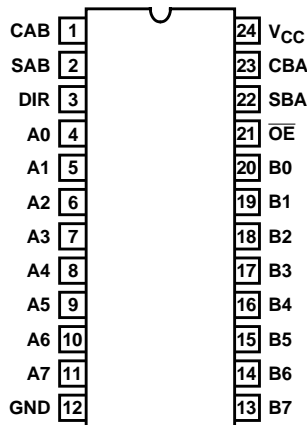
Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE
CD74HC646M	-55 to 125	24 Ld SOIC
CD74HC646M96	-55 to 125	24 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel.
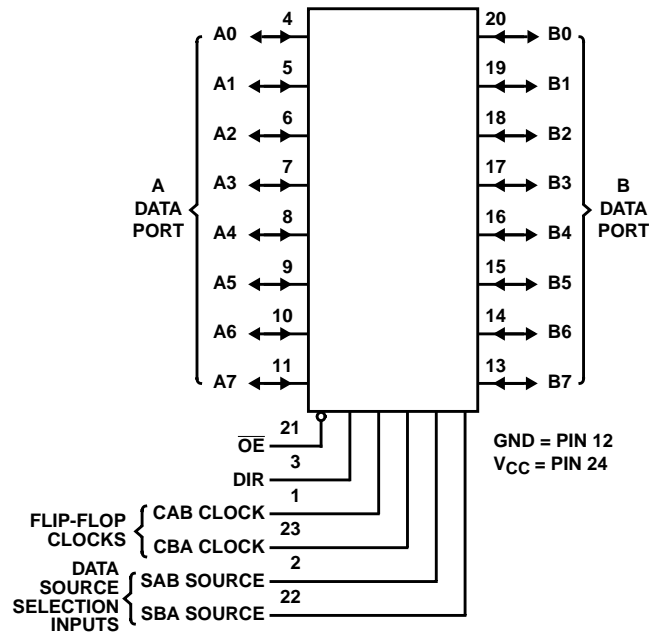
Pinout

CD74HC646
(SOIC)
TOP VIEW

Pin	Signal		Pin	Signal
1	CAB		24	V_{CC}
2	SAB		23	CBA
3	DIR		22	SBA
4	A0		21	$\overline{OE}$
5	A1		20	B0
6	A2		19	B1
7	A3		18	B2
8	A4		17	B3
9	A5		16	B4
10	A6		15	B5
11	A7		14	B6
12	GND		13	B7

Functional Diagram

FUNCTION TABLE

INPUTS						DATA I/O (NOTE 1)		
$\overline{OE}$	DIR	CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	OPERATION OR FUNCTION
X	X	↑	X	X	X	Input	Not Specified	Store A, B Unspecified
X	X	X	↑	X	X	Not Specified	Input	Store B, A Unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, Hold Storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus

NOTE:

1. The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data inputs functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs. To prevent excess currents in the High-Z modes all I/O terminals should be terminated with 10kΩ resistors.

CD74HC646

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
   For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . ±20mA
DC Output Diode Current, I_{OK}
   For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . ±20mA
DC Drain Current, per Output, I_O
   For -0.5V < V_O < V_{CC} + 0.5V . . . . ±35mA
DC Output Source or Sink Current per Output Pin, I_O
   For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} . . . . ±50mA

Thermal Information

Thermal Resistance (Typical) θ_{JA} (^{o}C/W)
  M (SOIC) Package (Note 2).   46
Maximum Junction Temperature . . . . 150°C
Maximum Storage Temperature Range . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
  (SOIC - Lead Tips Only)

Operating Conditions

Temperature Range, T_A . . . . -55°C to 125°C
Supply Voltage Range, V_{CC}
  HC Types . . . . .2V to 6V
DC Input or Output Voltage, V_I, V_O . . . . 0V to V_{CC}
Input Rise and Fall Time
  2V . . . . 1000ns (Max)
  4.5V. . . . . 500ns (Max)
  6V . . . . 400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			-6	4.5	3.98	-	-	3.84	-	3.7	-	V
			-7.8	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			6	4.5	-	-	0.26	-	0.33	-	0.4	V
			7.8	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	µA
Three-State Leakage Current	I_{OZ}	V_{IL} or V_{IH}	V_O = V_{CC} or GND	6	-	-	±0.5	-	±5	-	±10	µA

Prerequisite for Switching Specifications

PARAMETER	SYMBOL	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C TYP	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C TYP	-55°C TO 125°C MAX	UNITS
HC TYPES												
Maximum Frequency	f_{MAX}	2	6	-	-	5	-	-	4	-	-	MHz
		4.5	30	-	-	25	-	-	20	-	-	MHz
		6	35	-	-	29	-	-	23	-	-	MHz
Setup Time Data to Clock	t_{SU}	2	60	-	-	75	-	-	90	-	-	ns
		4.5	12	-	-	15	-	-	18	-	-	ns
		6	10	-	-	13	-	-	15	-	-	ns
Hold Time Data to Clock	t_H	2	35	-	-	45	-	-	55	-	-	ns
		4.5	7	-	-	9	-	-	11	-	-	ns
		6	6	-	-	8	-	-	9	-	-	ns
Clock Pulse Width	t_W	2	80	-	-	100	-	-	120	-	-	ns
		4.5	16	-	-	20	-	-	24	-	-	ns
		6	14	-	-	17	-	-	20	-	-	ns

Switching Specifications C_L = 50pF, Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
HC TYPES											
Propagation Delay Store A Data to B Bus Store B Data to B Bus	t_{PHL}, t_{PLH}	C_L = 50pF	2	-	-	220	-	275	-	330	ns
			4.5	-	-	44	-	55	-	66	ns
		C_L = 15pF	5	-	18	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	37	-	47	-	56	ns
A Data to B Bus B Data to A Bus	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	135	-	170	-	205	ns
			4.5	-	-	27	-	34	-	41	ns
		C_L = 15pF	5	-	12	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	23	-	29	-	35	ns
Select to Data	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	170	-	215	-	255	ns
			4.5	-	-	34	-	43	-	51	ns
		C_L = 15pF	5	-	14	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	29	-	37	-	43	ns

CD74HC646

Switching Specifications C_L = 50pF, Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Three-State Disabling Time Bus to Output or Register to Output	t_{PLZ}, t_{PHZ}	C_L = 50pF	2	-	-	175	-	220	-	265	ns
			4.5	-	-	35	-	44	-	53	ns
		C_L = 15pF	5	-	14	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	30	-	37	-	45	ns
Three-State Enabling Time Bus to Output or Register to Output	t_{PZL}, t_{PZH}	C_L = 50pF	2	-	-	175	-	220	-	265	ns
			4.5	-	-	35	-	44	-	53	ns
		C_L = 15pF	5	-	14	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	30	-	37	-	45	ns
Output Transition Time	t_{TLH}, t_{THL}	C_L = 50pF	2	-	-	60	-	75	-	90	ns
			4.5	-	-	12	-	15	-	18	ns
		C_L = 50pF	6	-	-	10	-	13	-	15	ns
Input Capacitance	C_{IN}	C_L = 50pF	-	10	-	10	-	10	-	10	pF
Three-State Output Capacitance	C_O	-	-	-	-	20	-	20	-	20	pF
Maximum Frequency	f_{MAX}	C_L = 15pF	5	-	60	-	-	-	-	-	MHz
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	-	5	-	52	-	-	-	-	-	pF

NOTES:

3. C_{PD} is used to determine the dynamic power consumption, per package.

4. $P_D = V_{CC}^2 C_{PD} f_i \Sigma V_{CC}^2 C_L f_o$ where f_i = Input Frequency, f_o = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

CD74HC646

Test Circuits and Waveforms
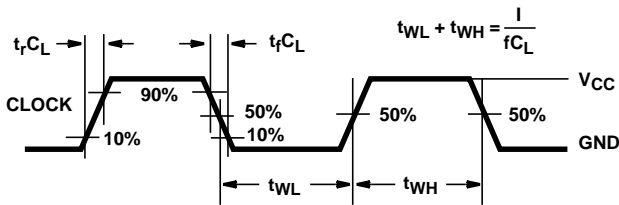
NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX}, input duty cycle = 50%.

FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

$$t_{WL} + t_{WH} = \frac{1}{fC_L}$$
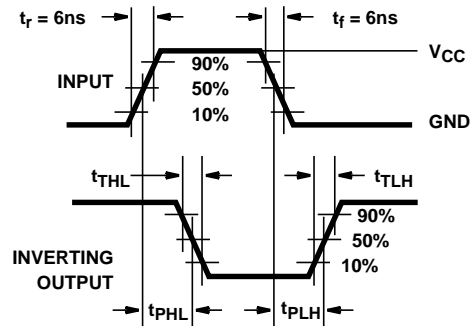
FIGURE 2. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC
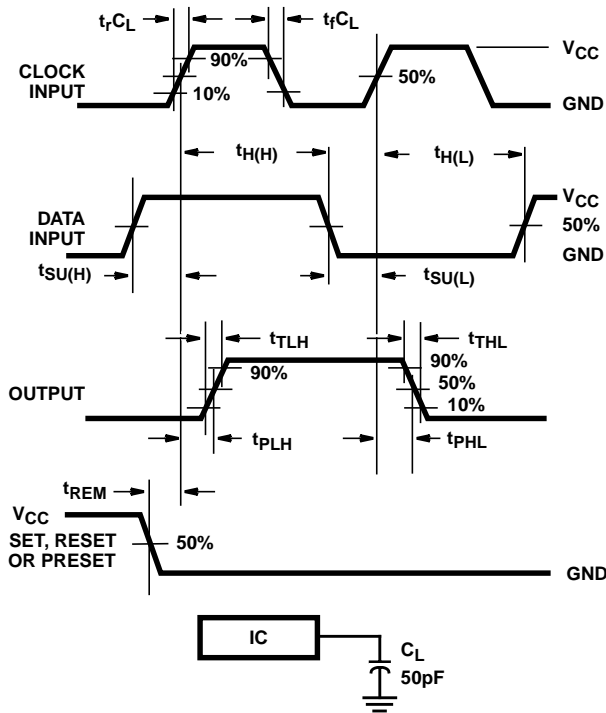
FIGURE 3. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS
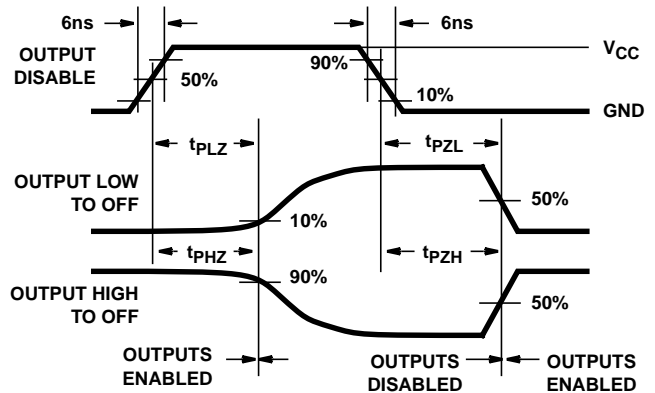
FIGURE 4. HC THREE-STATE PROPAGATION DELAY WAVEFORM

OTHER INPUTS TIED HIGH OR LOW

IC WITH THREE-STATE OUTPUT

OUTPUT DISABLE

OUTPUT $R_L = 1k\Omega$

C_L 50pF

V_{CC} FOR t_{PLZ} AND t_{PZL}
GND FOR t_{PHZ} AND t_{PZH}
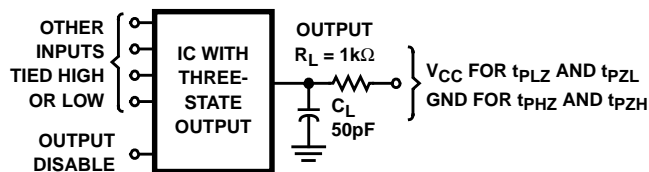
NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output $R_L = 1k\Omega$ to V_{CC}, C_L = 50pF.

FIGURE 5. HC THREE-STATE PROPAGATION DELAY TEST CIRCUIT

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
CD74HC646EN	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI
CD74HC646ENE4	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI
CD74HC646M	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
CD74HC646M96	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
CD74HC646M96E4	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
CD74HC646ME4	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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OTHER QUALIFIED VERSIONS OF CD74HC646 :
● Military: CD54HC646

NOTE: Qualified Version Definitions:
     ● Military - QML certified for Military and Defense Applications

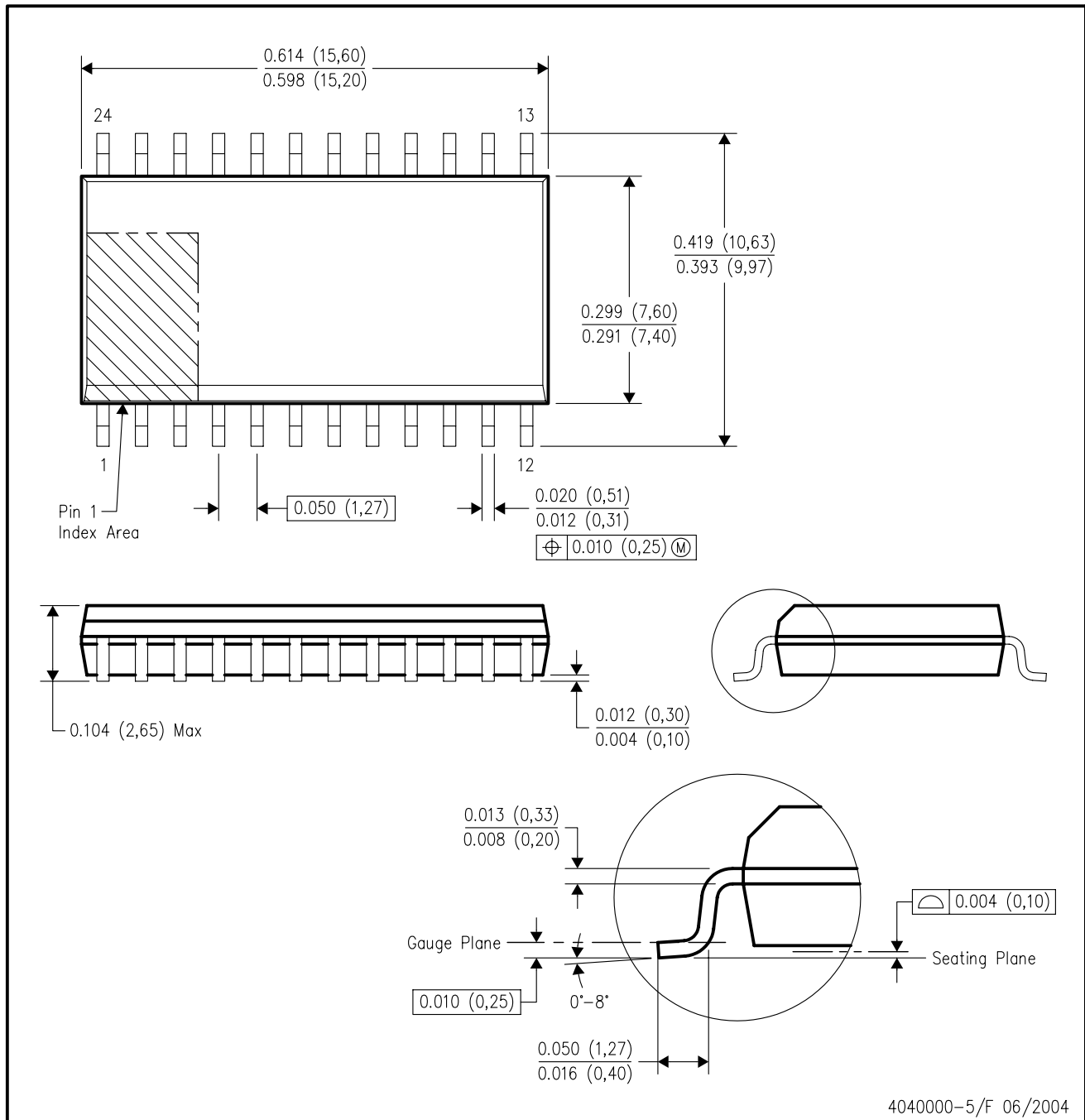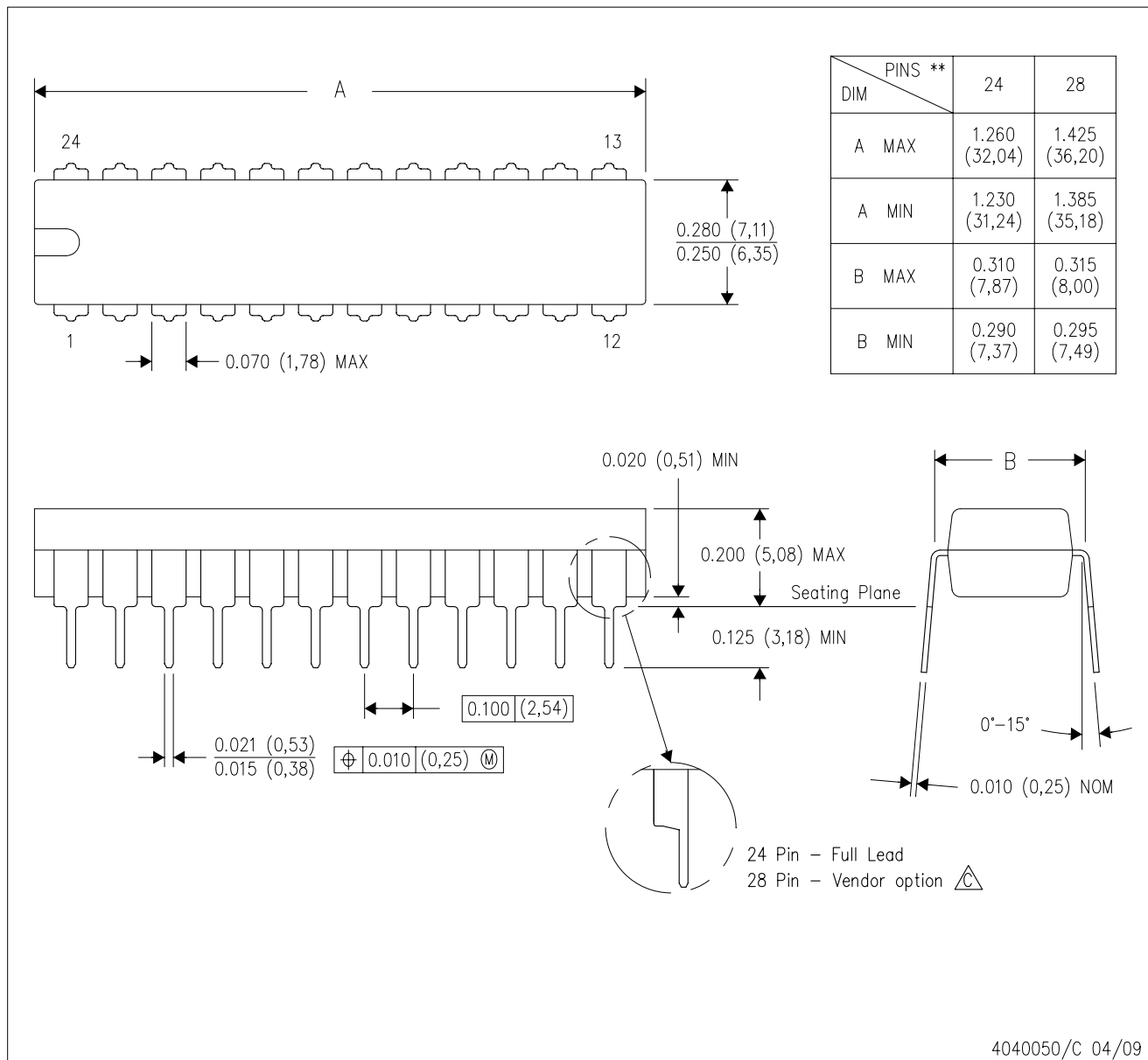NT (R−PDIP−T**)   PLASTIC DUAL−IN−LINE PACKAGE
24 PINS SHOWN

PINS ** DIM	24	28
A MAX	1.260 (32,04)	1.425 (36,20)
A MIN	1.230 (31,24)	1.385 (35,18)
B MAX	0.310 (7,87)	0.315 (8,00)
B MIN	0.290 (7,37)	0.295 (7,49)

0.280 (7,11)
0.250 (6,35)

0.070 (1,78) MAX

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)   ⊕ | 0.010 | (0,25) Ⓜ

B

0°−15°

0.010 (0,25) NOM

24 Pin − Full Lead
28 Pin − Vendor option ⚠C

4040050/C 04/09
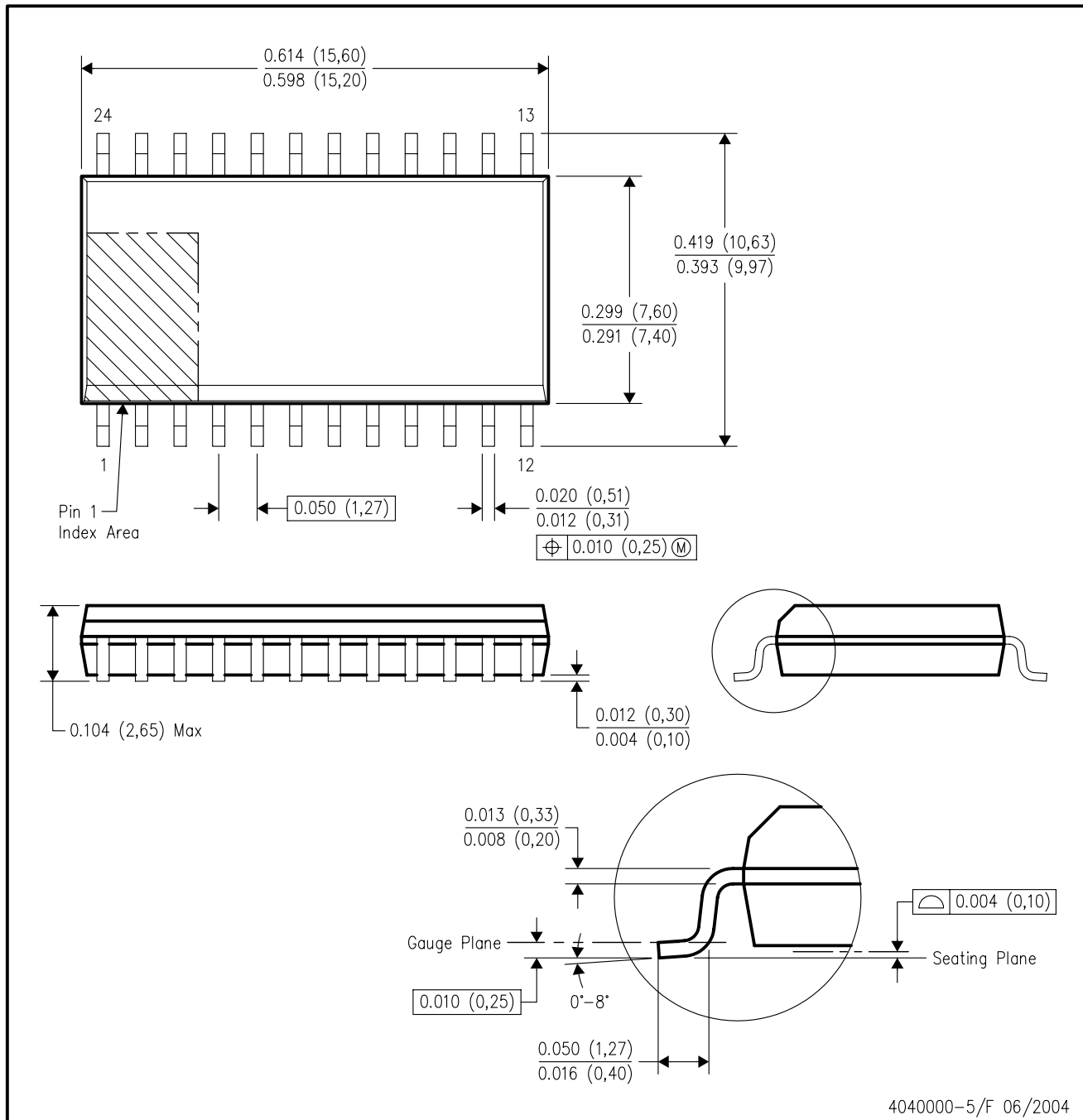
NOTES: A.   All linear dimensions are in millimeters.   Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         ⚠C   The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R−PDSO−G24)   PLASTIC SMALL−OUTLINE PACKAGE

0.614 (15,60)
0.598 (15,20)

24   13

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   12

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

Gauge Plane

0.010 (0,25)

0°−8°

0.004 (0,10)

Seating Plane

0.050 (1,27)
0.016 (0,40)

4040000−5/F 06/2004

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MS−013 variation AD.

TEXAS
INSTRUMENTS
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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
CD74HC646EN	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	Samples Not Available
CD74HC646ENE4	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	Samples Not Available
CD74HC646M	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	Samples Not Available
CD74HC646M96	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	Samples Not Available
CD74HC646M96E4	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	Samples Not Available
CD74HC646ME4	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	Samples Not Available

(1) The marketing status values are defined as follows:
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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF CD74HC646 :

● Military: CD54HC646

NOTE: Qualified Version Definitions:

● Military - QML certified for Military and Defense Applications

NT (R−PDIP−T**)   PLASTIC DUAL−IN−LINE PACKAGE
24 PINS SHOWN

DIM \ PINS **	24	28
A MAX	1.260 (32,04)	1.425 (36,20)
A MIN	1.230 (31,24)	1.385 (35,18)
B MAX	0.310 (7,87)	0.315 (8,00)
B MIN	0.290 (7,37)	0.295 (7,49)

A

24   13

0.280 (7,11)
0.250 (6,35)

1   12

0.070 (1,78) MAX

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)   ⊕ 0.010 (0,25) Ⓜ

B

0°−15°

0.010 (0,25) NOM

24 Pin − Full Lead
28 Pin − Vendor option ⚠C

4040050/C 04/09

NOTES: A.   All linear dimensions are in millimeters.   Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         ⚠C   The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R−PDSO−G24) PLASTIC SMALL−OUTLINE PACKAGE

0.614 (15,60)
0.598 (15,20)

24   13

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   12

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

◯ 0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040000−5/F 06/2004

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D. Falls within JEDEC MS−013 variation AD.

IMPORTANT NOTICE