

Field Programmable Blank Oscillator

Series **CPPFX**

- Programmed with the PG-2000P, PG-3000 field oscillator programming instrument within seconds
- Can be programmed twice
- Provides a sealed finished custom oscillator
- Standard Package Options



Part Numbering Example: CPPFX C 1 L Z - A5 BR - XX.XXXX TS

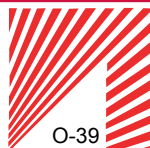
CPPFX	C	1	L	Z	A7	BR	XX.XXXX	TS
SERIES	OUTPUT	PACKAGE STYLE	VOLTAGE	ADDED FEATURES	OPERATING TEMP.	STABILITY	FREQUENCY	TRI-STATE
CPPFX	C = CMOS T = TTL	1 = Full Size 4 = Half Size 5 = 3.2X5 Ceramic 7 = 5X7 Ceramic 8 = PLASTIC SMD 8B = PLASTIC SMD	Blank = 5V L = 3.3 V R = 2.7 V	Blank = Bulk T = Tube Z = Tape and Reel	Blank = 0°C +70°C A7 = -40°C +85°C	BD = ±20 ppm BR = ±25 ppm	1.000~133.000 MHz	TS = Tri-State PD=PowerDwn

Specifications:

Description	Min	Typ	Max	Unit
Frequency Range: Programmable to Any Discrete Frequency	1.000		133.000	MHz
Available Stability Options:	-20 -25		20 25	ppm ppm
Programmable Supply Voltage: (1–133 MHz)	4.5	5.0	5.5	V
(1–133 MHz)	3.0	3.3	3.6	V
Operating Temperature Range Options:	0 -40		+70 +85	°C °C
Storage Temperature:	-55		+125	°C
Aging (PPM/Year) Ta=25C, Vdd=5/3.3V			±5	
Programmable Output Level: TTL/CMOS				
Packaging: Tape and Reel (1K per Reel) Tube				

Operating Conditions:

Description	Min	Max	Unit
Vdd Supply Voltage	3.0	5.5	V
CTTL Max Capacitive Load on outputs for TTL levels 4.5V–5.5V Vdd ≤ 40 MHz 4.5V–5.5V Vdd > 40–133 MHz		50	pF
		25	pF
CCMOS Max Capacitive Load on outputs for CMOS levels 4.5V–5.5V Vdd, ≤ 66 MHz 4.5V–5.5V Vdd, >66–133 MHz 3.0V–3.6V Vdd, ≤ 40 MHz 3.0V–3.6V Vdd, >40–100 MHz		50	pF
		25	pF
		30	pF
		15	pF



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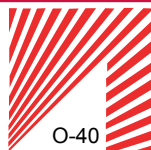
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Electrical Characteristics

Description	TEST CONDITIONS	Min	Typ	Max	Unit
Input Characteristics (Pin 1):					
V _{IL} , Low-Level Input Voltage TO TRI-STATE OR POWER DOWN	4.5–5.5V V _{dd} 3.0–3.6V V _{dd}			0.8 0.2V _{dd}	V V
V _{IH} , High-Level Input Voltage TO ENABLE OUTPUT OR OPEN	4.5–5.5V V _{dd} τ3.0–3.6V V _{dd}	2.0 0.7V _{dd}			V
I _{IL} , Input Low Current I _{IH} , Input High Current	V _{IN} = 0V V _{IN} = V _{dd}			10 5	μA μA
Output Characteristics:					
V _{OL} , Low-Level Output Voltage	4.5V–5.5V V _{dd} , 16 mA I _{oL} 3.0V–3.6V V _{dd} , 8 mA I _{oL}			0.4 0.4	V V
V _{OHTTL} , High-level Output Voltage TTL	4.5V–5.5V V _{dd} , -16 mA I _{oL}	2.4			V
V _{OHCMS} , High-level CMOS Voltage	4.5V–5.5V V _{dd} , -16 mA I _{oL} 3.0V–3.6V V _{dd} , -8 mA I _{oL}	V _{dd} -0.4 V _{dd} -0.4			V V
Power Supply Current: (unloaded)	4.5–5.5 V _{dd} , OUTPUT FREQ ≤ 133 MHz 3.0–3.6 V _{dd} , OUTPUT FREQ ≤ 100 MHz			45 25	mA mA
Standby Current:			10	50	μA
Tri State pull up (P_{IN1})	4.5–5.5 V _{dd} , V _{IN} = 0V 4.5–5.5 V _{dd} , V _{IN} = 0.7V	1.1 50	3.0 100	8.0 200	MΩ KΩ
Tri-State Leakage Current	5.0 V _{dd}		20		μA
Output Enable Mode:	Output is Tri-Stated				
Power Down Mode:	Output is Tri-Stated.				

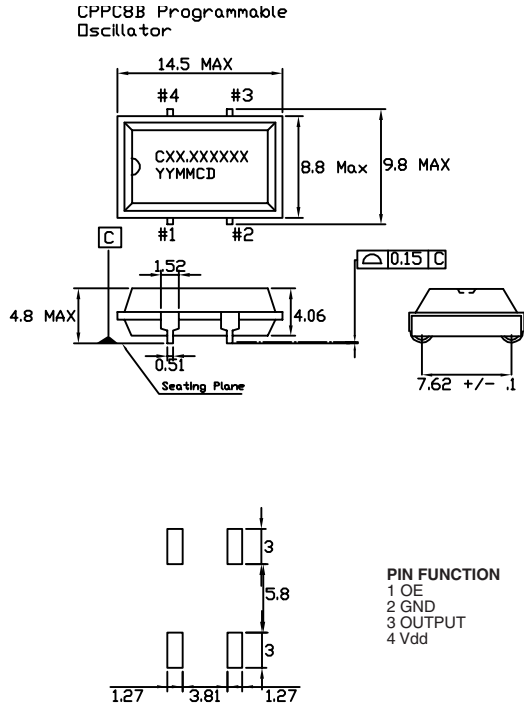
"Tristate internal pull up. Output active when high"



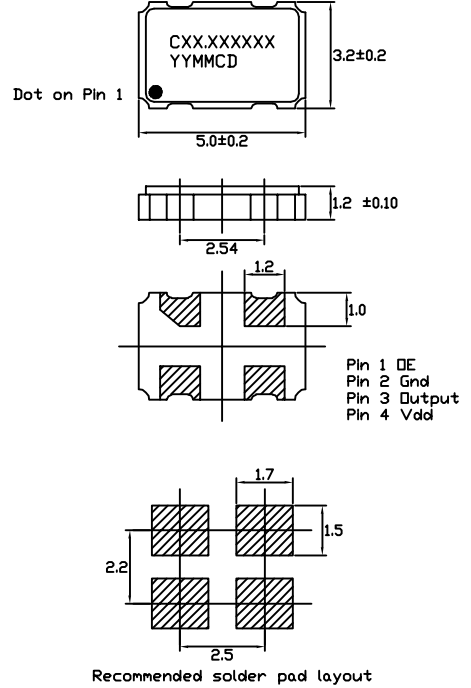
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Note: *Bypass Vdd to GND with a 0.01 μF capacitor*

Style 8B Plastic SMD



Style 5 3.2x5 Ceramic SMD

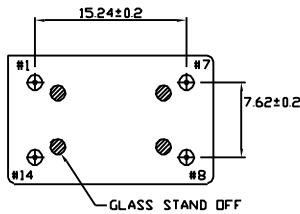
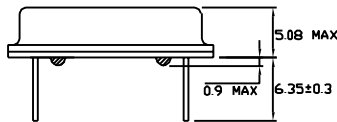
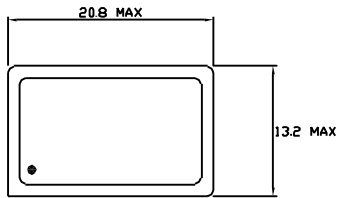


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Note: Bypass Vdd to GND with a 0.01 μ F capacitor

Style 1 Full Size 14 Pin Dip

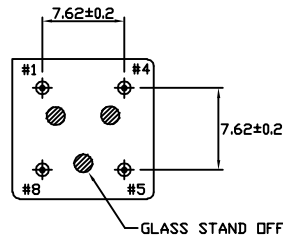
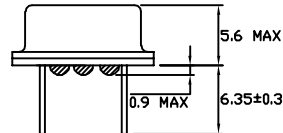
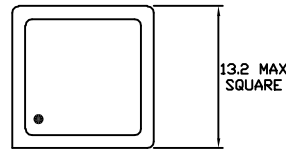
STYLE 1 FULL SIZE 14 PIN DIP



PIN FUNCTION
 1 CONTROL
 7 GND
 8 OUTPUT
 14 Vdd

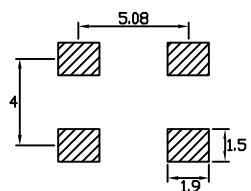
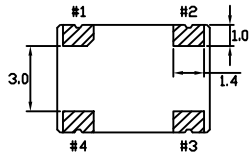
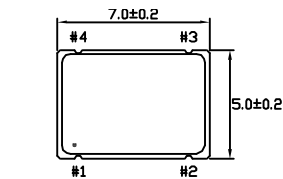
Style 4 Half Size 8 Pin Dip

STYLE 4 HALFSIZE 8 PIN DIP



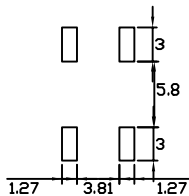
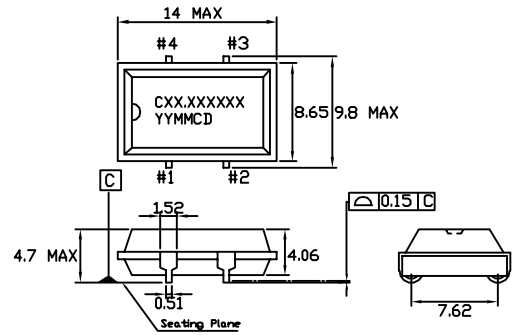
PIN FUNCTION
 1 CONTROL
 4 GND
 5 OUTPUT
 8 Vdd

Style 7 5x7 Ceramic SMD



PIN FUNCTION
 1 CONTROL
 2 GND
 3 OUTPUT
 4 Vdd

Style 8 Plastic SMD



PIN FUNCTION
 1 CONTROL
 2 GND
 3 OUTPUT
 4 Vdd

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Output Clock Switching Characteristics

Description	TEST CONDITIONS	Min	Typ	Max	Unit
Duty Cycle: TTL @ 1.4 V 4.5-5.5 Vdd	≤ 50 MHz, C _L = 50 pF	45		55	%
	50-66 MHz, C _L = 15 pF	45		55	%
	66-125 MHz, C _L = 25 pF	40		60	%
	125-133 MHz, C _L = 15 pF	40		60	%
Duty Cycle: CMOS @ Vdd/2 4.5-5.5 Vdd 3.0-3.6 Vdd	≤ 66 MHz, C _L ≤ 25 pF	45		55	%
	66-125 MHz, C _L ≤ 25 pF	40		60	%
	125-133 MHz, C _L ≤ 15 pF	40		60	%
	≤ 40 MHz, C _L ≤ 30 pF	45		55	%
	40-100 MHz, C _L ≤ 15 pF	40		60	%
Output Clock Rise/Fall	0.8V-2.0V, 4.5-5.5 Vdd, C _L = 50			1.8	ns
	0.8V-2.0V, 4.5-5.5 Vdd, C _L = 25			1.2	ns
	0.8V-2.0V, 4.5-5.5 Vdd, C _L = 15			0.9	ns
	0.2-0.8Vdd, 4.5-5.5 Vdd, C _L = 50			3.4	ns
	0.2-0.8Vdd, 3.0-3.6 Vdd, C _L = 30			4.0	ns
	0.2-0.8Vdd, 3.0-3.6 Vdd, C _L = 15			2.4	ns
Start Up Time	From power on			10	ms
Power Down Delay Time Synchronous Asynchronous	PWR_DWN pin LOW to output Hi-Z		T/2	T+10	ns
			10	15	ns
Output Disable Time Synchronous Asynchronous	OE pin LOW to output Hi-Z T = Frequency oscillator period		T/2	T+10	ns
			10	15	ns
Output Enable Time				100	n
RMS Period Jitter:	≤ 33.000 MHz		11	13	ps
	> 33.000, MHz		8	11	ps
Peak to Peak	≤ 33.000 MHz		80	110	ps
	> 33.000 MHz		65	80	ps

