CY14E256L

256 Kbit (32K x 8) nvSRAM

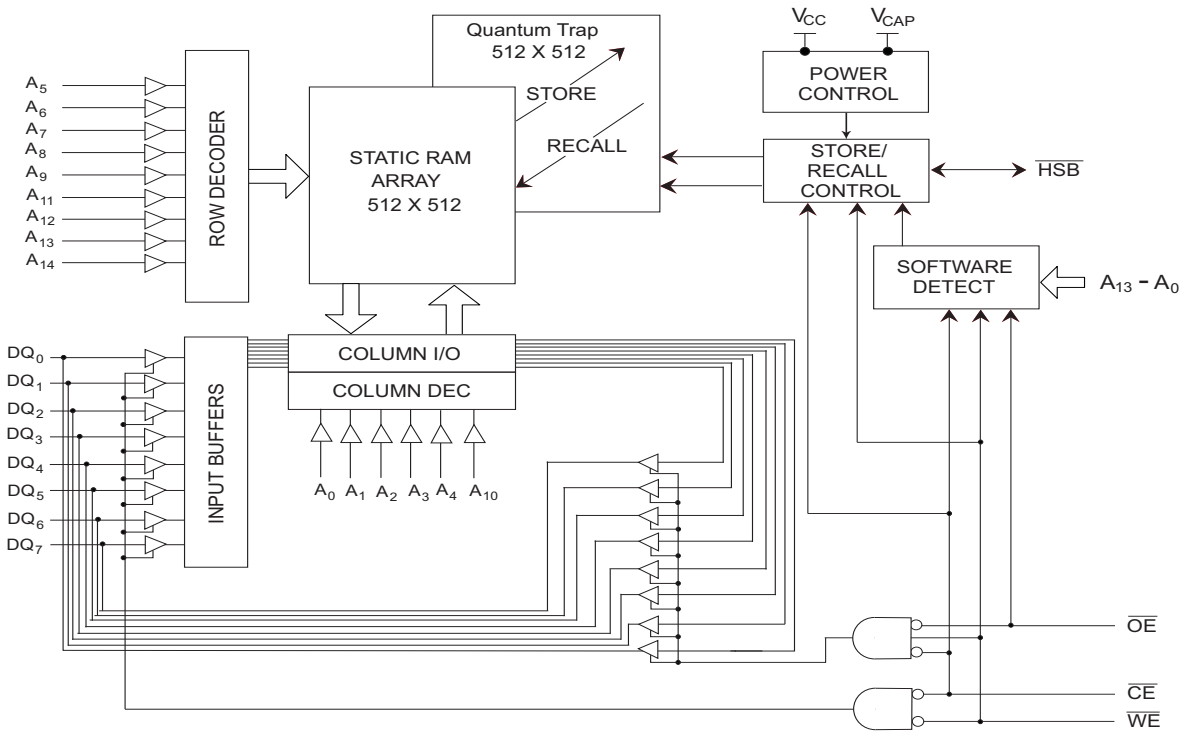
Features

- 25 ns and 45 ns access times
- Hands off Automatic STORE on power down with external 68 μF capacitor
- STORE to QuantumTrap™ nonvolatile elements is initiated by software, hardware, or AutoStore™ on power down
- RECALL to SRAM Initiated by software or power up
- Infinite READ, WRITE, and RECALL cycles
- 15 mA typical ICC at 200 ns cycle time
- 1,000,000 STORE cycles to QuantumTrap
- 100 year data retention to QuantumTrap
- Single 5V operation +10%
- Commercial temperature
- SOIC package
- RoHS compliance

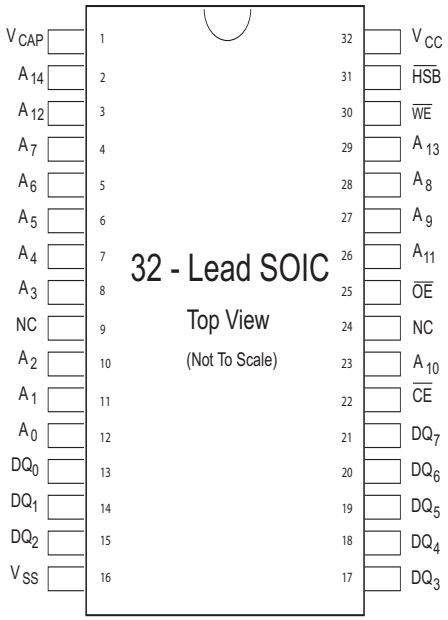
Functional Description

The Cypress CY14E256L is a fast static RAM with a nonvolatile element in each memory cell. The embedded nonvolatile elements incorporate QuantumTrap technology producing the world's most reliable nonvolatile memory. The SRAM provides infinite read and write cycles, while independent, nonvolatile data resides in the highly reliable QuantumTrap cell. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power down. On power up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. Both the STORE and RECALL operations are also available under software control. A hardware STORE is initiated with the HSB pin.

Logic Block Diagram



Pin Configurations



Pin Definitions

Pin Name	IO Type	Description
A_0–A_{14}	Input	**Address Inputs.** Used to select one of the 32,768 bytes of the nvSRAM.
DQ0-DQ7	Input or Output	**Bidirectional Data IO Lines**. Used as input or output lines depending on operation.
$\overline{WE}$	Input	**Write Enable Input, Active LOW**. When selected LOW, this writes data on the IO pins to the address location latched by the falling edge of $\overline{CE}$.
$\overline{CE}$	Input	**Chip Enable Input, Active LOW**. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{OE}$	Input	**Output Enable, Active LOW**. The active LOW $\overline{OE}$ input enables the data output buffers during read cycles. Deasserting $\overline{OE}$ HIGH causes the IO pins to tri-state.
V_{SS}	Ground	**Ground for the Device**. It is connected to ground of the system.
V_{CC}	Power Supply	**Power Supply Inputs to the Device**.
$\overline{HSB}$	Input or Output	**Hardware Store Busy (HSB)**. When low, this output indicates a Hardware Store is in progress. When pulled low external to the chip, it initiates a nonvolatile STORE operation. A weak internal pull up resistor keeps this pin HIGH if not connected (connection optional).
V_{CAP}	Power Supply	**Autostore Capacitor**. Supplies power to nvSRAM during power loss to store data from SRAM to nonvolatile elements.
NC	No Connect	**No Connect**. This pin is not connected to the die.

Device Operation

The CY14E256L nvSRAM is made up of two functional components paired in the same physical cell. These are an SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM is transferred to the nonvolatile cell (the STORE operation) or from the nonvolatile cell to SRAM (the RECALL operation). This unique architecture enables storage and recall of all cells in parallel. During the STORE and RECALL operations, SRAM READ and WRITE operations are inhibited. The CY14E256L supports infinite reads and writes similar to a typical SRAM. In addition, it provides infinite RECALL operations from the nonvolatile cells and up to one million STORE operations.

SRAM Read

The CY14E256L performs a READ cycle whenever $\overline{CE}$ and $\overline{OE}$ are LOW while $\overline{WE}$ and $\overline{HSB}$ are HIGH. The address specified on pins $A_{0–14}$ determines which of the 32,768 data bytes are accessed. When the READ is initiated by an address transition, the outputs are valid after a delay of t_{AA} (READ cycle 1). If the READ is initiated by $\overline{CE}$ or $\overline{OE}$, the outputs are valid at t_{ACE} or at t_{DOE}, whichever is later (READ cycle 2). The data outputs repeatedly respond to address changes within the t_{AA} access time without the need for transitions on any control input pins. They remain valid until another address change or until $\overline{CE}$ or $\overline{OE}$ is brought HIGH, or $\overline{WE}$ or $\overline{HSB}$ is brought LOW.

SRAM Write

A WRITE cycle is performed whenever $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{HSB}$ is HIGH. The address inputs are stable prior to entering the WRITE cycle and must remain stable until either $\overline{CE}$ or $\overline{WE}$ goes HIGH at the end of the cycle. The data on the common IO pins $IO_{0–7}$ is written into the memory if it is valid t_{SD} before the end of a $\overline{WE}$ controlled WRITE or before the end of an $\overline{CE}$ controlled WRITE. Keep $\overline{OE}$ HIGH during the entire WRITE cycle to avoid data bus contention on common IO lines. If $\overline{OE}$ is left LOW, internal circuitry turns off the output buffers t_{HZWE} after $\overline{WE}$ goes LOW.

AutoStore Operation

The CY14E256L stores data to nvSRAM using one of three storage operations:

1. Hardware store activated by $\overline{HSB}$
2. Software store activated by an address sequence
3. AutoStore on device power down

AutoStore operation is a unique feature of QuantumTrap technology and is enabled by default on the CY14E256L.

During normal operation, the device draws current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge is used by the chip to perform a single STORE operation. If the voltage on the V_{CC} pin drops below V_{SWITCH}, the part automatically disconnects the V_{CAP} pin from V_{CC}. A STORE operation is initiated with power provided by the V_{CAP} capacitor.

Figure 1 shows the proper connection of the storage capacitor (V_{CAP}) for automatic store operation. Refer to the “” on page 6 for the size of V_{CAP}. The voltage on the V_{CAP} pin is driven to 5V by a charge pump internal to the chip. A pull up is placed on $\overline{WE}$ to hold it inactive during power up.

Figure 1. AutoStore Mode

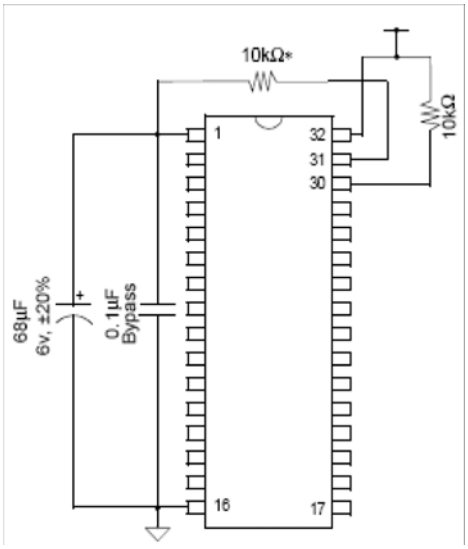
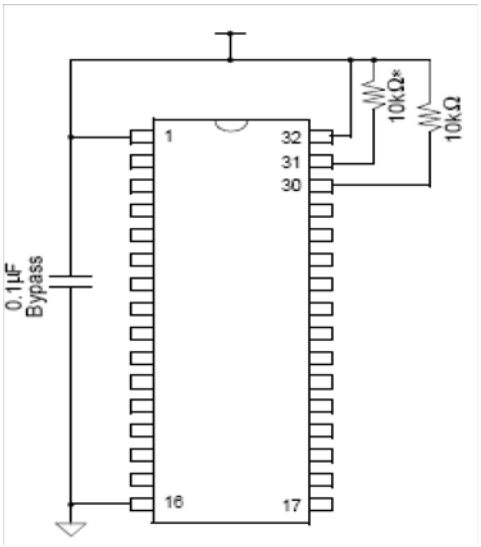


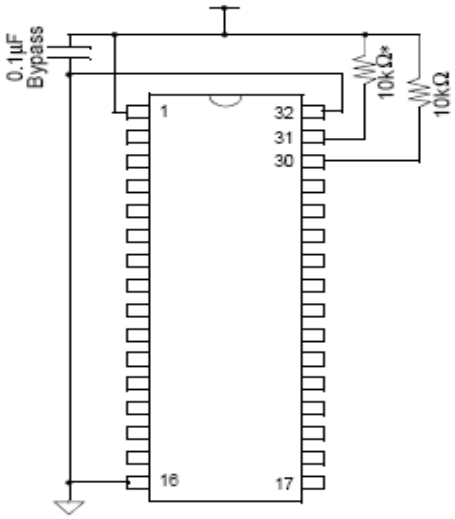
Figure 2. System Power Mode



In system power mode (Figure 2), both V_{CC} and V_{CAP} are connected to the +5V power supply without the 68 µF capacitor. In this mode, the AutoStore function of the CY14E256L operates on the stored system charge as power goes down. The user must, however, guarantee that V_{CC} does not drop below 3.6V during the 10 ms STORE cycle.

If an automatic STORE on power loss is not required, then V_{CC} is tied to ground and + 5V is applied to V_{CAP} (Figure 3). This is the AutoStore Inhibit mode where the AutoStore function is disabled. If the CY14E256L is operated in this configuration, references to V_{CC} is changed to V_{CAP} throughout this data sheet. In this mode, STORE operations are triggered through software control or the $\overline{HSB}$ pin. It is not permissible to change between these three options at will.

Figure 3. AutoStore Inhibit Mode



To reduce unnecessary nonvolatile stores, AutoStore and Hardware Store operations are ignored unless at least one WRITE operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a WRITE operation has taken place. The HSB signal is monitored by the system to detect if an AutoStore cycle is in progress. (In the above, Figure 1, Figure 2, and Figure 3 indicate that If HSB is not used, it is left unconnected.)

Hardware STORE ($\overline{HSB}$) Operation

The CY14E256L provides the $\overline{HSB}$ pin for controlling and acknowledging the STORE operations. The HSB pin is used to request a hardware STORE cycle. When the HSB pin is driven low, the CY14E256L conditionally initiates a STORE operation after t_{DELAY}. An actual STORE cycle only begins if a WRITE to the SRAM took place since the last STORE or RECALL cycle. The $\overline{HSB}$ pin also acts as an open drain driver that is internally driven LOW to indicate a busy condition, while the STORE (initiated by any means) is in progress.

SRAM READ and WRITE operations that are in progress when HSB is driven LOW by any means are given time to complete before the STORE operation is initiated. After HSB goes LOW, the CY14E256L continues SRAM operations for t_{DELAY}. During t_{DELAY}, multiple SRAM READ operations take place. If a WRITE is in progress when $\overline{HSB}$ is pulled LOW, it is allowed a time, t_{DELAY}, to complete. However, any SRAM WRITE cycles requested after $\overline{HSB}$ goes LOW is inhibited until $\overline{HSB}$ returns HIGH.

The $\overline{HSB}$ pin is used to synchronize multiple CY14E256L while using a single larger capacitor. To operate in this mode, the HSB pin is connected together to the HSB pins from the other CY14E256L. An external pull up resistor to +5V is required, since HSB acts as an open drain pull down. The V_{CAP} pins from the other CY14E256L parts are tied together and share a single capacitor. The capacitor size is scaled by the number of devices connected to it. When any one of the CY14E256L detects a power loss and asserts HSB, the common HSB pin causes all parts to request a STORE cycle. (A STORE takes place in those CY14E256L that are written since the last nonvolatile cycle.)

During any STORE operation, regardless of how it is initiated, the CY14E256L continues to drive the HSB pin low, releasing it only when the STORE is complete. After completing the STORE operation, the CY14E256L remains disabled until the $\overline{HSB}$ pin returns HIGH.

If $\overline{HSB}$ is not used, it is left unconnected.

Hardware RECALL (Power Up)

During power up or after any low power condition (V_{CC} greater than V_{SWITCH}), an internal RECALL request is latched. When V_{CC} once again exceeds the sense voltage of V_{SWITCH}, a RECALL cycle is automatically initiated and takes $t_{HRECALL}$ to complete.

If the CY14E256L is in a WRITE state at the end of power up RECALL, the SRAM data is corrupted. To help avoid this situation, a 10 Kohm resistor is connected either between WE and system V_{CC} or between CE and system V_{CC}.

Software STORE

Data transfers from the SRAM to the nonvolatile memory by a software address sequence. The CY14E256L software STORE cycle is initiated by executing sequential CE controlled READ cycles from six specific address locations in exact order. During the STORE cycle, an erase of the previous nonvolatile data is first performed followed by a program of the nonvolatile elements. When a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for STORE initiation, it is important that no other READ or WRITE accesses intervene in the sequence. If the READ or WRITE accesses intervene, the sequence is aborted and no STORE or RECALL takes place.

To initiate the software STORE cycle, the following READ sequence is performed:

1. Read address 0x0E38, Valid READ
2. Read address 0x31C7, Valid READ
3. Read address 0x03E0, Valid READ
4. Read address 0x3C1F, Valid READ
5. Read address 0x303F, Valid READ
6. Read address 0x0FC0, Initiate STORE cycle

The software sequence is clocked with $\overline{CE}$ controlled READs or $\overline{OE}$ controlled READs. When the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled. It is important that READ cycles and not WRITE cycles are used in the sequence. It is not necessary that $\overline{OE}$ is low for a valid sequence. After the t_{STORE} cycle time is fulfilled, the SRAM is again activated for READ and WRITE operation.

Software RECALL

Data transfers from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of $\overline{CE}$ controlled READ operations is performed:

1. Read address 0x0E38, Valid READ
2. Read address 0x31C7, Valid READ
3. Read address 0x03E0, Valid READ
4. Read address 0x3C1F, Valid READ
5. Read address 0x303F, Valid READ
6. Read address 0x0C63, Initiate RECALL cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and then the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time, the SRAM is once again ready for READ and WRITE operations. The RECALL operation in no way alters the data in the nonvolatile elements.

Data Protection

The CY14E256L protects data from corruption during low voltage conditions by inhibiting all externally initiated STORE and WRITE operations. The low voltage condition is detected when V_{CC} is less than V_{SWITCH}. If the CY14E256L is in a WRITE mode (both $\overline{CE}$ and $\overline{WE}$ are LOW) at power up, after a RECALL or after a STORE, the WRITE is inhibited until a negative transition on $\overline{CE}$ or $\overline{WE}$ is detected. This protects against inadvertent writes during power up or brown out conditions.

Noise Considerations

The CY14E256L is a high speed memory. It has a high frequency bypass capacitor of approximately 0.1 µF connected between V_{CC} and V_{SS}, using leads and traces that are as short as possible. As with all high speed CMOS ICs, careful routing of power, ground, and signals reduce circuit noise.

Low Average Active Power

CMOS technology provides the CY14E256L the benefit of drawing significantly less current when it is cycled at times longer than 50 ns. Figure 4 shows the relationship between I_{CC} and READ/WRITE cycle time. Worst case current consumption is shown for both CMOS and TTL input levels (commercial temperature range, VCC = 5.5V, 100% duty cycle on chip enable).

.

Figure 4. Current versus Cycle Time (READ)

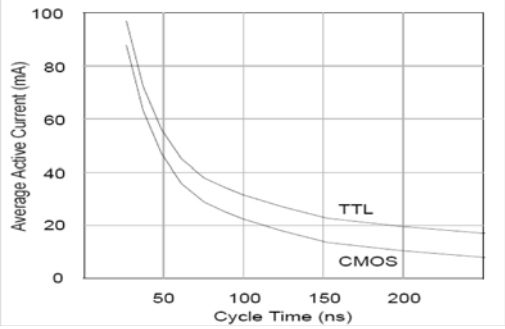
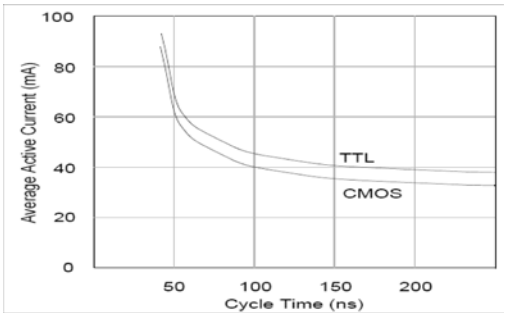


Figure 5. Current versus Cycle Time (WRITE)



Only standby current is drawn when the chip is disabled. The overall average current drawn by the CY14E256L depends on the following items:

1. The duty cycle of chip enable
2. The overall cycle rate for accesses
3. The ratio of READs to WRITEs
4. CMOS vs. TTL input levels
5. The operating temperature
6. The V_{CC} level
7. IO loading

Preventing STOREs

The STORE function is disabled by holding $\overline{HSB}$ HIGH with a driver capable of sourcing 30 mA at a V_{OH} of at least 2.2V. This overpowers the internal pull down device that drives $\overline{HSB}$ LOW for 20 µs at the onset of a STORE. When the CY14E256L is connected for AutoStore operation (system V_{CC} connected to V_{CC} and a 68 µF capacitor on V_{CAP}) and V_{CC} crosses V_{SWITCH} on the way down, the CY14E256L attempts to pull $\overline{HSB}$ LOW. If $\overline{HSB}$ does not actually get below V_{IL}, the part stops trying to pull $\overline{HSB}$ LOW and abort the STORE attempt.

Table 1. Hardware Mode Selection

$\overline{CE}$	$\overline{WE}$	$\overline{HSB}$	A13–A0	Mode	IO	Power
H	X	H	X	Not Selected	Output High Z	Standby
L	H	H	X	Read SRAM	Output Data	Active
L	L	H	X	Write SRAM	Input Data	Active
X	X	L	X	Nonvolatile STORE	Output High Z	I_{CC2}

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage on V_{CC} Relative to GND .....–0.5V to 7.0V

Voltage Applied to Outputs in High Z State ..... –0.5V to V_{CC} + 0.5V

Input Voltage.....–0.5V to Vcc+0.5V

Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... –2.0V to V_{CC} + 2.0V

Package Power Dissipation Capability (T_A = 25°C) 1.0W

Surface Mount Lead Soldering Temperature (3 Seconds) ..... +260°C

Output Short Circuit Current [1] ..... 15 mA

Static Discharge Voltage..... > 2001V (MIL-STD-883, Method 3015)

Latch Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	4.5V to 5.5V

DC Electrical Characteristics

Over the Operating Range (V_{CC} = 4.5V to 5.5V) [2]

Parameter	Description	Test Conditions		Min	Max	Unit
I_{CC1}	Average V_{CC} Current	t_{RC} = 25 ns t_{RC} = 45 ns Dependent on output loading and cycle rate. Values obtained without output loads. I_{OUT} = 0 mA.	Commercial		97 70	mA mA mA
I_{CC2}	Average V_{CC} Current during STORE	All inputs do not care, V_{CC} = Max. Average current for duration t_{STORE}			3	mA
I_{CC3}	Average V_{CC} Current at t_{AVAV} = 200 ns, 5V, 25°C Typical	$\overline{WE}$ > (V_{CC} – 0.2). All other inputs cycling. Dependent on output loading and cycle rate. Values obtained without output loads.			15	mA
I_{CC4}	Average V_{CAP} Current during AutoStore Cycle	All Inputs do not care, V_{CC} = Max. Average current for duration t_{STORE}.			2	mA
I_{SB}	V_{CC} Standby Current	$\overline{CE}$ > (V_{CC} – 0.2). All others V_{IN} < 0.2V or > (V_{CC} – 0.2V). Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0 MHz.			1.5	mA
I_{IX}	Input Leakage Current	V_{CC} = Max, $V_{SS} \le V_{IN} \le V_{CC}$		-1	+1	µA
I_{OZ}	Off State Output Leakage Current	V_{CC} = Max, $V_{SS} \le V_{IN} \le V_{CC}$, $\overline{CE}$ or $\overline{OE}$ > V_{IH}		-5	+5	µA
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			V_{SS} – 0.5	0.8	V
V_{OH}	Output HIGH Voltage	I_{OUT} = –2 mA		2.4		V
V_{OL}	Output LOW Voltage	I_{OUT} = 4 mA			0.4	V

Notes
1. Outputs shorted for no more than one second. No more than one output shorted at a time.
2. Typical conditions for the Active Current shown on the front page of the data sheet are average values at 25°C (room temperature) and V_{CC} = 5V. Not 100% tested.

Capacitance

These parameters are guaranteed but not tested.

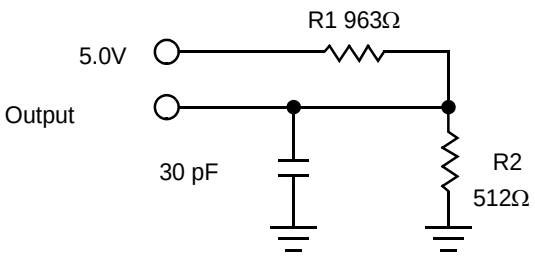
Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 0 to 3.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

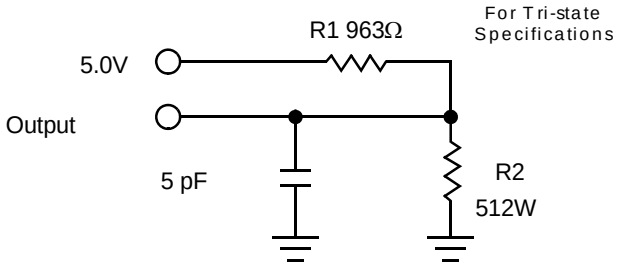
Thermal Resistance

These parameters are guaranteed but not tested.

Parameter	Description	Test Conditions	32-SOIC	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	TBD	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		TBD	°C/W

AC Test Loads





AC Test Conditions

Input Pulse Levels .....0V to 3V
Input Rise and Fall Times (10% - 90%) ..... ≤5 ns
Input and Output Timing Reference Levels 1.5V

AC Switching Characteristics

Parameter		Description	25 ns Part		45 ns Part		Unit
Cypress Parameter	Alt. Parameter		Min	Max	Min	Max	
SRAM Read Cycle							
t_{ACE}	t_{ACS}	Chip Enable Access Time		25		45	ns
t_{RC} [4]	t_{RC}	Read Cycle Time	25		45		ns
t_{AA} [5]	t_{AA}	Address Access Time		25		45	ns
t_{DOE}	t_{OE}	Output Enable to Data Valid		10		20	ns
t_{OHA} [5]	t_{OH}	Output Hold After Address Change	5		5		ns
t_{LZCE} [6]	t_{LZ}	Chip Enable to Output Active	5		5		ns
t_{HZCE} [6]	t_{HZ}	Chip Disable to Output Inactive		10		15	ns
t_{LZOE} [6]	t_{OLZ}	Output Enable to Output Active	0		0		ns
t_{HZOE} [6]	t_{OHZ}	Output Disable to Output Inactive		10		15	ns
t_{PU} [3]	t_{PA}	Chip Enable to Power Active	0		0		ns
t_{PD} [3]	t_{PS}	Chip Disable to Power Standby		25		45	ns
t_{WC}	t_{WC}	Write Cycle Time	25		45		ns
t_{PWE}	t_{WP}	Write Pulse Width	20		30		ns
t_{SCE}	t_{CW}	Chip Enable to End of Write	20		30		ns
t_{SD}	t_{DW}	Data Setup to End of Write	10		15		ns
t_{HD}	t_{DH}	Data Hold After End of Write	0		0		ns
t_{AW}	t_{AW}	Address Setup to End of Write	20		30		ns
t_{SA}	t_{AS}	Address Setup to Start of Write	0		0		ns
t_{HA}	t_{WR}	Address Hold After End of Write	0		0		ns
t_{HZWE} [6,7]	t_{WZ}	Write Enable to Output Disable		10		14	ns
t_{LZWE} [6]	t_{OW}	Output Active After End of Write	5		5		ns

AutoStore or Power Up RECALL

Parameter	Description	CY14E256L		Unit
		Min	Max	
$t_{HRECALL}$ [8]	Power Up RECALL Duration		550	µs
t_{STORE} [9]	STORE Cycle Duration		10	ms
V_{SWITCH}	Low Voltage Trigger Level	4.0	4.5	V
$t_{VCCRISE}$	V_{CC} Rise Time	150		µs

Notes
3. These parameters are guaranteed but not tested
4. $\overline{WE}$ must be HIGH during SRAM Read Cycles.
5. Device is continuously selected with $\overline{CE}$ and $\overline{OE}$ both LOW.
6. Measured ±200mV from steady state output voltage.
7. If $\overline{WE}$ is LOW when $\overline{CE}$ goes LOW, the outputs remain in the high impedance state.
8. $t_{HRECALL}$ starts from the time V_{CC} rises above V_{SWITCH}.
9. If an SRAM Write has not taken place since the last nonvolatile cycle, no STORE takes place.

Software Controlled STORE or RECALL Cycle

The software controlled STORE or RECALL cycle follows. [10,11]

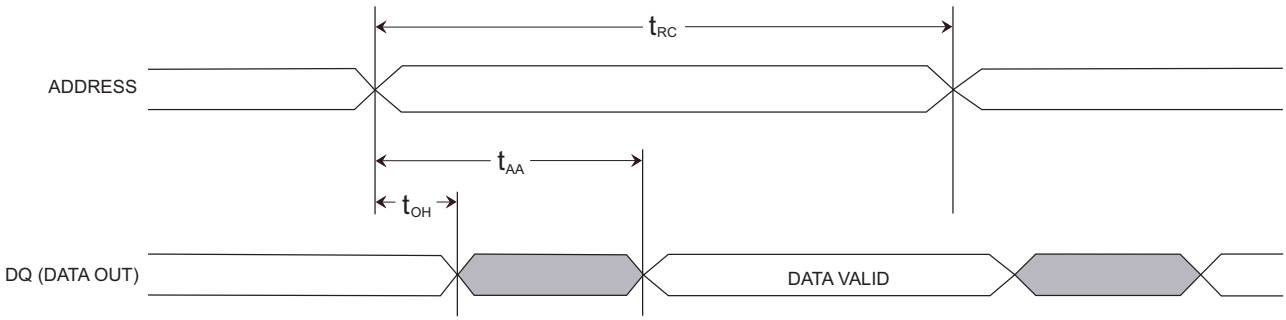
Parameter	Description	25 ns Part		45 ns Part		Unit
		Min	Max	Min	Max	
t_{RC}	STORE/RECALL Initiation Cycle Time	25		45		ns
t_{AS}	Address Setup Time	0		0		ns
t_{CW}	Clock Pulse Width	20		30		ns
t_{GLAX}	Address Hold Time	20		20		ns
t_{RECALL}	RECALL Duration		20		20	µs

Hardware STORE Cycle

Parameter	Description	CY14E256L		Unit
		Min	Max	
t_{STORE} [6]	STORE Cycle Duration		10	ms
t_{DELAY} [12]	Time Allowed to Complete SRAM Cycle	1		µs
$t_{RESTORE}$ [13]	Hardware STORE High to Inhibit Off		700	ns
t_{HLHX}	Hardware STORE Pulse Width	15		ns
t_{HLBL}	Hardware STORE Low to STORE Busy		300	ns

Switching Waveforms

Figure 6. SRAM Read Cycle Number 1: Address Controlled [4, 5, 14]



Notes
10. The software sequence is clocked with $\overline{CE}$ controlled READs.
11. The six consecutive addresses is read in the order listed in the Mode Selection table. $\overline{WE}$ is HIGH during all six consecutive cycles.
12. Read and Write cycles in progress before $\overline{HSB}$ are given this amount of time to complete.
13. $t_{RESTORE}$ is only applicable after t_{STORE} is complete.
14. $\overline{HSB}$ must remain HIGH during READ and WRITE cycles.

Switching Waveforms (continued)

Figure 7. SRAM Read Cycle Number 2: $\overline{CE}$ Controlled [4,14]

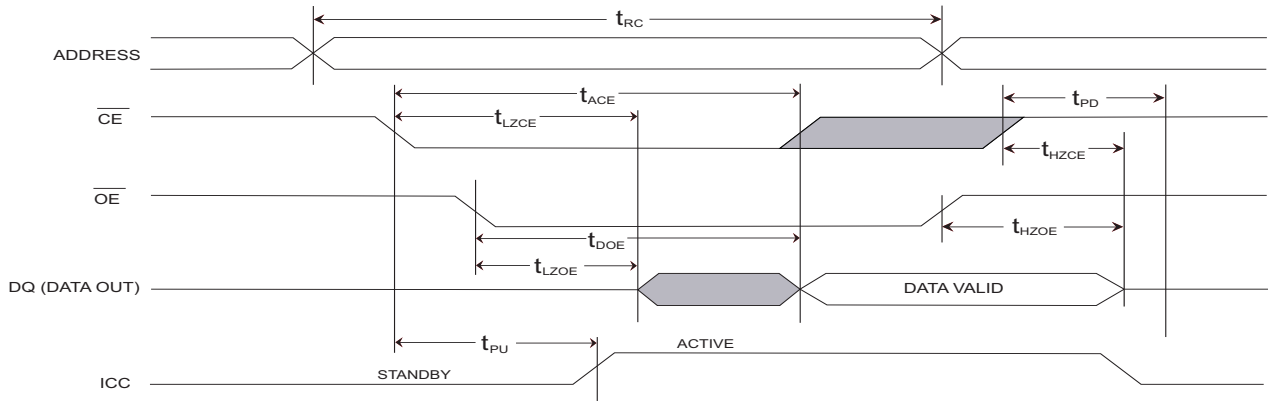
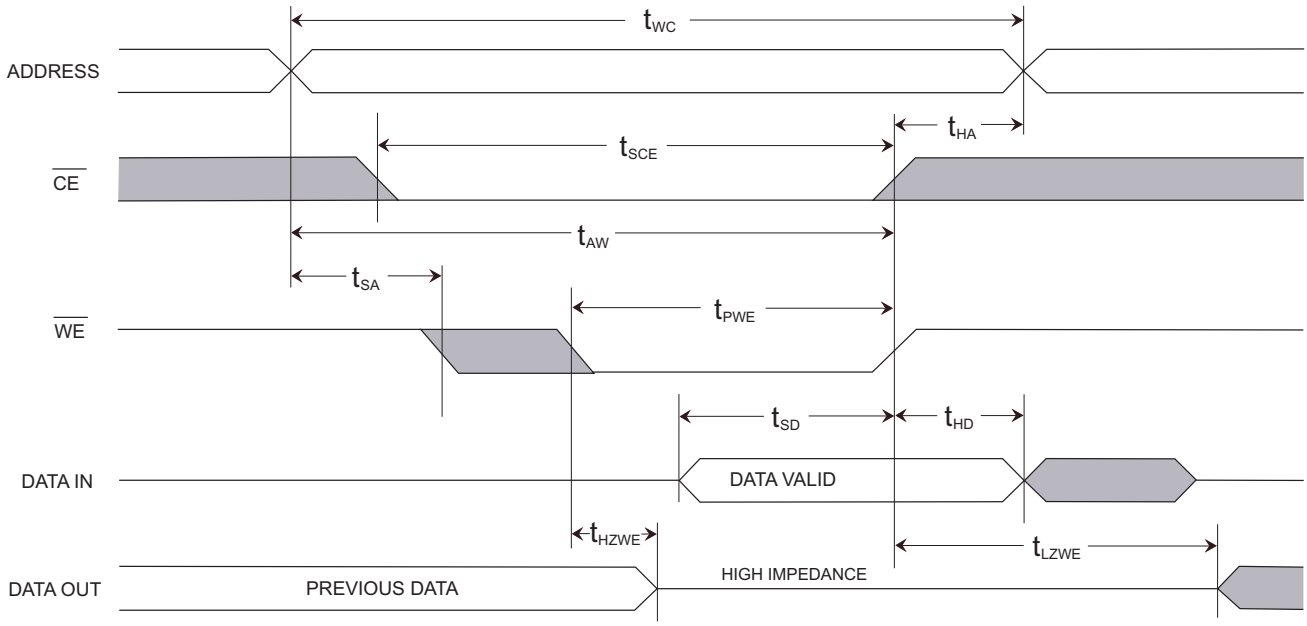


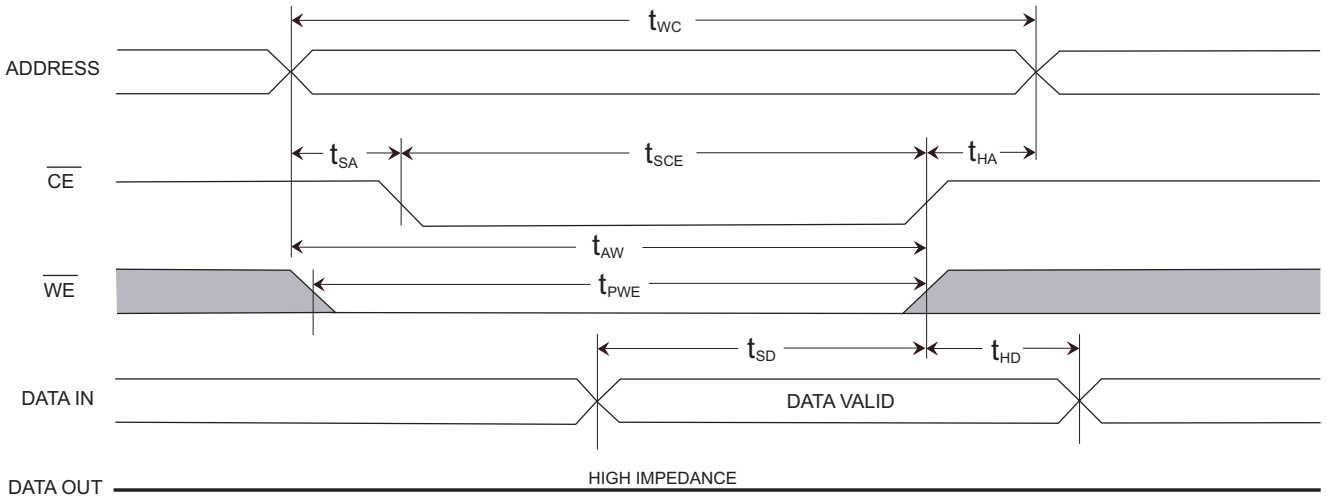
Figure 8. SRAM Write Cycle Number 1: $\overline{WE}$ Controlled [14,15]



Note
15. $\overline{CE}$ or $\overline{WE}$ is less than V_{IH} during address transitions.

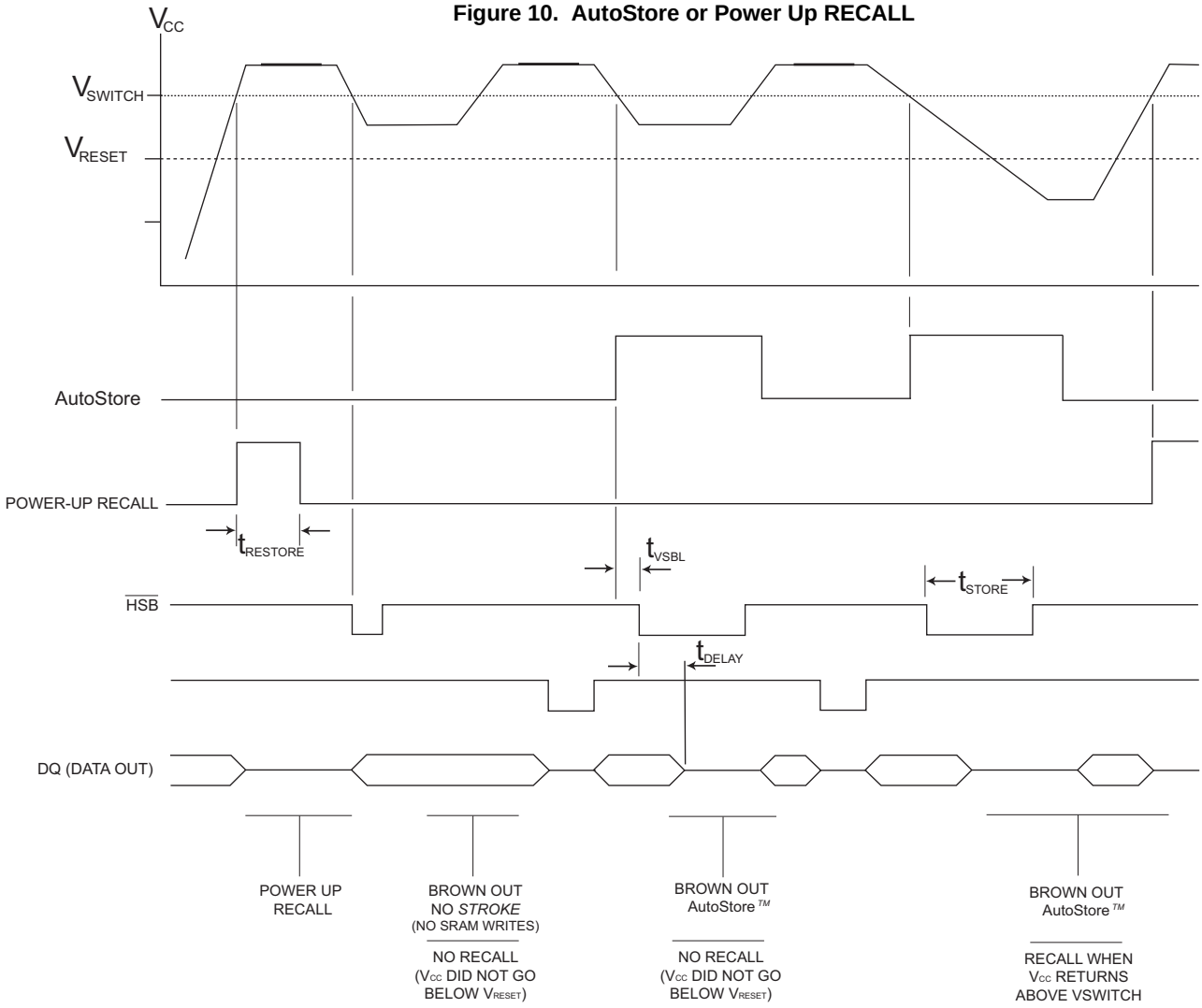
Switching Waveforms (continued)

Figure 9. SRAM Write Cycle Number 2: $\overline{CE}$ Controlled



Switching Waveforms (continued)

Figure 10. AutoStore or Power Up RECALL



Switching Waveforms (continued)

Figure 11. $\overline{CE}$ Controlled Software STORE/RECALL Cycle [11]

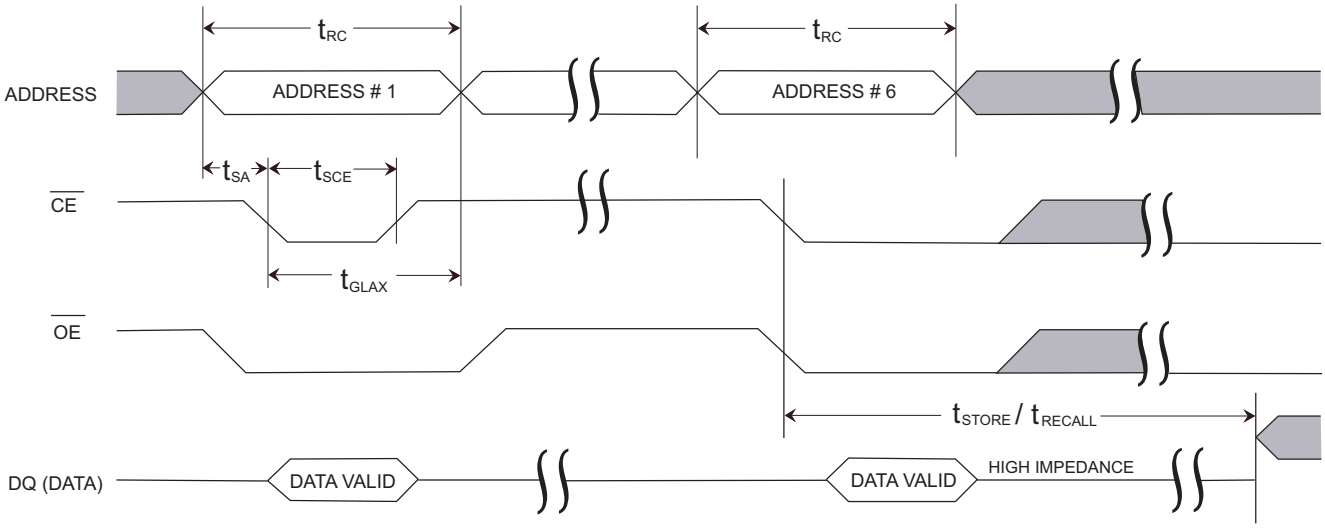
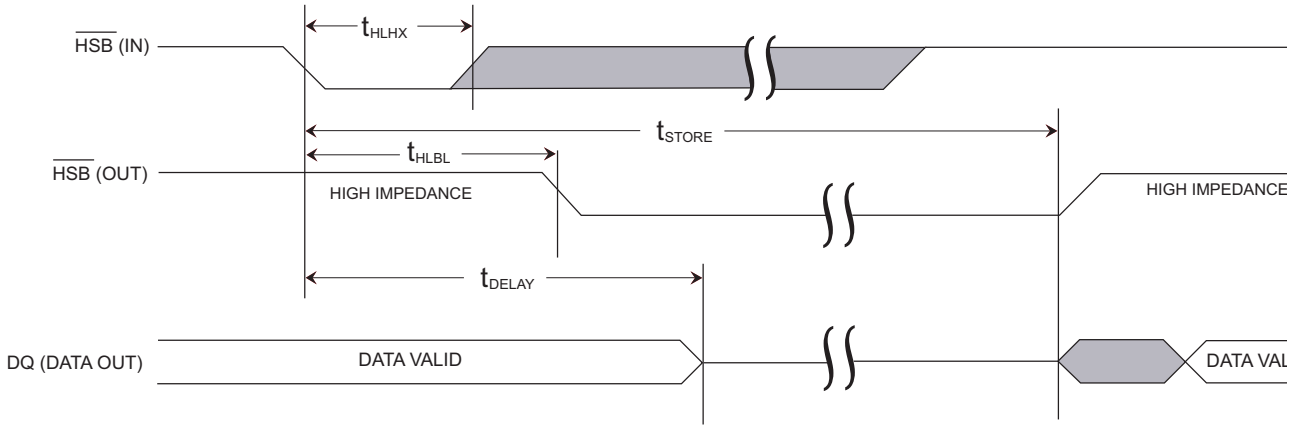
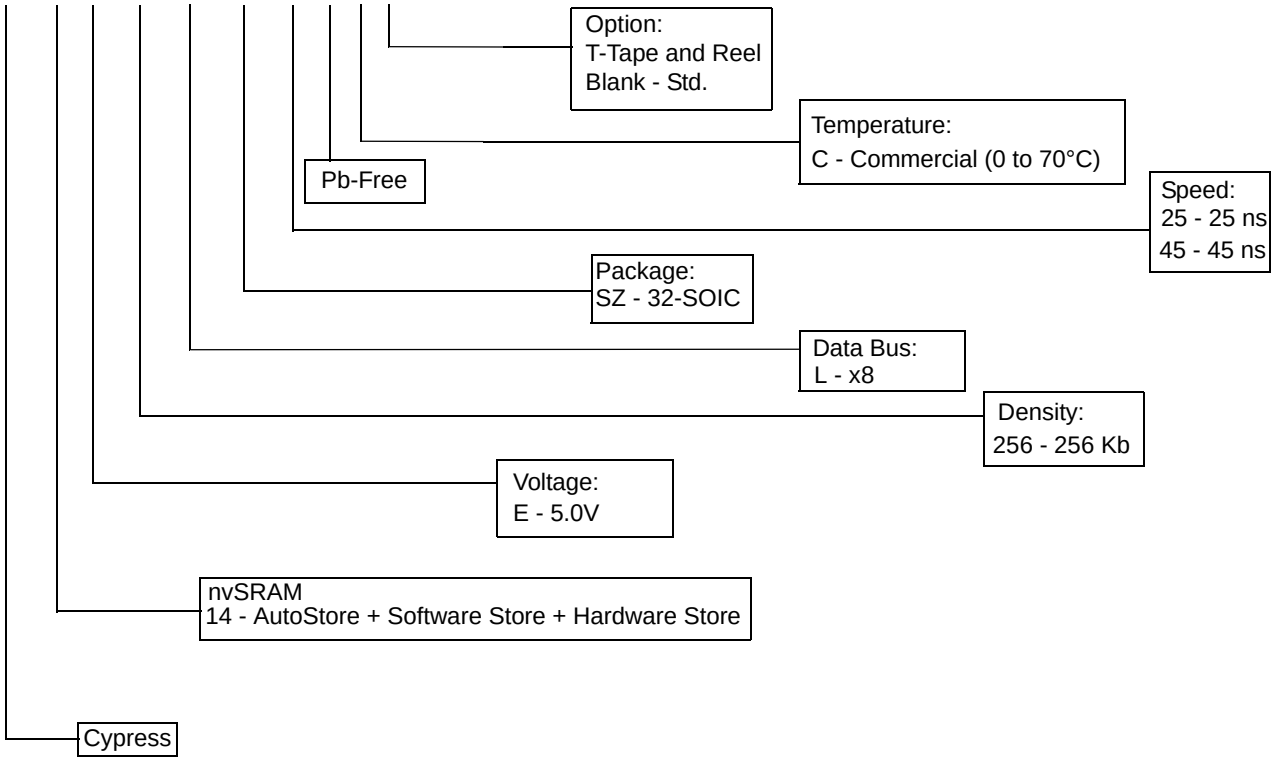


Figure 12. Hardware STORE Cycle



Part Numbering Nomenclature

CY 14 E 256 L- SZ 25 X C T

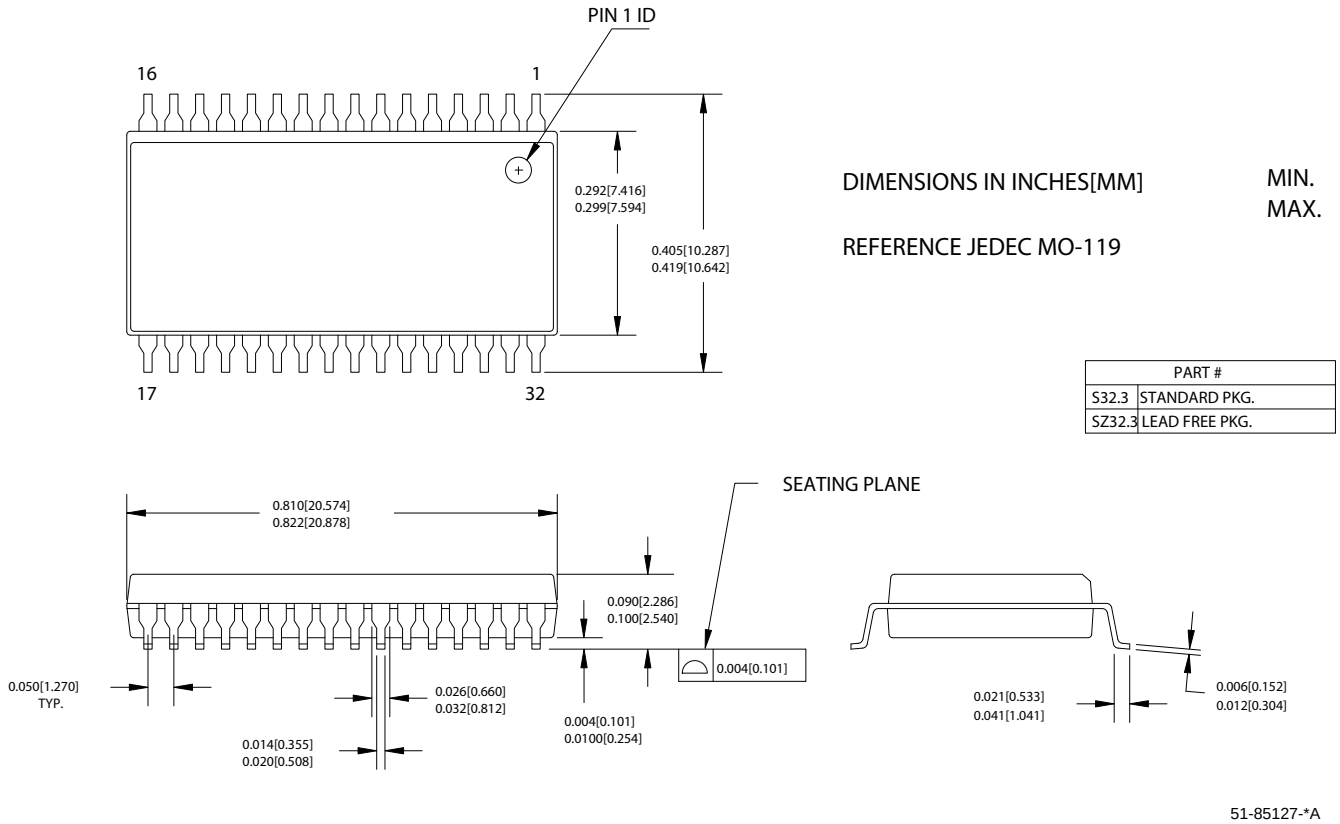


Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
25	CY14E256L-SZ25XCT	51-85127	32-pin SOIC (Pb-Free)	Commercial
	CY14E256L-SZ25XC	51-85127	32-pin SOIC (Pb-Free)	
25	CY14E256L-SZ25XIT	51-85127	32-pin SOIC (Pb-Free)	Industrial
	CY14E256L-SZ25XI	51-85127	32-pin SOIC (Pb-Free)	
35	CY14E256L-SZ35XCT	51-85127	32-pin SOIC (Pb-Free)	Commercial
	CY14E256L-SZ35XC	51-85127	32-pin SOIC (Pb-Free)	
35	CY14E256L-SZ35XIT	51-85127	32-pin SOIC (Pb-Free)	Industrial
	CY14E256L-SZ35XI	51-85127	32-pin SOIC (Pb-Free)	
45	CY14E256L-SZ45XCT	51-85127	32-pin SOIC (Pb-Free)	Commercial
	CY14E256L-SZ45XC	51-85127	32-pin SOIC (Pb-Free)	
45	CY14E256L-SZ45XIT	51-85127	32-pin SOIC (Pb-Free)	Industrial
	CY14E256L-SZ45XI	51-85127	32-pin SOIC (Pb-Free)	

Package Diagram

32-pin (300 Mil) SOIC



Document History Page

Document Title: CY14E256L 256 Kbit (32K x 8) nvSRAM Document Number: 001-06968				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	427789	See ECN	TUP	New data sheet
*A	437321	See ECN	TUP	Show data sheet on external Web
*B	472053	See ECN	TUP	Updated Part Numbering Nomenclature and Ordering Information
*C	503290	See ECN	PCI	Changed from “Advance” to “Preliminary” Changed the term “Unlimited” to “Infinite” Changed I_{CC3} value from 10mA to 15mA Removed Industrial Grade mention Removed 35 ns speed bin Removed I_{CC1} values from the DC table for 35 ns Industrial Grade Corrected V_{IL} min specification from (V_{CC} - 0.5) to (V_{SS} - 0.5) Removed all references pertaining to $\overline{OE}$ controlled Software STORE and RECALL operation Changed the address locations of the software STORE/RECALL command Updated Part Nomenclature Table and Ordering Information Table
*D	1349963	See ECN	UHA/SFV	Changed from “Preliminary” to “Final.” Updated AC Test Conditions Updated Ordering Information Table
*E	2427986	See ECN	GVCH	Move to external web