

1-Mb (64K x 16) Static RAM

Features

- **Temperature Ranges**
 - Industrial: -40°C to 85°C
 - Automotive: -40°C to 125°C
- **Very high speed: 45 ns**
- **Wide voltage range: 2.2V to 3.6V**
- **Pin compatible with CY62127BV**
- **Ultra-low active power**
 - Typical active current: 0.85 mA @ $f = 1 \text{ MHz}$
 - Typical active current: 5 mA @ $f = f_{\text{MAX}}$
- **Ultra-low standby power**
- **Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ features**
- **Automatic power-down when deselected**
- **Available in Pb-Free and non Pb-Free 48-ball FBGA and a 44-lead TSOP Type II packages**

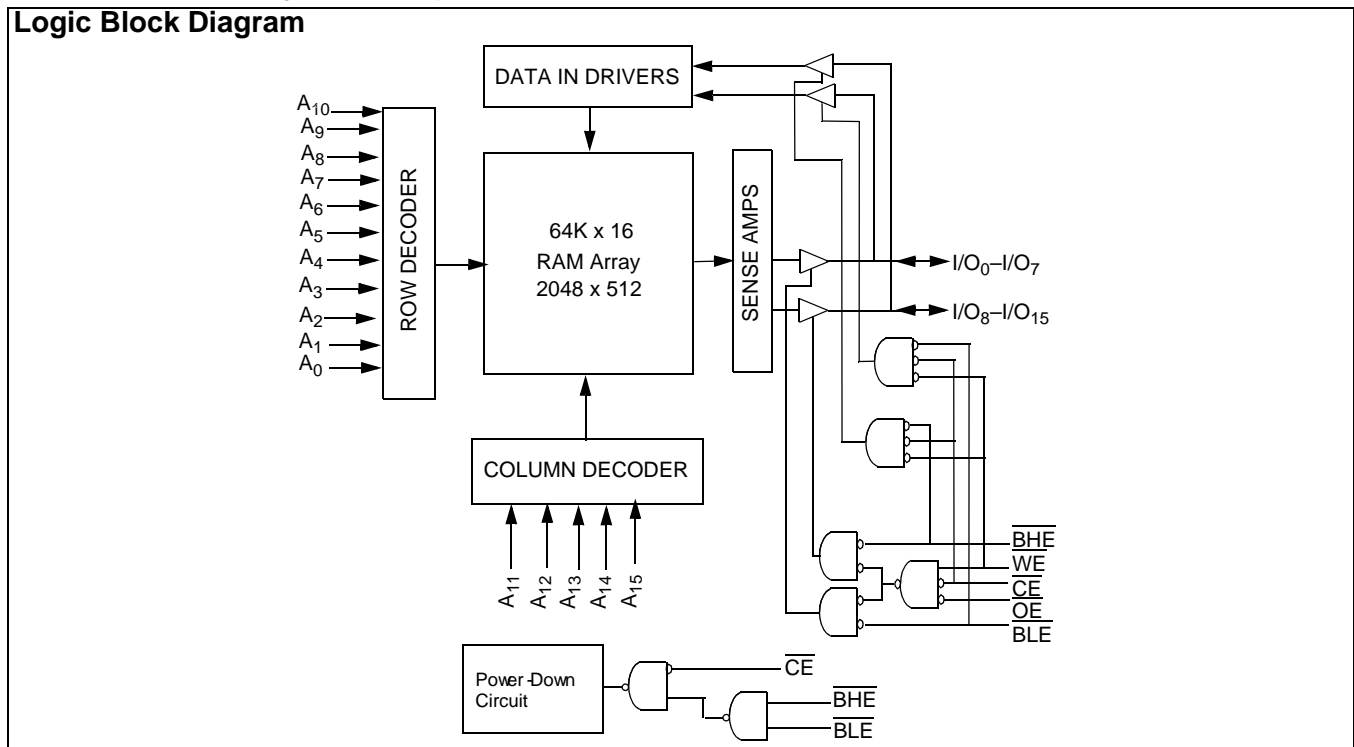
Functional Description^[1]

The CY62127DV30 is a high-performance CMOS static RAM organized as 64K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in

portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 90% when addresses are not toggling. The device can be put into standby mode reducing power consumption by more than 99% when deselected ($\overline{\text{CE}}$ HIGH or both $\overline{\text{BHE}}$ and $\overline{\text{BLE}}$ are HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected ($\overline{\text{CE}}$ HIGH), outputs are disabled ($\overline{\text{OE}}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{\text{BHE}}$, $\overline{\text{BLE}}$ HIGH) or during a write operation ($\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW).

Writing to the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Write Enable ($\overline{\text{WE}}$) inputs LOW. If Byte Low Enable ($\overline{\text{BLE}}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{15}). If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{15}).

Reading from the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Output Enable ($\overline{\text{OE}}$) LOW while forcing the Write Enable ($\overline{\text{WE}}$) HIGH. If Byte Low Enable ($\overline{\text{BLE}}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7 . If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15} . See the truth table at the back of this data sheet for a complete description of read and write modes



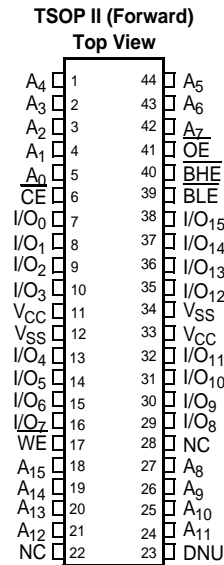
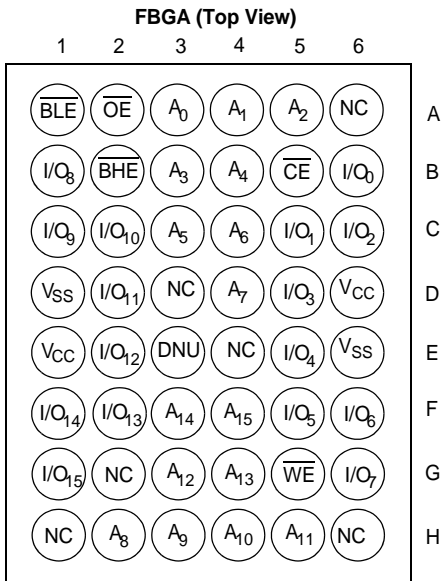
Note:

1. For best-practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

Product Portfolio

Product	V _{CC} Range (V)			Speed (ns)	Power Dissipation						
					Operating, I _{CC} (mA)					Standby I _{SB2} (μA)	
	Min.	Typ.	Max.		f = 1 MHz		f = f _{MAX}				
					Typ. ^[4]	Max.	Typ. ^[4]	Max.	Range	Typ. ^[4]	Max.
CY62127DV30L	2.2	3.0	3.6	45	0.85	1.5	6.5	13	Ind'l	1.5	5
CY62127DV30LL				45	0.85	1.5	6.5	13	Ind'l	1.5	4
CY62127DV30L	2.2	3.0	3.6	55	0.85	1.5	5	10	Ind'l	1.5	5
									Auto	1.5	15
CY62127DV30LL	2.2	3.0	3.6	55	0.85	1.5	5	10	Ind'l	1.5	4
CY62127DV30L	2.2	3.0	3.6	70	0.85	1.5	5	10	Ind'l	1.5	5
CY62127DV30LL				70	0.85	1.5	5	10	Ind'l	1.5	4

Pin Configurations^[2, 3]



Notes:

- NC pins are not connected to the die.
- Pin #23 of TSOP II and E3 ball of FBGA are DNU, which have to be left floating or tied to V_{SS} to ensure proper application. (Expansion Pins on FBGA Package: E4 - 2M, D3 - 4M, H1 - 8M, G2 - 16M, H6 - 32M).
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25°C.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with Power Applied..... -55°C to +125°C
 Supply Voltage to Ground Potential -0.3V to 3.9V
 DC Voltage Applied to Outputs in High-Z State^[5] -0.3V to $V_{CC} + 0.3V$

DC Input Voltage^[5] -0.3V to $V_{CC} + 0.3V$
 Output Current into Outputs (LOW)..... 20 mA
 Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)
 Latch-up Current..... > 200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{CC} ^[6]
Industrial	-40°C to +85°C	2.2V to 3.6V
Automotive	-40°C to +125°C	2.2V to 3.6V

DC Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions	-45			-55			-70			Unit	
			Min.	Typ. ^[4]	Max.	Min.	Typ. ^[4]	Max.	Min.	Typ. ^[4]	Max.		
V_{OH}	Output HIGH Voltage	$2.2 \leq V_{CC} \leq 2.7$	$I_{OH} = -0.1 \text{ mA}$		2.0			2.0			2.0	V	
		$2.7 \leq V_{CC} \leq 3.6$	$I_{OH} = -1.0 \text{ mA}$		2.4			2.4			2.4		
V_{OL}	Output LOW Voltage	$2.2 \leq V_{CC} \leq 2.7$	$I_{OL} = 0.1 \text{ mA}$					0.4			0.4	V	
		$2.7 \leq V_{CC} \leq 3.6$	$I_{OL} = 2.1 \text{ mA}$					0.4			0.4		
V_{IH}	Input HIGH Voltage	$2.2 \leq V_{CC} \leq 2.7$		1.8		$V_{CC} + 0.3$	1.8		$V_{CC} + 0.3$	1.8		$V_{CC} + 0.3$	V
		$2.7 \leq V_{CC} \leq 3.6$		2.2		$V_{CC} + 0.3$	2.2		$V_{CC} + 0.3$	2.2		$V_{CC} + 0.3$	
V_{IL}	Input LOW Voltage	$2.2 \leq V_{CC} \leq 2.7$		-0.3		0.6	-0.3		0.6	-0.3		0.6	V
		$2.7 \leq V_{CC} \leq 3.6$		-0.3		0.8	-0.3		0.8	-0.3		0.8	
I_{IX}	Input Leakage Current	$GND \leq V_I \leq V_{CC}$		Ind'l	-1	+1	-1	+1	-1	+1	-1	+1	μA
				Auto			-4	+4					μA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$, Output Disabled		Ind'l	-1	+1	-1	+1	-1	+1	-1	+1	μA
				Auto			-4	+4					μA
I_{CC}	V_{CC} Operating Supply Current	$f = f_{MAX} = 1/t_{RC}$	$V_{CC} = 3.6V$, $I_{OUT} = 0 \text{ mA}$, CMOS level		6.5	13		5	10		5	10	mA
		$f = 1 \text{ MHz}$			0.85	1.5		0.85	1.5		0.85	1.5	
I_{SB1}	Automatic CE Power-down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$, $V_{IN} \leq 0.2V$, $f = f_{MAX}$ (Address and Data Only), $f = 0$ (OE, WE, BHE and BLE)	L	Ind'l	1.5	5		1.5	5		1.5	5	μA
				Auto				1.5	15				
			LL		1.5	4		1.5	4		1.5	4	
I_{SB2}	Automatic CE Power-down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0$, $V_{CC} = 3.6V$	L	Ind'l	1.5	5		1.5	5		1.5	5	μA
				Auto				1.5	15				
			LL		1.5	4		1.5	4		1.5	4	

Capacitance^[7]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$ $V_{CC} = V_{CC(typ)}$	8	pF
C_{OUT}	Output Capacitance		8	pF

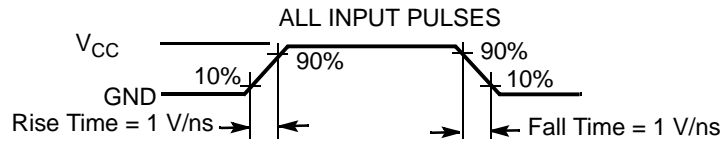
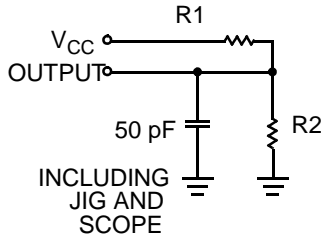
Notes:

- $V_{IL(min)}$ = -2.0V for pulse durations less than 20 ns., $V_{IH(max)}$ = $V_{CC} + 0.75V$ for pulse durations less than 20 ns.
- Full device operation requires linear ramp of V_{CC} from 0V to $V_{CC(min)}$ & V_{CC} must be stable at $V_{CC(min)}$ for 500 μs .
- Tested initially and after any design or process changes that may affect these parameters.

Thermal Resistance^[7]

Parameter	Description	Test Conditions	FBGA	TSOP II	Unit
θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	55	76	°C/W
θ_{JC}	Thermal Resistance (Junction to Case)		12	11	°C/W

AC Test Loads and Waveforms^[8]



Equivalent to: THEVENIN EQUIVALENT

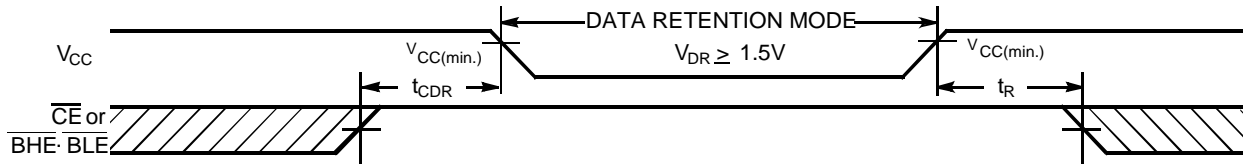


Parameters	2.5V (2.2V - 2.7V)	3.0V (2.7V - 3.6V)	Unit
R1	16600	1103	Ω
R2	15400	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Data Retention Characteristics

Parameter	Description	Conditions	Min.	Typ. ^[4]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1.5			V
I_{CCDR}	Data Retention Current	$V_{CC}=1.5V, \overline{CE} \geq V_{CC} - 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	L	Ind'l	4	μA
			L	Auto	10	
			LL	Ind'l	3	
$t_{CDR}^{[7]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[9]}$	Operation Recovery Time		200			μs

Data Retention Waveform^[10]



Notes:

- 8. Test condition for the 45-ns part is a load capacitance of 30 pF.
- 9. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} > 200 \mu s$.
- 10. BHE-BLE is the AND of both BHE and BLE. Chip can be deselected by either disabling the Chip Enable signals or by disabling both.

Switching Characteristics (Over the Operating Range)^[11]

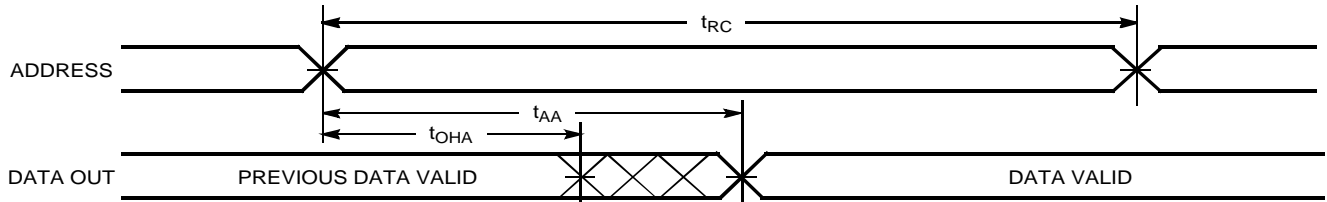
Parameter	Description	CY62127DV30-45 ^[8]		CY62127DV30-55		CY62127DV30-70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t _{RC}	Read Cycle Time	45		55		70		ns
t _{AA}	Address to Data Valid		45		55		70	ns
t _{OHA}	Data Hold from Address Change	10		10		10		ns
t _{ACE}	\overline{CE} LOW to Data Valid		45		55		70	ns
t _{DOE}	\overline{OE} LOW to Data Valid		25		25		35	ns
t _{LZOE}	\overline{OE} LOW to Low Z ^[12]	5		5		5		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[12,14]		15		20		25	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[12]	10		10		10		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[12,14]		20		20		25	ns
t _{PU}	\overline{CE} LOW to Power-up	0		0		0		ns
t _{PD}	\overline{CE} HIGH to Power-down		45		55		70	ns
t _{DBE}	$\overline{BLE}/\overline{BHE}$ LOW to Data Valid		45		55		70	ns
t _{LZBE} ^[13]	$\overline{BLE}/\overline{BHE}$ LOW to Low Z ^[12]	5		5		5		ns
t _{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to High-Z ^[12,14]		15		20		25	ns
Write Cycle^[15]								
t _{WC}	Write Cycle Time	45		55		70		ns
t _{SCE}	\overline{CE} LOW to Write End	40		40		60		ns
t _{AW}	Address Set-up to Write End	40		40		60		ns
t _{HA}	Address Hold from Write End	0		0		0		ns
t _{SA}	Address Set-up to Write Start	0		0		0		ns
t _{PWE}	\overline{WE} Pulse Width	35		40		50		ns
t _{BW}	$\overline{BLE}/\overline{BHE}$ LOW to Write End	40		40		60		ns
t _{SD}	Data Set-up to Write End	25		25		30		ns
t _{HD}	Data Hold from Write End	0		0		0		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[12,14]		15		20		25	ns
t _{LZWE}	\overline{WE} HIGH to Low Z ^[12]	10		10		5		ns

Notes:

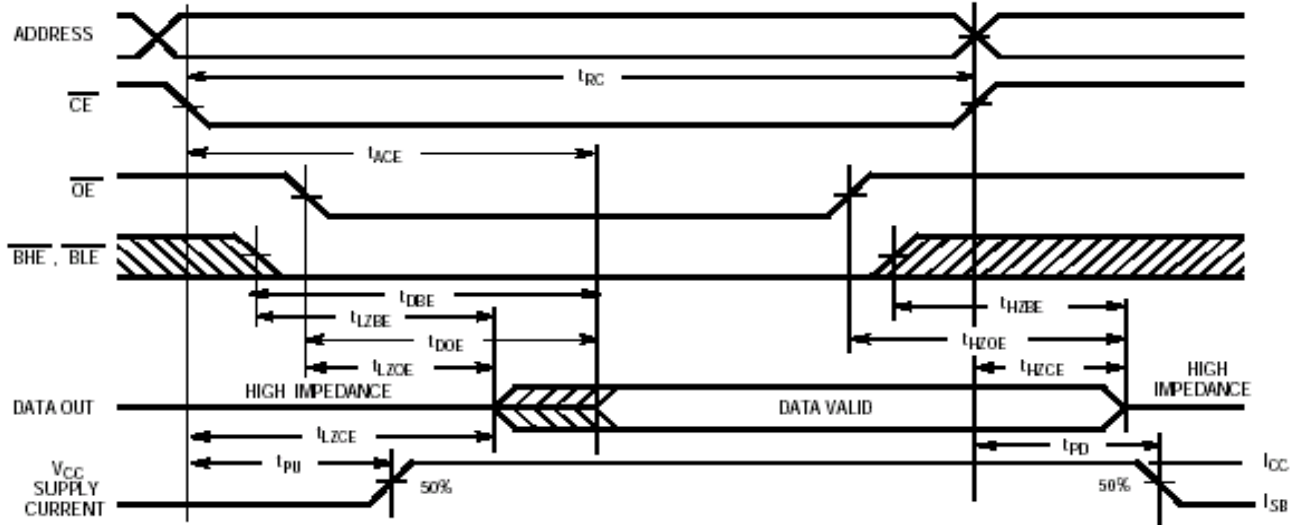
11. Test conditions assume signal transition time of 1V/ns or less, timing reference levels of $V_{CC(typ.)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL} .
12. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
13. If both byte enables are toggled together, this value is 10 ns.
14. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
15. The internal Write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

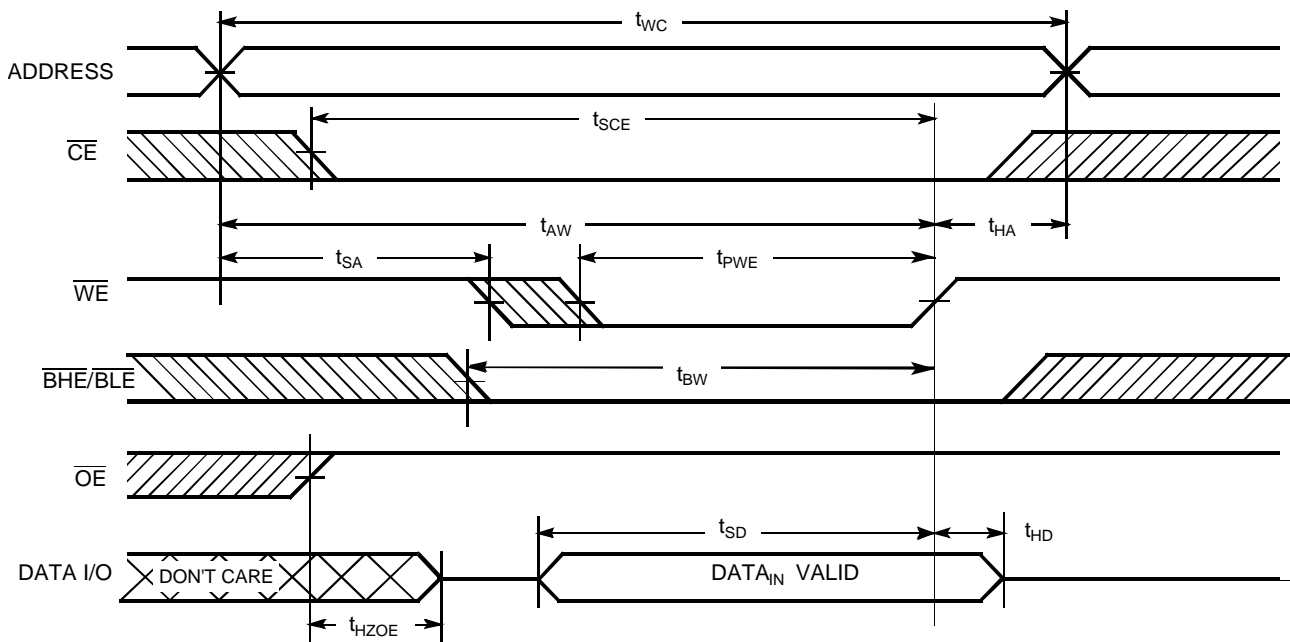
Read Cycle No. 1 (Address Transition Controlled)^[16,17]



Read Cycle No. 2 (OE Controlled)^[16,17,18]



Write Cycle No. 1 (\overline{WE} Controlled)^[14, 15, 19, 20, 21]

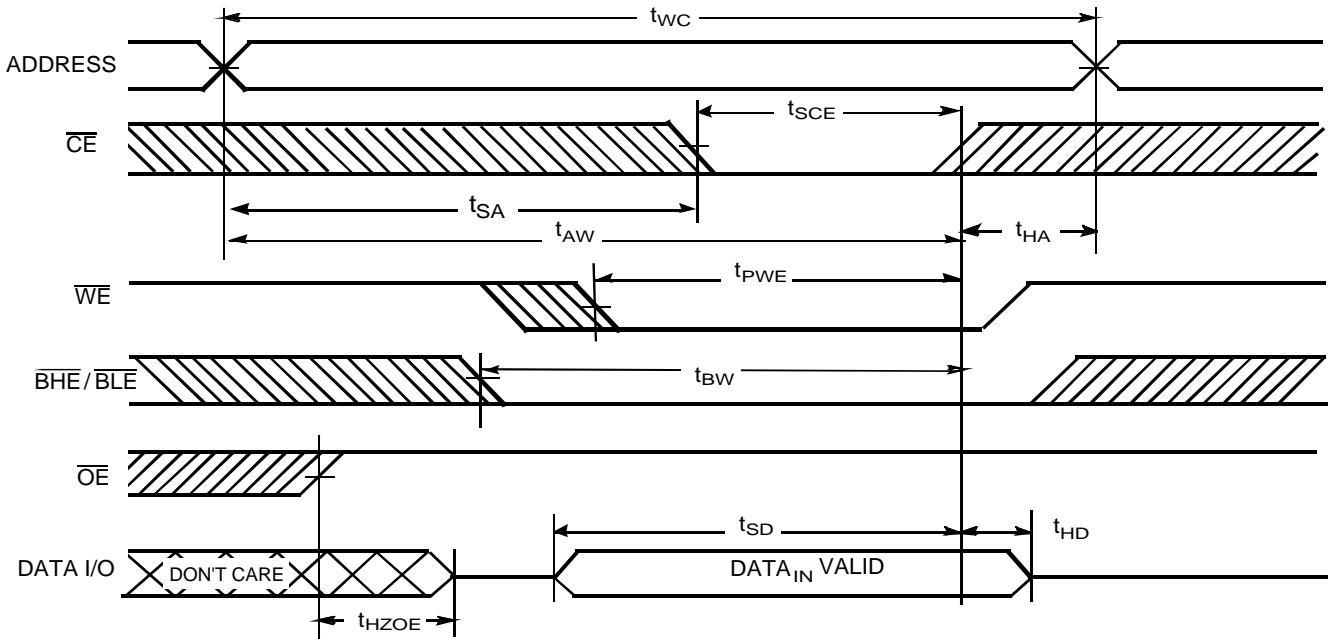


Notes:

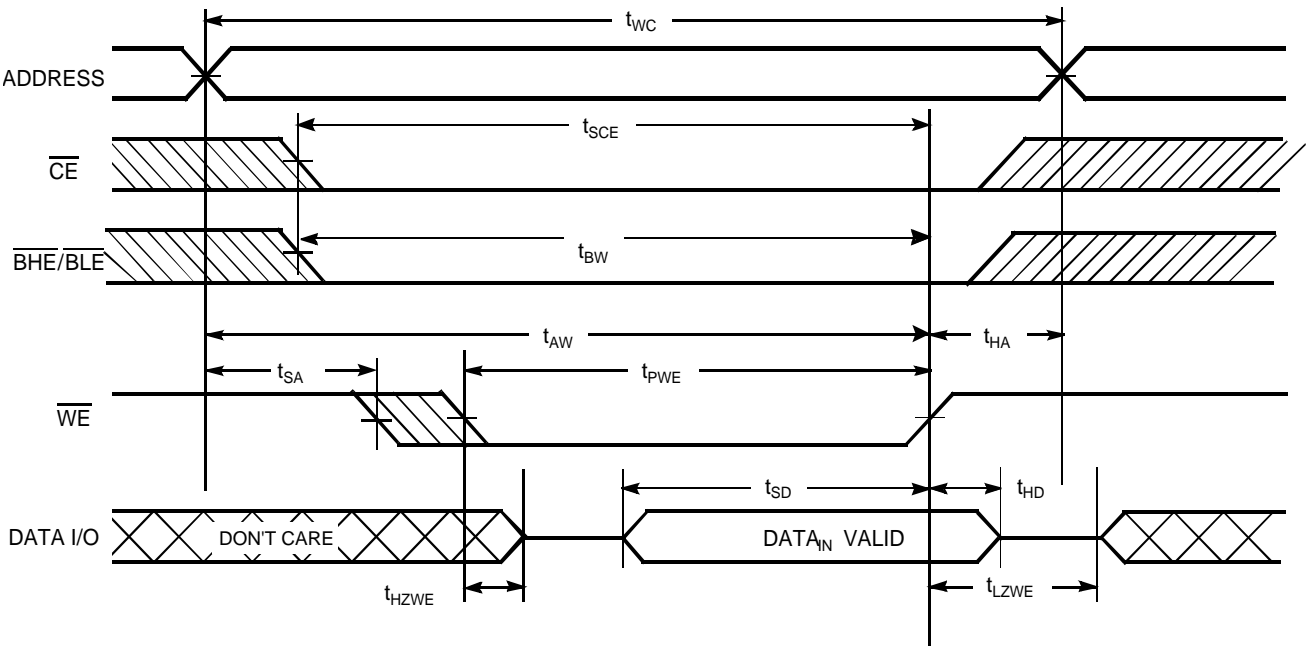
- 16. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$, \overline{BHE} , $\overline{BLE} = V_{IL}$.
- 17. \overline{WE} is HIGH for Read cycle.
- 18. Address valid prior to or coincident with \overline{CE} , \overline{BHE} , \overline{BLE} transition LOW.
- 19. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.
- 20. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.
- 21. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 2 (\overline{CE} Controlled)^[14, 15, 19, 20, 21]

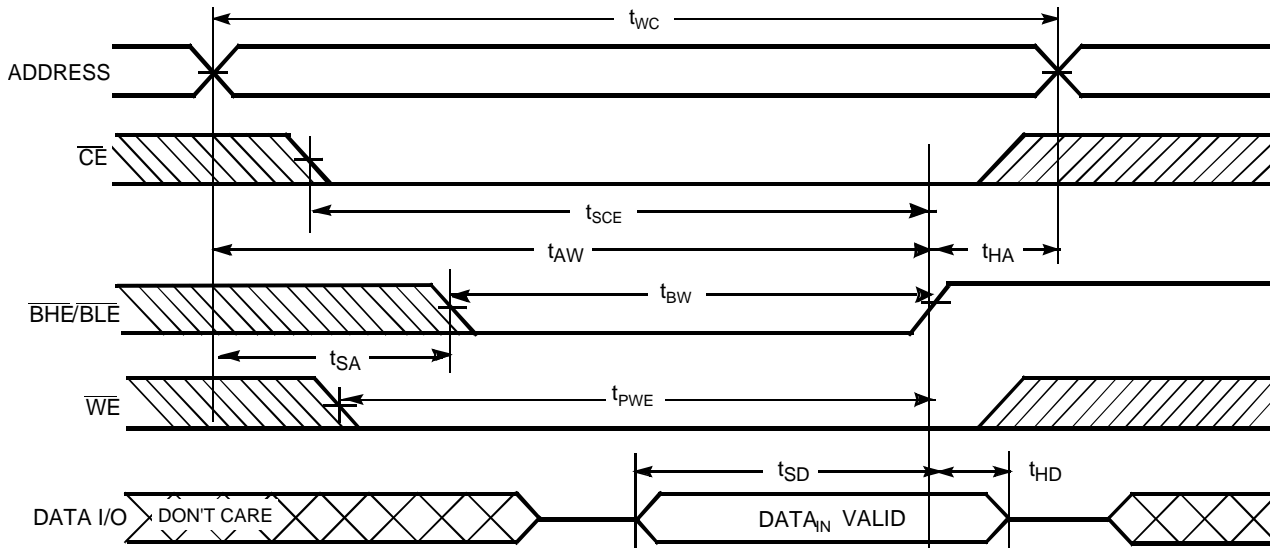


Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[20, 21]



Switching Waveforms (continued)

Write Cycle No. 4 ($\overline{\text{BHE}}/\overline{\text{BLE}}$ -controlled, $\overline{\text{OE}}$ LOW)^[20, 21]



Truth Table

CE	WE	OE	BHE	BLE	I/O ₀ -I/O ₇	I/O ₈ -I/O ₁₅	Mode	Power
H	X	X	X	X	High Z	High Z	Deselect/Power-down	Standby (I _{SB})
X	X	X	H	H	High Z	High Z	Deselect/Power-down	Standby (I _{SB})
L	H	L	L	L	Data Out	Data Out	Read All bits	Active (I _{CC})
L	H	L	H	L	Data Out	High Z	Read Lower Byte Only	Active (I _{CC})
L	H	L	L	H	High Z	Data Out	Read Upper Byte Only	Active (I _{CC})
L	H	H	L	L	High Z	High Z	Output Disabled	Active (I _{CC})
L	H	H	H	L	High Z	High Z	Output Disabled	Active (I _{CC})
L	H	H	L	H	High Z	High Z	Output Disabled	Active (I _{CC})
L	L	X	L	L	Data In	Data In	Write	Active (I _{CC})
L	L	X	H	L	Data In	High Z	Write Lower Byte Only	Active (I _{CC})
L	L	X	L	H	High Z	Data In	Write Upper Byte Only	Active (I _{CC})

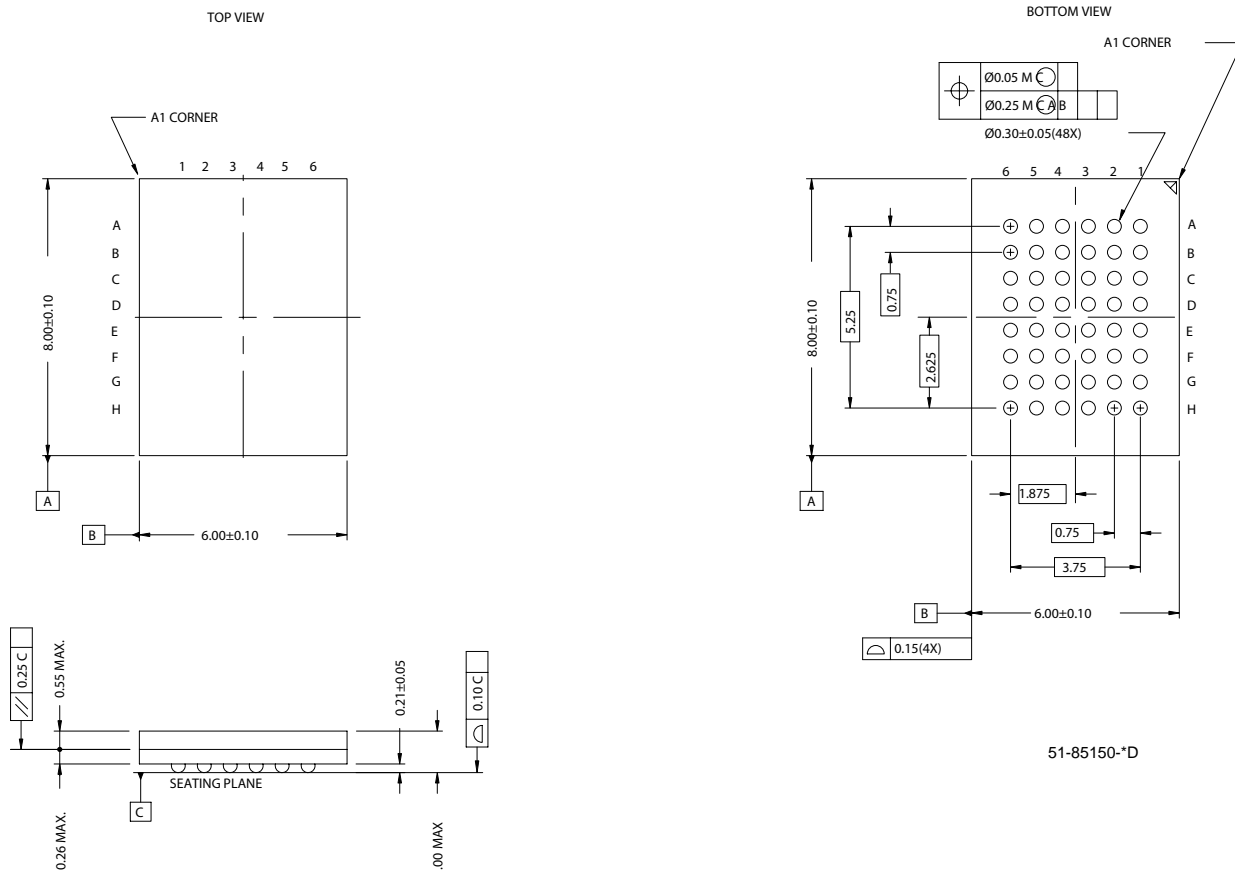
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62127DV30LL-45BVXI	51-85150	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm) (Pb-Free)	Industrial
	CY62127DV30LL-45ZXI	51-85087	44-lead TSOP Type II (Pb-Free)	
55	CY62127DV30LL-55BVI	51-85150	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	Industrial
	CY62127DV30LL-55BVXI	51-85150	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm) (Pb-Free)	
	CY62127DV30LL-55ZI	51-85087	44-lead TSOP Type II	
	CY62127DV30L-55ZXI	51-85087	44-lead TSOP Type II (Pb-Free)	
	CY62127DV30LL-55ZXI	51-85087	44-lead TSOP Type II (Pb-Free)	
	CY62127DV30L-55BVXE	51-85150	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm) (Pb-Free)	Automotive
	CY62127DV30L-55ZSXE	51-85087	44-lead TSOP Type II (Pb-Free)	
70	CY62127DV30L-70BVI	51-85150	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	Industrial
	CY62127DV30LL-70BVXI	51-85150	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm) (Pb-Free)	
	CY62127DV30L-70ZI	51-85087	44-lead TSOP Type II	
	CY62127DV30LL-70ZXI	51-85087	44-lead TSOP Type II (Pb-Free)	

Please contact your local Cypress sales representative for availability of these parts

Package Diagrams

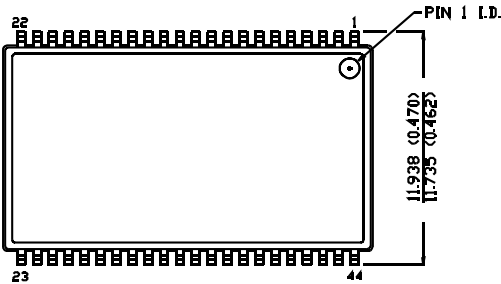
48-ball VFBGA (6 x 8 x 1 mm) (51-85150)



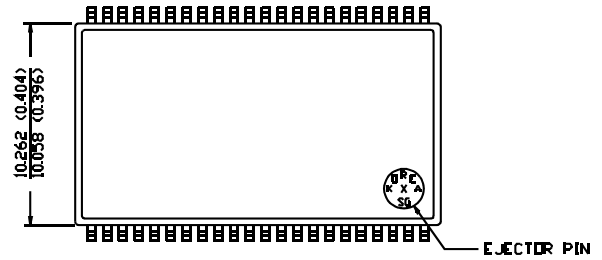
Package Diagrams (continued)

44-lead TSOP II (51-85087)

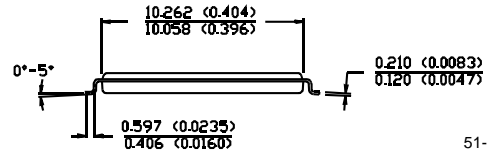
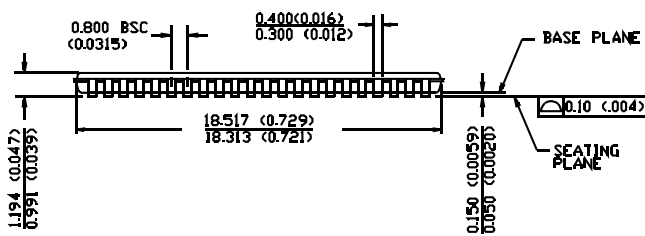
DIMENSION IN MM (INCH)
MAX
MIN



TOP VIEW



BOTTOM VIEW



51-85087-A

MoBL is a registered trademark, and MoBL2 and More Battery Life are trademarks of Cypress Semiconductor. All product and company names mentioned in this document are the trademarks of their respective holders.

Document History Page

Document Title: CY62127DV30 MoBL [®] 1-Mb (64K x 16) Static RAM				
Document Number: 38-05229				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	117690	08/27/02	JUI	New Data Sheet
*A	127311	06/13/03	MPR	Changed From Advanced Status to Preliminary Changed Isb2 to 5 μ A (L), 4 μ A (LL) Changed Iccdr to 4 μ A (L), 3 μ A (LL) Changed Cin from 6 pF to 8 pF
*B	128341	07/22/03	JUI	Changed from Preliminary to Final Add 70-ns speed, updated ordering information
*C	129000	08/29/03	CDY	Changed Icc 1 MHz typ from 0.5 mA to 0.85 mA
*D	316039	See ECN	PCI	Added 45-ns Speed Bin in AC, DC and Ordering Information tables Added Footnote # 8 on page #4 Added Lead-Free Package ordering information on page# 9 Changed 44-lead TSOP-II package name from Z44 to ZS44
*E	346982	See ECN	AJU	Added 56-pin QFN package
*F	369955	See ECN	SYT	Added Temperature Ranges in the Features Section on Page # 1 Added Automotive Specs for I _{IX} , I _{OZ} , I _{SB1} and I _{SB2} in the Product portfolio on Page #2 and the DC Electrical Characteristics table on Page# 4 Added Automotive spec for I _{CCDR} in the Data Retention Characteristics table on Page# 5 Added Pb-Free Automotive parts for 55 ns Speed bin
*G	457685	See ECN	NXR	Removed 56-pin QFN package from product offering Updated ordering Information Table
*H	470383	See ECN	NXR	Changed pin #23 of TSOP II from NC to DNU and updated footnote #2