

256K (32K x 8) Static RAM

Features

- **High Speed**
 - 70 ns
- **Temperature Ranges**
 - Commercial: 0°C to 70°C
 - Industrial: -40°C to 85°C
 - Automotive: -40°C to 125°C
- **Low voltage range:**
 - 2.7V – 3.6V
- **Low active power and standby power**
- **Easy memory expansion with \overline{CE} and \overline{OE} features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Available in a Pb-free and non Pb-free standard 28-pin narrow SOIC, 28-pin TSOP-1 and 28-pin Reverse TSOP-1 packages**

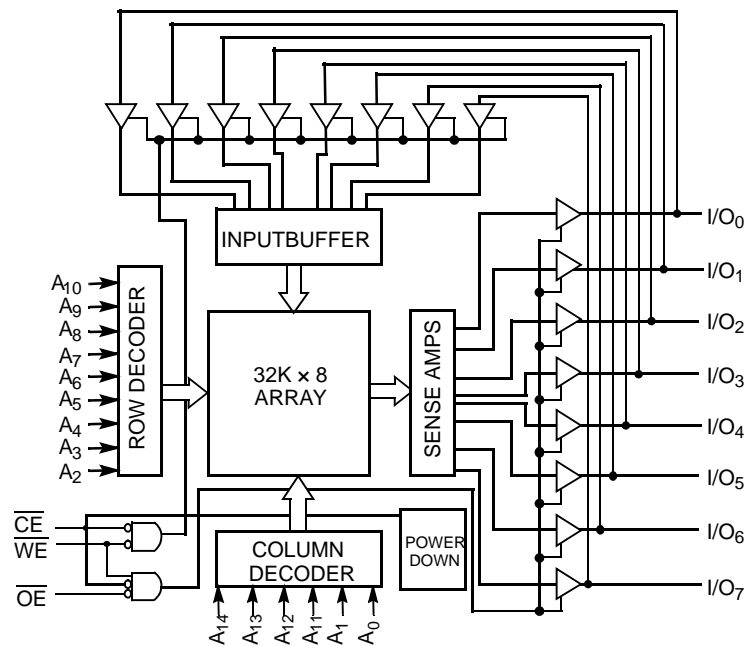
Functional Description^[1]

The CY62256V family is composed of two high-performance CMOS static RAM's organized as 32K words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (\overline{CE}) and active LOW output enable (\overline{OE}) and Tri-state drivers. These devices have an automatic power-down feature, reducing the power consumption by over 99% when deselected.

An active LOW write enable signal (\overline{WE}) controls the writing/reading operation of the memory. When \overline{CE} and \overline{WE} inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, \overline{CE} and \overline{OE} active LOW, while \overline{WE} remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable (\overline{WE}) is HIGH.

Logic Block Diagram

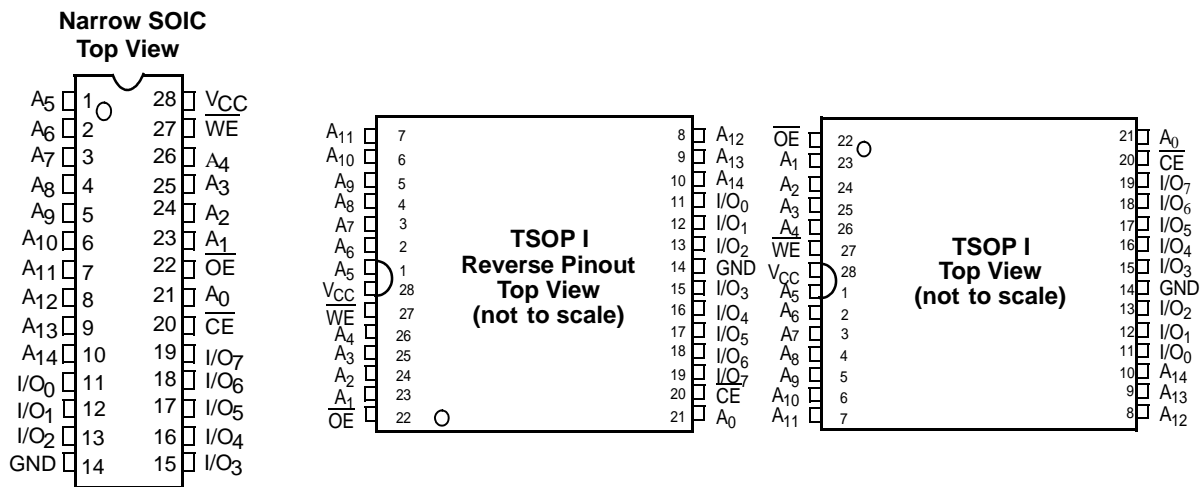


Note:

1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

Product Portfolio

| Product | Range | V _{CC} Range (V) | | | Speed (ns) | Power Dissipation | | | |
|------------|-------------|---------------------------|---------------------|------|---------------|---------------------------------|------|--------------------------------|------|
| | | Min. | Typ. ^[2] | Max. | | Operating, I _{CC} (mA) | | Standby, I _{SB2} (μA) | |
| | | | | | | Typ. ^[2] | Max. | Typ. ^[2] | Max. |
| CY62256VLL | Com'l/Ind'l | 2.7 | 3.0 | 3.6 | 70 | 11 | 30 | 0.1 | 5 |
| | Automotive | | | | | | | | 130 |

Pin Configurations

Pin Definitions

| Pin Number | Type | Description |
|-----------------|---------------|--|
| 1–10, 21, 23–26 | Input | A₀–A₁₄ . Address Inputs |
| 11–13, 15–19 | Input/Output | I/O₀–I/O₇ . Data lines. Used as input or output lines depending on operation |
| 27 | Input/Control | \overline{WE} . When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted |
| 20 | Input/Control | \overline{CE} . When LOW, selects the chip. When HIGH, deselects the chip |
| 22 | Input/Control | \overline{OE} . Output Enable. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are Tri-stated, and act as input data pins |
| 14 | Ground | GND . Ground for the device |
| 28 | Power Supply | V_{CC} . Power supply for the device |

Note:

2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25°C, and t_{AA} = 70 ns.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with Power Applied..... -55°C to +125°C
 Supply Voltage to Ground Potential (Pin 28 to Pin 14) -0.5V to +4.6V
 DC Voltage Applied to Outputs in High-Z State^[3] -0.5V to $V_{CC} + 0.5V$
 DC Input Voltage^[3] -0.5V to $V_{CC} + 0.5V$

Output Current into Outputs (LOW)..... 20 mA
 Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)
 Latch-up Current..... > 200 mA

Operating Range

| Device | Range | Ambient Temperature (T_A) ^[4] | V_{CC} |
|----------|------------|--|--------------|
| CY62256V | Commercial | 0°C to +70°C | 2.7V to 3.6V |
| | Industrial | -40°C to +85°C | |
| | Automotive | -40°C to +125°C | |

Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | CY62256V-70 | | | Unit | |
|-----------|--|--|--------------|---------------------|-----------------|---------|-----|
| | | | Min. | Typ. ^[2] | Max. | | |
| V_{OH} | Output HIGH Voltage | $I_{OH} = -1.0 \text{ mA}$, $V_{CC} = 2.7V$ | 2.4 | | | V | |
| V_{OL} | Output LOW Voltage | $I_{OL} = 2.1 \text{ mA}$, $V_{CC} = 2.7V$ | | | 0.4 | V | |
| V_{IH} | Input HIGH Voltage | | 2.2 | | $V_{CC} + 0.3V$ | V | |
| V_{IL} | Input LOW Voltage | | -0.5 | | 0.8 | V | |
| I_{IX} | Input Leakage Current | $GND \leq V_{IN} \leq V_{CC}$ | Com'l, Ind'l | -1 | +1 | μA | |
| | | | Automotive | -10 | +10 | μA | |
| I_{OZ} | Output Leakage Current | $GND \leq V_{IN} \leq V_{CC}$, Output Disabled | Com'l, Ind'l | -1 | +1 | μA | |
| | | | Automotive | -10 | +10 | μA | |
| I_{CC} | V_{CC} Operating Supply Current | $V_{CC} = 3.6V$, $I_{OUT} = 0 \text{ mA}$, $f = f_{Max} = 1/t_{RC}$ | All ranges | 11 | 30 | mA | |
| I_{SB1} | Automatic CE Power-down Current— TTL Inputs | $V_{CC} = 3.6V$, $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{Max}$ | All ranges | 100 | 300 | μA | |
| I_{SB2} | Automatic CE Power-down Current— CMOS Inputs | $V_{CC} = 3.6V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$, $f = 0$ | Com'l | 0.1 | 5 | μA | |
| | | | Ind'l | | 0.1 | | 10 |
| | | | Automotive | | 0.1 | | 130 |

Notes:

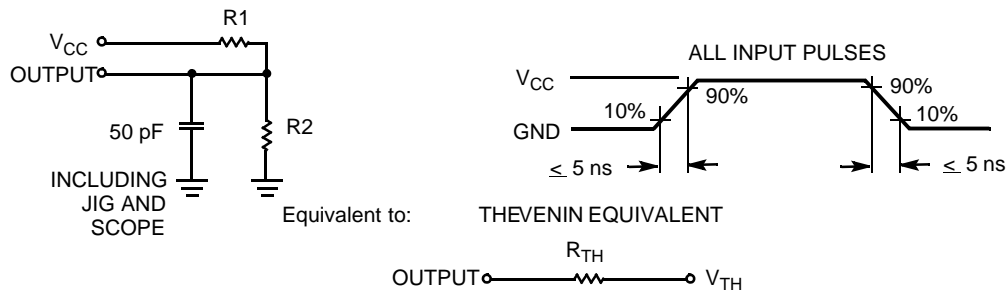
- V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
- T_A is the "Instant-On" case temperature.

Capacitance^[5]

| Parameter | Description | Test Conditions | Max. | Unit |
|------------------|--------------------|---|------|------|
| C _{IN} | Input Capacitance | T _A = 25°C, f = 1 MHz, V _{CC} = V _{CC(typ.)} | 6 | pF |
| C _{OUT} | Output Capacitance | | 8 | pF |

Thermal Resistance

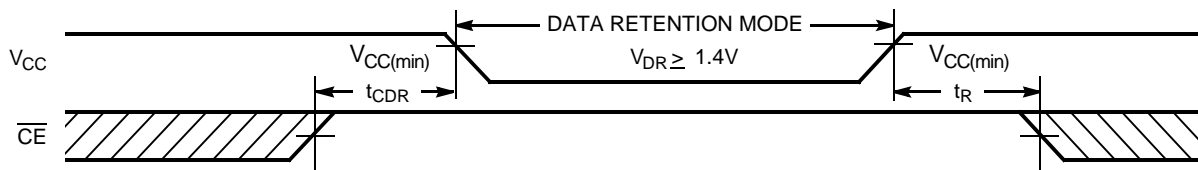
| Parameter | Description | Test Conditions | SOIC | TSOPI | RTSOPI | Unit |
|-----------------|---|--|-------|-------|--------|------|
| θ _{JA} | Thermal Resistance (Junction to Ambient) ^[6] | Still Air, soldered on a 3 × 4.5 inch, 2-layer printed circuit board | 68.45 | 87.62 | 87.62 | °C/W |
| θ _{JC} | Thermal Resistance (Junction to Case) ^[5] | | 26.94 | 23.73 | 23.73 | °C/W |

AC Test Loads and Waveforms


| Parameter | 3.3V | Units |
|-----------------|-------|-------|
| R1 | 1100 | Ohms |
| R2 | 1500 | Ohms |
| R _{TH} | 645 | Ohms |
| V _{TH} | 1.750 | Volts |

Data Retention Characteristics (Over the Operating Range)

| Parameter | Description | Conditions ^[6] | Min. | Typ. ^[2] | Max. | Unit |
|---------------------------------|--------------------------------------|--|-----------------|---------------------|------|------|
| V _{DR} | V _{CC} for Data Retention | | 1.4 | | | V |
| I _{CCDR} | Data Retention Current | V _{CC} = 1.4V, $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V | Com'l | 0.1 | 3 | μA |
| | | | Ind'l | 0.1 | 6 | |
| | | | Auto | 0.1 | 50 | |
| t _{CDR} ^[6] | Chip Deselect to Data Retention Time | | 0 | | | ns |
| t _R ^[6] | Operation Recovery Time | | t _{RC} | | | ns |

Data Retention Waveform

Notes:

5. Tested initially and after any design or process changes that may affect these parameters.
6. No input may exceed V_{CC} + 0.3V.

Switching Characteristics Over the Operating Range^[7]

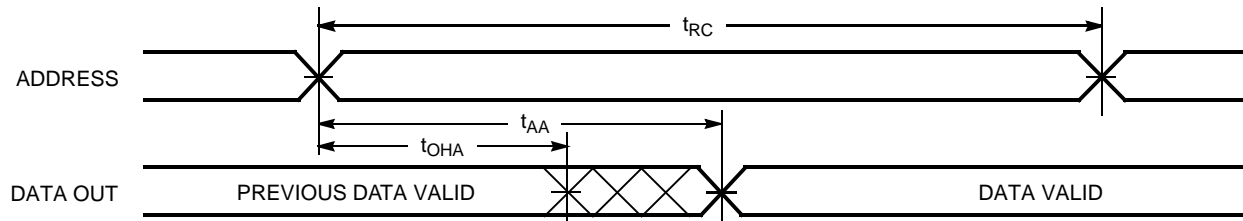
| Parameter | Description | CY62256V-70 | | Unit |
|---------------------------------------|--|-------------|------|------|
| | | Min. | Max. | |
| Read Cycle | | | | |
| t_{RC} | Read Cycle Time | 70 | | ns |
| t_{AA} | Address to Data Valid | | 70 | ns |
| t_{OHA} | Data Hold from Address Change | 10 | | ns |
| t_{ACE} | \overline{CE} LOW to Data Valid | | 70 | ns |
| t_{DOE} | \overline{OE} LOW to Data Valid | | 35 | ns |
| t_{LZOE} | \overline{OE} LOW to Low-Z ^[8] | 5 | | ns |
| t_{HZOE} | \overline{OE} HIGH to High-Z ^[8, 9] | | 25 | ns |
| t_{LZCE} | \overline{CE} LOW to Low-Z ^[8] | 10 | | ns |
| t_{HZCE} | \overline{CE} HIGH to High-Z ^[8, 9] | | 25 | ns |
| t_{PU} | \overline{CE} LOW to Power-up | 0 | | ns |
| t_{PD} | \overline{CE} HIGH to Power-down | | 70 | ns |
| Write Cycle^[10, 11] | | | | |
| t_{WC} | Write Cycle Time | 70 | | ns |
| t_{SCE} | \overline{CE} LOW to Write End | 60 | | ns |
| t_{AW} | Address Set-up to Write End | 60 | | ns |
| t_{HA} | Address Hold from Write End | 0 | | ns |
| t_{SA} | Address Set-up to Write Start | 0 | | ns |
| t_{PWE} | \overline{WE} Pulse Width | 50 | | ns |
| t_{SD} | Data Set-up to Write End | 30 | | ns |
| t_{HD} | Data Hold from Write End | 0 | | ns |
| t_{HZWE} | \overline{WE} LOW to High-Z ^[8, 9] | | 25 | ns |
| t_{LZWE} | \overline{WE} HIGH to Low-Z ^[8] | 10 | | ns |

Notes:

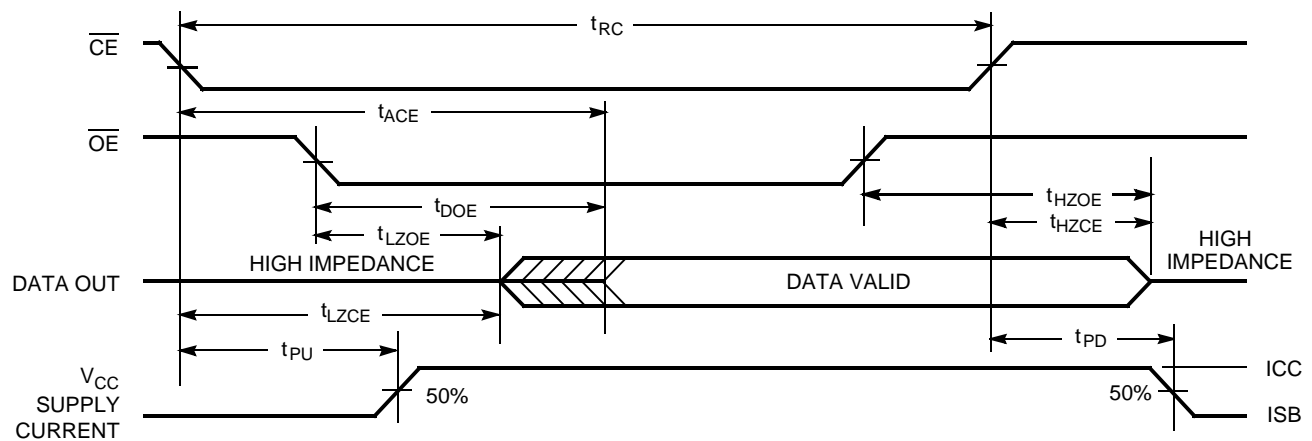
7. Test conditions assume signal transition time of 5 ns or less timing reference levels of $V_{CC}/2$, input pulse levels of 0 to V_{CC} , and output loading of the specified I_{OL}/I_{OH} and 50 pF load capacitance.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
9. t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with $C_L = 5$ pF as in (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
10. The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. The minimum write cycle time for write cycle #3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

Switching Waveforms

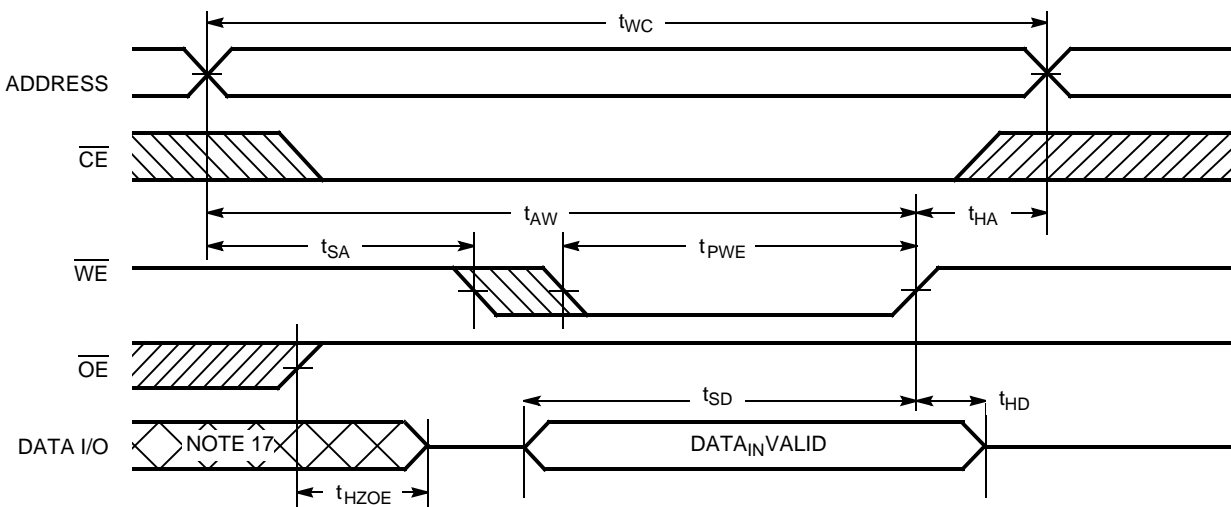
Read Cycle No. 1 (Address Transition Controlled)^[12, 13]



Read Cycle No. 2 (\overline{OE} Controlled)^[13, 14]



Write Cycle No. 1 (\overline{WE} Controlled)^[10, 15, 16]

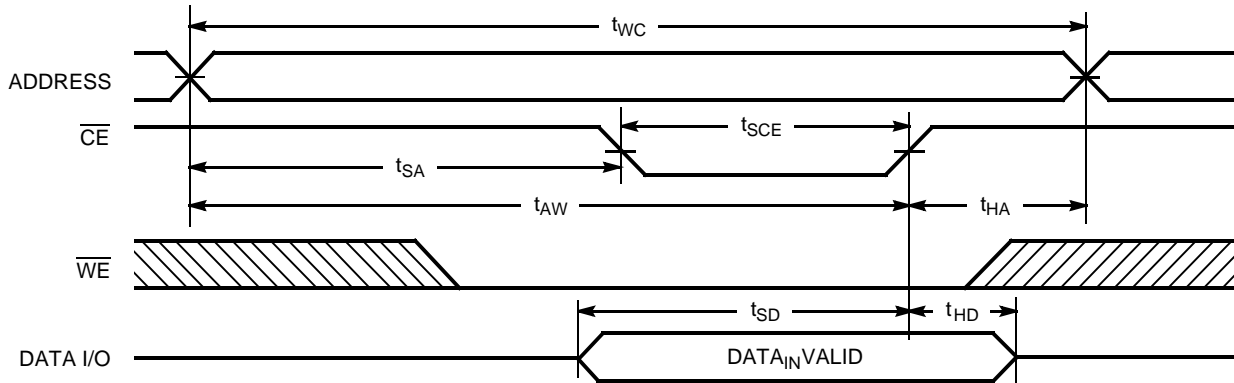


Notes:

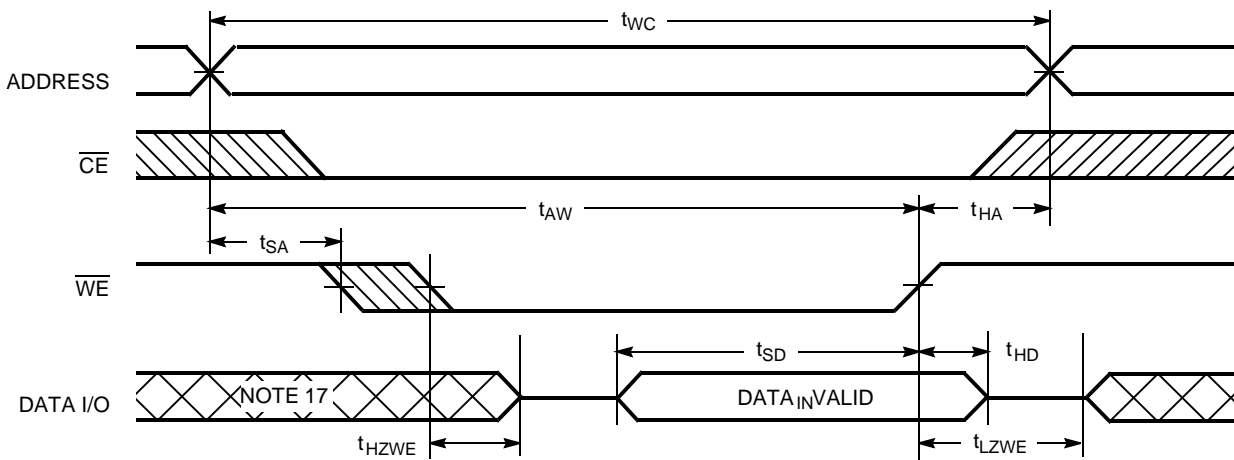
- 12. Device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}$.
- 13. \overline{WE} is HIGH for read cycle.
- 14. Address valid prior to or coincident with \overline{CE} transition LOW.
- 15. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 16. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.
- 17. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

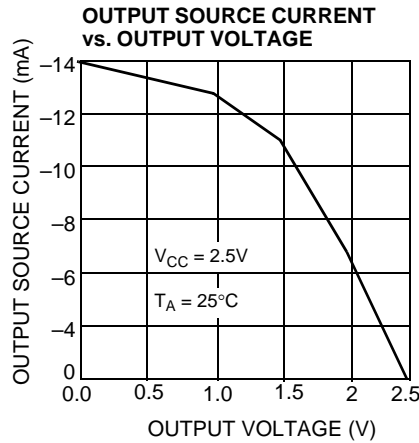
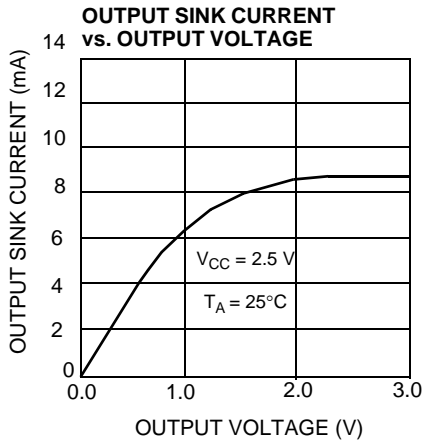
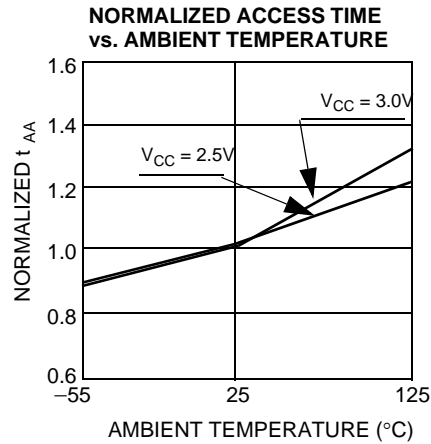
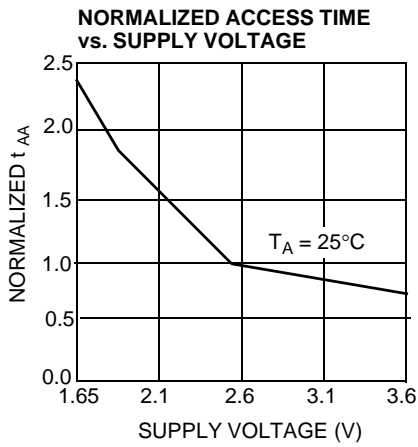
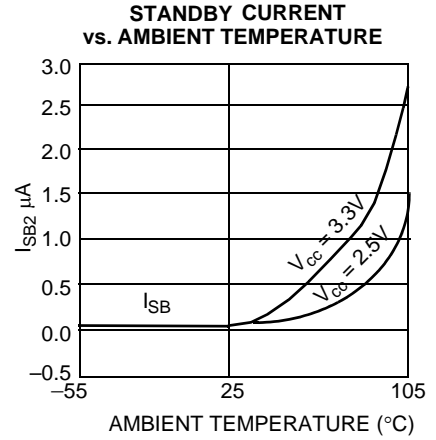
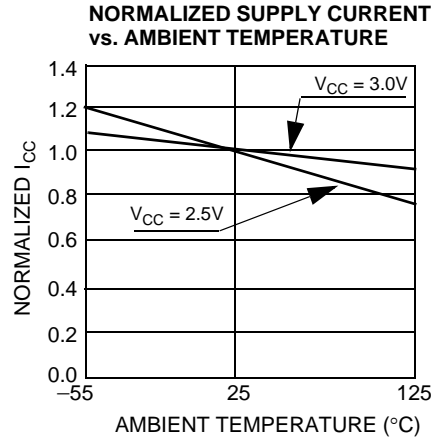
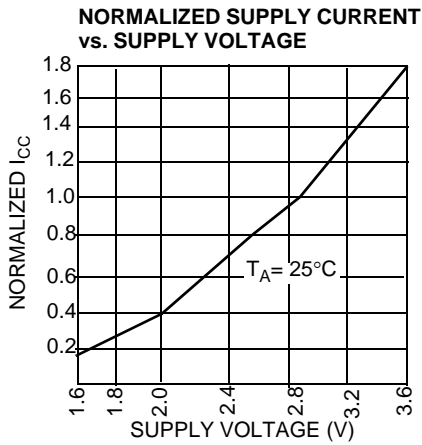
Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled)^[10, 15, 16]

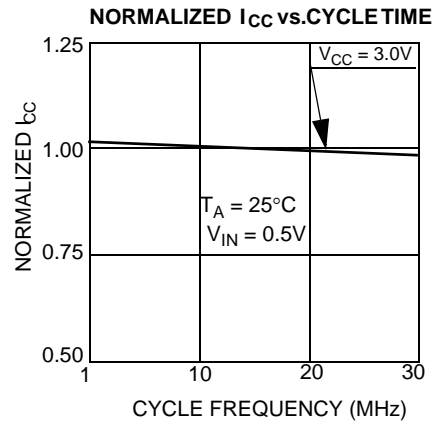
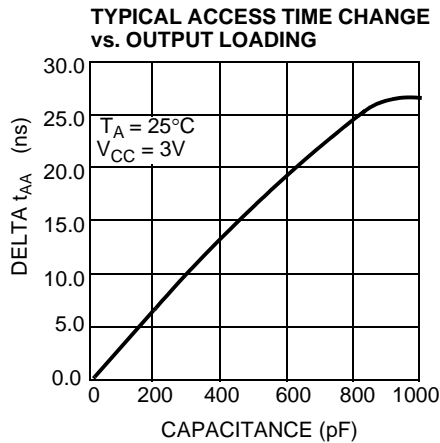


Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[11, 16]



Typical DC and AC Characteristics



Typical DC and AC Characteristics (continued)

Truth Table

| $\overline{\text{CE}}$ | $\overline{\text{WE}}$ | $\overline{\text{OE}}$ | Inputs/Outputs | Mode | Power |
|------------------------|------------------------|------------------------|----------------|---------------------------|-----------------------------|
| H | X | X | High-Z | Deselect/Power-down | Standby (I_{SB}) |
| L | H | L | Data Out | Read | Active (I_{CC}) |
| L | L | X | Data In | Write | Active (I_{CC}) |
| L | H | H | High-Z | Deselect, Output Disabled | Active (I_{CC}) |

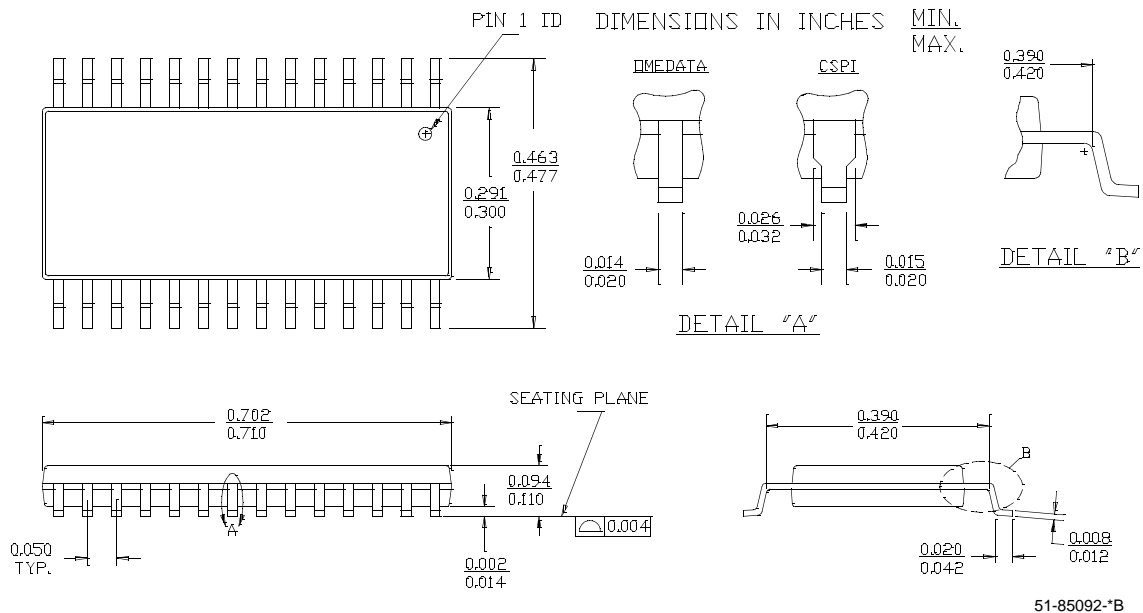
Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range | |
|------------|-------------------|-----------------|--|-----------------|------------|
| 70 | CY62256VLL-70SNC | 51-85092 | 28-pin (300-mil Narrow Body) SNC | Commercial | |
| | CY62256VLL-70SNXC | | 28-pin (300-mil Narrow Body) SNC (Pb-Free) | | |
| | CY62256VLL-70ZC | 51-85071 | 28-pin TSOP I | Industrial | |
| | CY62256VLL-70ZXC | | 28-pin TSOP I (Pb-Free) | | |
| | CY62256VLL-70SNXI | 51-85092 | 28-pin (300-mil Narrow Body) SNC (Pb-Free) | | Industrial |
| | CY62256VLL-70ZI | 51-85071 | 28-pin TSOP I | | |
| | CY62256VLL-70ZXI | | 28-pin TSOP I (Pb-Free) | | |
| | CY62256VLL-70ZRI | 51-85074 | 28-pin Reverse TSOP I | | |
| | CY62256VLL-70ZRXI | | 28-pin Reverse TSOP I (Pb-Free) | | |
| | CY62256VLL-70SNE | 51-85092 | 28-pin (300-mil Narrow Body) SNC | | Automotive |
| | CY62256VLL-70SNXE | | 28-pin (300-mil Narrow Body) SNC (Pb-Free) | | |
| | CY62256VLL-70ZE | 51-85071 | 28-pin TSOP I | | |
| | CY62256VLL-70ZXE | | 28-pin TSOP I (Pb-Free) | | |
| | CY62256VLL-70ZRE | 51-85074 | 28-pin Reverse TSOP I | | |
| | CY62256VLL-70ZRXE | | 28-pin Reverse TSOP I (Pb-Free) | | |

Please contact your local Cypress sales representative for availability of these parts

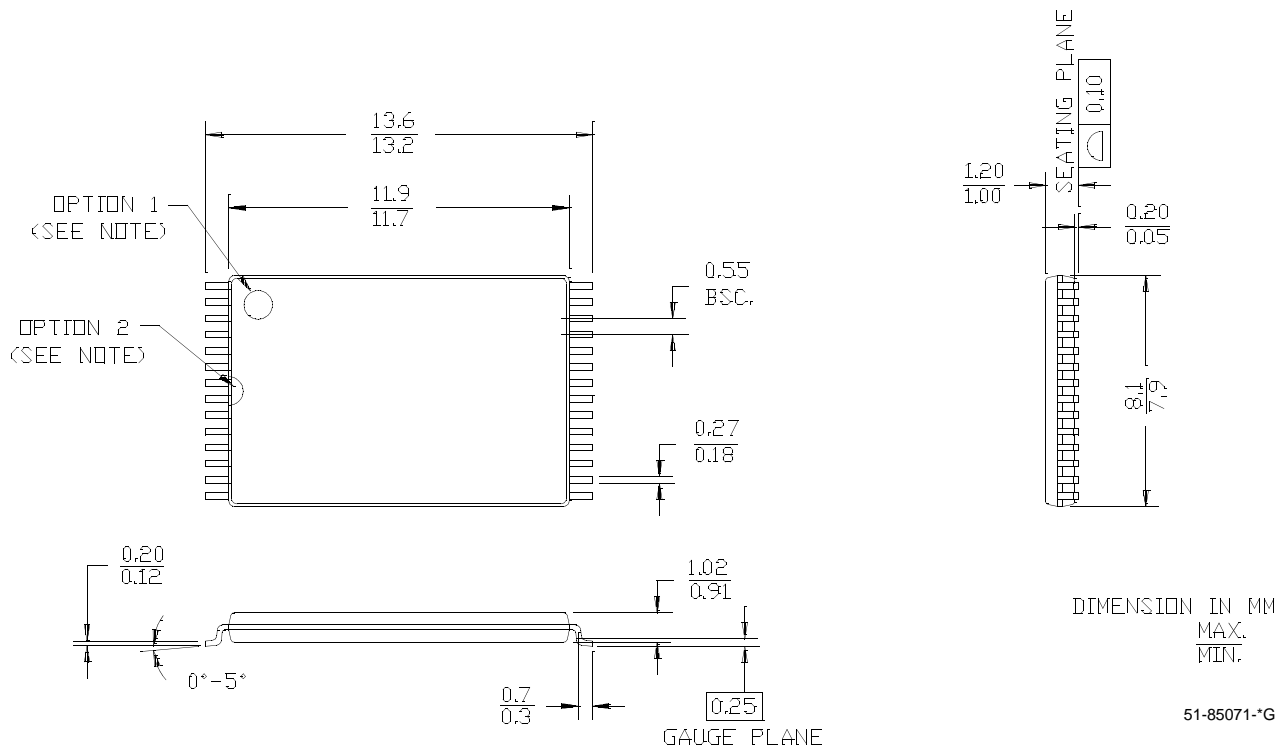
Package Diagrams

28-pin (300-mil) SNC (Narrow Body) (51-85092)



28-pin Thin Small Outline Package Type 1 (8 x 13.4 mm) (51-85071)

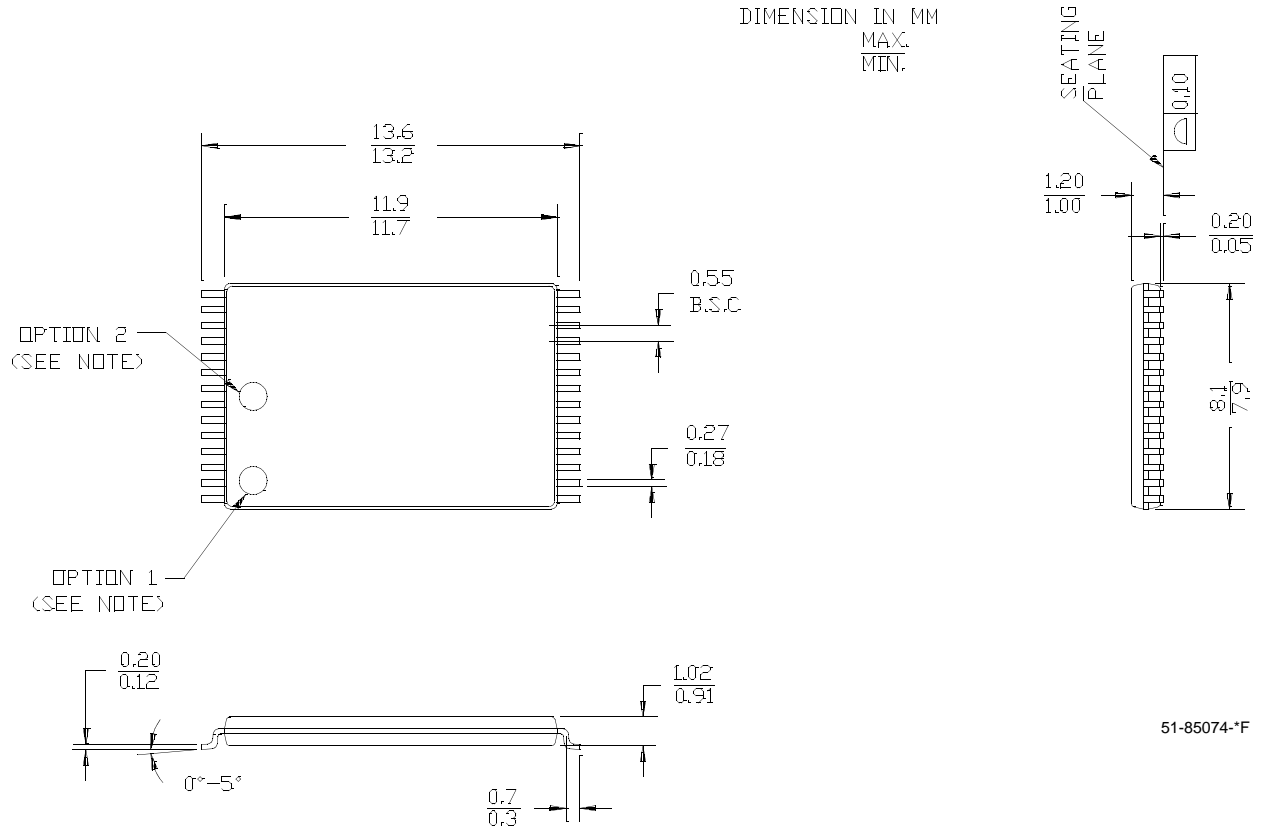
NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2



Package Diagrams (continued)

28-pin Reverse Thin Small Outline Package Type 1 (8 × 13.4 mm) (51-85074)

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2



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Document History Page

| Document Title: CY62256V, 256K (32K x 8) Static RAM Document Number: 38-05057 | | | | |
|--|---------|------------|-----------------|---|
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 107248 | 09/10/01 | SZV | Changed from spec number: 38-00519 to 38-05057 |
| *A | 111445 | 11/01/01 | MGN | Removed obsolete parts. Change to standard format |
| *B | 115229 | 05/23/02 | GBI | Changed SN package diagram |
| *C | 116507 | 09/04/02 | GBI | Added footnote 1 Clarified I _{CC} spec for V _{CC(typ)} = 2.5V |
| *D | 239134 | See ECN | AJU | Added Automotive product information |
| *E | 344595 | See ECN | SYT | Added Pb-Free packages on page# 10 |
| *F | 493277 | See ECN | VKN | Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court" Removed part # CY62256V25LL from the product offering Updated Ordering Information Table |