

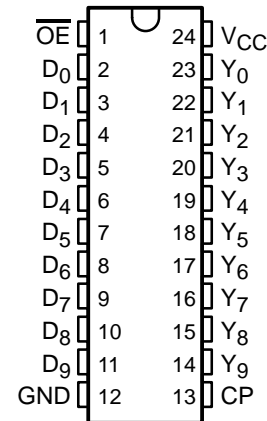
# CY74FCT821T

## 10-BIT BUS-INTERFACE REGISTER WITH 3-STATE OUTPUTS

SCCS033B– MAY 1994 – REVISED NOVEMBER 2001

- **Function, Pinout, and Drive Compatible With FCT, F Logic, and AM29821**
- **Reduced  $V_{OH}$  (Typically = 3.3 V) Version of Equivalent FCT Functions**
- **Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics**
- **$I_{off}$  Supports Partial-Power-Down Mode Operation**
- **Matched Rise and Fall Times**
- **Fully Compatible With TTL Input and Output Logic Levels**
- **ESD Protection Exceeds JESD 22**
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- **64-mA Output Sink Current**  
**32-mA Output Source Current**
- **High-Speed Parallel Register With Positive-Edge-Triggered D-Type Flip-Flops**
- **3-State Outputs**

**P, Q, OR SO PACKAGE  
(TOP VIEW)**



### description

This bus-interface register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The CY74FCT821T is a 10-bit-wide buffered version of the popular CY74FCT374 function. This device is ideal for use as an output port requiring high  $I_{OL}/I_{OH}$ .

This device is designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. Outputs are designed for low-capacitance bus loading in the high-impedance state.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

**PIN DESCRIPTION**

NAME	I/O	DESCRIPTION
D	I	D flip-flop data inputs
CP	O	Clock pulse for the register. Enters data into the register on the low-to-high clock transition.
Y	O	Register 3-state outputs
$\overline{OE}$	I	Output control. When $\overline{OE}$ is high, the Y outputs are in the high-impedance state. When $\overline{OE}$ is low, true register data is present at the Y outputs.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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# CY74FCT821T

## 10-BIT BUS-INTERFACE REGISTER

### WITH 3-STATE OUTPUTS

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#### ORDERING INFORMATION

TA	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QSOP – Q	Tape and reel	6	CY74FCT821CTQCT	FCT821C
	SOIC – SO	Tube	6	CY74FCT821CTSOC	FCT821C
		Tape and reel	6	CY74FCT821CTSUCT	
	DIP – P	Tube	7.5	CY74FCT821BTPC	CY74FCT821BTPC
	SOIC – SO	Tube	7.5	CY74FCT821BTSOC	FCT821B
		Tape and reel	7.5	CY74FCT821BTSUCT	
	QSOP – Q	Tape and reel	10	CY74FCT821ATQCT	FCT821A
	SOIC – SO	Tube	10	CY74FCT821ATSOC	FCT821A
Tape and reel		10	CY74FCT821ATSUCT		

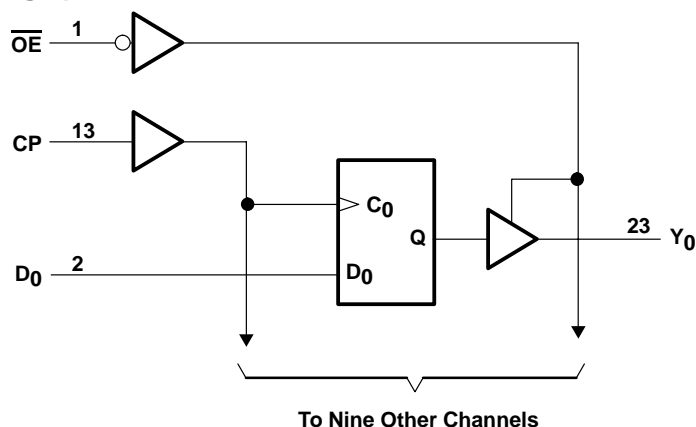
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

#### FUNCTION TABLE

INPUTS			INTERNAL OUTPUTS		FUNCTION
$\overline{OE}$	D	CP	Q	Y	
H	X	↑	L	Z	Z
H	L	↑	L	Z	Load
H	H	↑	H	Z	
L	L	↑	L	L	
L	H	↑	H	H	

H = High logic level, L = Low logic level, X = Don't care, ↑ = Low-to-high transition, Z = High-impedance state

#### logic diagram (positive logic)



**CY74FCT821T**  
**10-BIT BUS-INTERFACE REGISTER**  
**WITH 3-STATE OUTPUTS**

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**absolute maximum rating over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range to ground potential .....	–0.5 V to 7 V
DC input voltage range .....	–0.5 V to 7 V
DC output voltage range .....	–0.5 V to 7 V
DC output current (maximum sink current/pin) .....	120 mA
Package thermal impedance, $\theta_{JA}$ (see Note 1): P package .....	67°C/W
(see Note 2): Q package .....	61°C/W
(see Note 2): SO package .....	46°C/W
Ambient temperature range with power applied, $T_A$ .....	–65°C to 135°C
Storage temperature range, $T_{Stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The package thermal impedance is calculated in accordance with JESD 51-3.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 3)**

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	4.75	5	5.25	V
$V_{IH}$ High-level input voltage	2			V
$V_{IL}$ Low-level input voltage	0.8			V
$I_{OH}$ High-level output current	–32			mA
$I_{OL}$ Low-level output current	64			mA
$T_A$ Operating free-air temperature	–40		85	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.



# CY74FCT821T

## 10-BIT BUS-INTERFACE REGISTER

### WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	$V_{CC} = 4.75\text{ V}$ ,	$I_{IN} = -18\text{ mA}$		-0.7	-1.2	V
$V_{OH}$	$V_{CC} = 4.75\text{ V}$	$I_{OH} = -32\text{ mA}$		2		V
		$I_{OH} = -15\text{ mA}$	2.4	3.3		
$V_{OL}$	$V_{CC} = 4.75\text{ V}$ ,	$I_{OL} = 64\text{ mA}$		0.3	0.55	V
$V_{hys}$	All inputs			0.2		V
$I_I$	$V_{CC} = 5.25\text{ V}$ ,	$V_{IN} = V_{CC}$			5	$\mu\text{A}$
$I_{IH}$	$V_{CC} = 5.25\text{ V}$ ,	$V_{IN} = 2.7\text{ V}$			$\pm 1$	$\mu\text{A}$
$I_{IL}$	$V_{CC} = 5.25\text{ V}$ ,	$V_{IN} = 0.5\text{ V}$			$\pm 1$	$\mu\text{A}$
$I_{OZH}$	$V_{CC} = 5.25\text{ V}$ ,	$V_{OUT} = 2.7\text{ V}$			10	$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 5.25\text{ V}$ ,	$V_{OUT} = 0.5\text{ V}$			-10	$\mu\text{A}$
$I_{OS}^\ddagger$	$V_{CC} = 5.25\text{ V}$ ,	$V_{OUT} = 0\text{ V}$	-60	-120	-225	mA
$I_{off}$	$V_{CC} = 0\text{ V}$ ,	$V_{OUT} = 4.5\text{ V}$			$\pm 1$	$\mu\text{A}$
$I_{CC}$	$V_{CC} = 5.25\text{ V}$ ,	$V_{IN} \leq 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$		0.1	0.2	mA
$\Delta I_{CC}$	$V_{CC} = 5.25\text{ V}$ , $V_{IN} = 3.4\text{ V}^\S$ , $f_1 = 0$ , Outputs open			0.5	2	mA
$I_{CCD}^\P$	$V_{CC} = 5.25\text{ V}$ , One bit switching at 50% duty cycle, Outputs open, $OE = EN = \text{GND}$ , $V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$			0.06	0.12	mA/MHz
$I_{C\#}$	$V_{CC} = 5.25\text{ V}$ , Outputs open, $OE = \overline{EN} = \text{GND}$	One bit switching at $f_1 = 5\text{ MHz}$ at 50% duty cycle	$V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$	0.7	1.4	mA
			$V_{IN} = 3.4\text{ V}$ or GND	1.2	3.4	
		Eight bits switching at $f_1 = 2.5\text{ MHz}$ at 50% duty cycle	$V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$	1.6	3.2	
			$V_{IN} = 3.4\text{ V}$ or GND	3.9	12.2	
$C_i$				5	10	pF
$C_o$				9	12	pF

† Typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.

§ Per TTL-driven input ( $V_{IN} = 3.4\text{ V}$ ); all other inputs at  $V_{CC}$  or GND

¶ This parameter is derived for use in total power-supply calculations.

#  $I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

$I_C$  = Total supply current

$I_{CC}$  = Power-supply current with CMOS input levels

$\Delta I_{CC}$  = Power-supply current for a TTL high input ( $V_{IN} = 3.4\text{ V}$ )

$D_H$  = Duty cycle for TTL inputs high

$N_T$  = Number of TTL inputs at  $D_H$

$I_{CCD}$  = Dynamic current caused by an input transition pair (HLH or LHL)

$f_0$  = Clock frequency for registered devices, otherwise zero

$f_1$  = Input signal frequency

$N_1$  = Number of inputs changing at  $f_1$

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the  $I_{CC}$  formula.



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**10-BIT BUS-INTERFACE REGISTER**  
**WITH 3-STATE OUTPUTS**

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER			TEST LOAD	CY74FCT821AT		CY74FCT821BT		CY74FCT821CT		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	CP	$C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$	7		6		6		ns
$t_{su}$	Setup time, before CP $\uparrow$	Data	$C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$	4		3		3		ns
$t_h$	Hold time, after CP $\uparrow$	Data	$C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$	2		1.5		1.5		ns

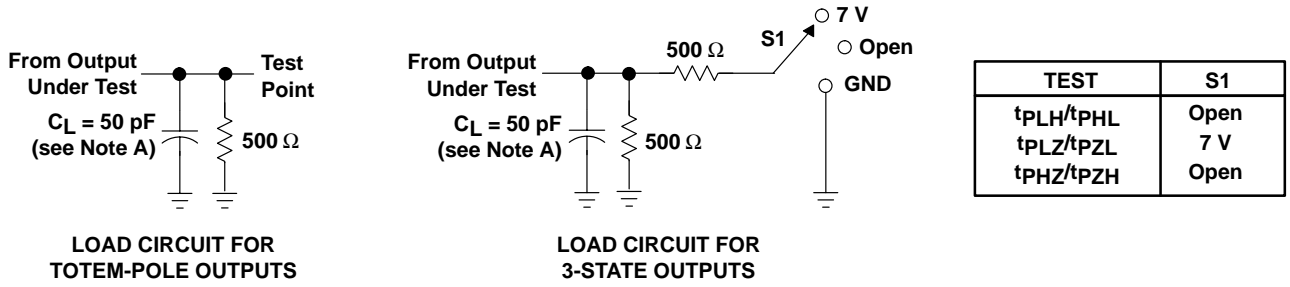
switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST LOAD	CY74FCT821AT		CY74FCT821BT		CY74FCT821CT		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	CP	Y	$C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$	10		7.5		6		ns
$t_{PHL}$				10		7.5		6		
$t_{PLH}$	CP	Y	$C_L = 300 \text{ pF}$ , $R_L = 500 \Omega$	20		15		12.5		ns
$t_{PHL}$				20		15		12.5		
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$	12		8		7		ns
$t_{PZL}$				12		8		7		
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 300 \text{ pF}$ , $R_L = 500 \Omega$	23		15		12.5		ns
$t_{PZL}$				23		15		12.5		
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 5 \text{ pF}$ , $R_L = 500 \Omega$	7		6.5		6		ns
$t_{PLZ}$				7		6.5		6		
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$	8		7.5		6.5		ns
$t_{PLZ}$				8		7.5		6.5		

**CY74FCT821T**  
**10-BIT BUS-INTERFACE REGISTER**  
**WITH 3-STATE OUTPUTS**

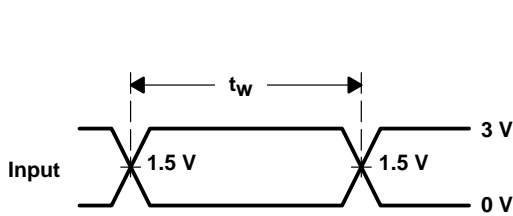
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**PARAMETER MEASUREMENT INFORMATION**

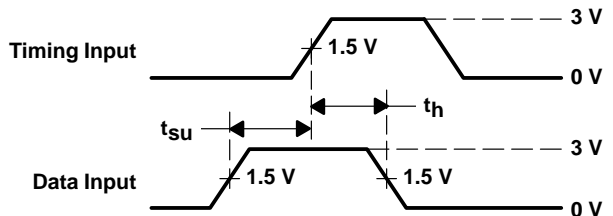


**LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS**

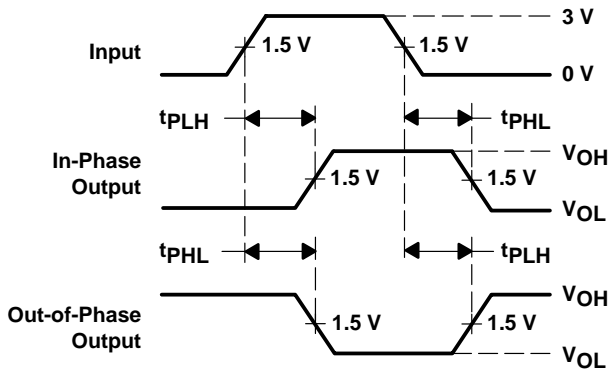
**LOAD CIRCUIT FOR 3-STATE OUTPUTS**



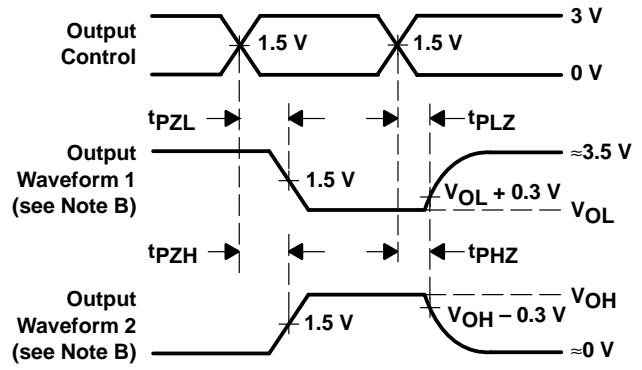
**VOLTAGE WAVEFORMS PULSE DURATION**



**VOLTAGE WAVEFORMS SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CY74FCT821ATQCT	ACTIVE	SSOP/QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT821ATQCTE4	ACTIVE	SSOP/QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT821ATQCTG4	ACTIVE	SSOP/QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT821ATSOC	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT821ATSOCE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT821ATSOCG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT821ATSOCT	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT821ATSOCTE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT821ATSOCTG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT821BTPC	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CY74FCT821BTPCE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CY74FCT821BTSOC	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT821BTSOCE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT821BTSOCG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT821BTSOCT	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT821BTSOCTE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT821BTSOCTG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT821CTQCT	ACTIVE	SSOP/QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT821CTQCTE4	ACTIVE	SSOP/QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT821CTQCTG4	ACTIVE	SSOP/QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT821CTSOC	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT821CTSOCE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT821CTSOCG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT821CTSOCT	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT821CTSOCTE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CY74FCT821CTSOCTG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT821ATQCT	SSOP/QSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT821ATSOCT	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CY74FCT821BTSOCT	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CY74FCT821CTQCT	SSOP/QSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT821CTSOCT	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT821ATQCT	SSOP/QSOP	DBQ	24	2500	346.0	346.0	33.0
CY74FCT821ATSOCT	SOIC	DW	24	2000	346.0	346.0	41.0
CY74FCT821BTSOCT	SOIC	DW	24	2000	346.0	346.0	41.0
CY74FCT821CTQCT	SSOP/QSOP	DBQ	24	2500	346.0	346.0	33.0
CY74FCT821CTSOCT	SOIC	DW	24	2000	346.0	346.0	41.0



NT (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.



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