# 1-Mbit (64K x 16) Static RAM

## Features

- **Temperature Range**
  - **— Automotive: –40°C to 125°C**
- **High speed**
  - **— $t_{AA}$ = 15 ns**
- **Optimized voltage range: 2.5V – 2.7V**
- **Low active power: 220 mW (Max.)**
- **Automatic power-down when deselected**
- **Independent control of upper and lower bits**
- **CMOS for optimum speed/power**
- **Available in Pb-free and non Pb-free 44-pin TSOP II , 44-pin (400-Mil) Molded SOJ and Pb-free 48-ball FPBGA packages**

## Functional Description

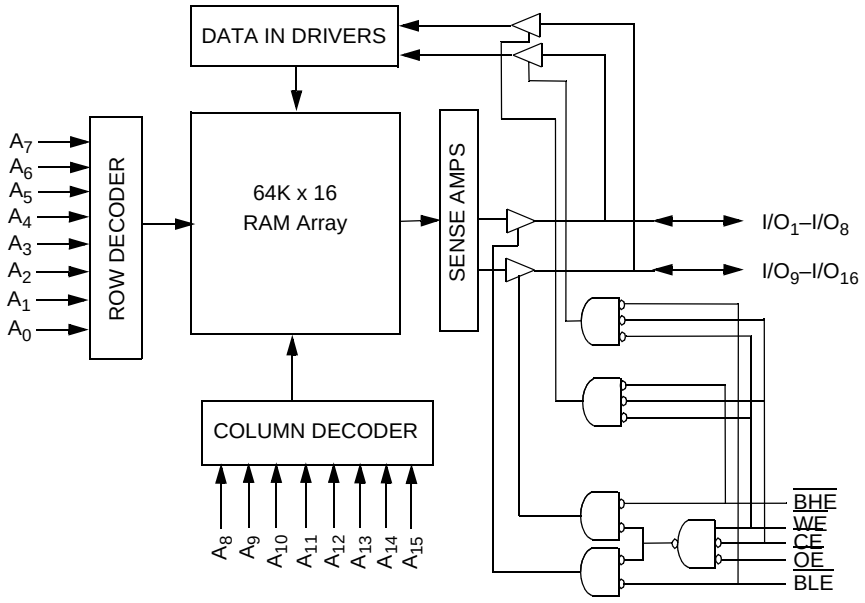
The CY7C1021CV26 is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins ($I/O_1$ through $I/O_8$), is written into the location specified on the address pins ($A_0$ through $A_{15}$). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins ($I/O_9$ through $I/O_{16}$) is written into the location specified on the address pins ($A_0$ through $A_{15}$).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on $I/O_1$ to $I/O_8$. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on $I/O_9$ to $I/O_{16}$. See the truth table at the end of this data sheet for a complete description of Read and Write modes.

The input/output pins ($I/O_1$ through $I/O_{16}$) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a Write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

## Logic Block Diagram



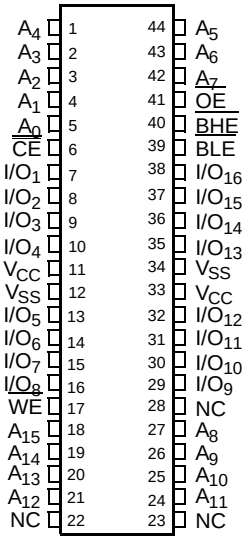

## Selection Guide[1]

| | -15 | Unit |
|---|---|---|
| Maximum Access Time | 15 | ns |
| Maximum Operating Current | 80 | mA |
| Maximum CMOS Standby Current | 10 | mA |

**Note:**
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25°C$.

## Pin Configuration[2]

**TSOP II -Top View**




## Pin Definitions

| Pin Name | Pin Number | I/O Type | Description |
|---|---|---|---|
| $A_0$–$A_{15}$ | 1–5, 18–21, 24–27, 42–44 | Input | **Address Inputs used to select one of the address locations.** |
| $I/O_1$–$I/O_{16}$ | 7–10, 13–16, 29–32, 35–38 | Input/Output | **Bidirectional Data I/O lines**. Used as input or output lines depending on operation. |
| NC | 22, 23, 28 | No Connect | **No Connects**. This pin is not connected to the die. |
| $\overline{WE}$ | 17 | Input/Control | **Write Enable Input, active LOW**. When selected LOW, a Write is conducted. When selected HIGH, a Read is conducted. |
| $\overline{CE}$ | 6 | Input/Control | **Chip Enable Input, active LOW**. When LOW, selects the chip. When HIGH, deselects the chip. |
| $\overline{BHE}$, $\overline{BLE}$ | 40, 39 | Input/Control | **Byte Write Select Inputs, active LOW**. $\overline{BHE}$ controls $I/O_{16}$–$I/O_9$, $\overline{BLE}$ controls $I/O_8$–$I/O_1$. |
| $\overline{OE}$ | 41 | Input/Control | **Output Enable, active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. |
| $V_{SS}$ | 12, 34 | Ground | **Ground for the device**. Should be connected to ground of the system. |
| $V_{CC}$ | 11, 33 | Power Supply | **Power Supply inputs to the device.** |

**Note:**
2. NC pins are not connected on the die.

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage on $V_{CC}$ to Relative GND[3] .... –0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State[3] ..... –0.5V to $V_{CC}$+0.5V

DC Input Voltage[3] ..... –0.5V to $V_{CC}$ + 0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... >200 mA

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Automotive | –40°C to +125°C | 2.5V–2.7V |

## Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | -15 | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $I_{OH}$ = –1.0 mA | 2.3 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $I_{OL}$ = 1.0 mA | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input LOW Voltage[3] | | –0.3 | 0.8 | V |
| $I_{IX}$ | Input Leakage Current | GND ≤ $V_I$ ≤ $V_{CC}$ | –3 | +3 | µA |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_I$ ≤ $V_{CC}$, Output Disabled | –3 | +3 | µA |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | $V_{CC}$ = Max., $I_{OUT}$ = 0 mA, f = $f_{MAX}$ = $1/t_{RC}$ | | 80 | mA |
| $I_{SB1}$ | Automatic CE Power-Down Current —TTL Inputs | Max. $V_{CC}$, $\overline{CE}$ ≥ $V_{IH}$ $V_{IN}$ ≥ $V_{IH}$ or $V_{IN}$ ≤ $V_{IL}$, f = $f_{MAX}$ | | 15 | mA |
| $I_{SB2}$ | Automatic CE Power-Down Current —CMOS Inputs | Max. $V_{CC}$, $\overline{CE}$ ≥ $V_{CC}$ – 0.3V, $V_{IN}$ ≥ $V_{CC}$ – 0.3V, or $V_{IN}$ ≤ 0.3V, f = 0 | | 10 | mA |

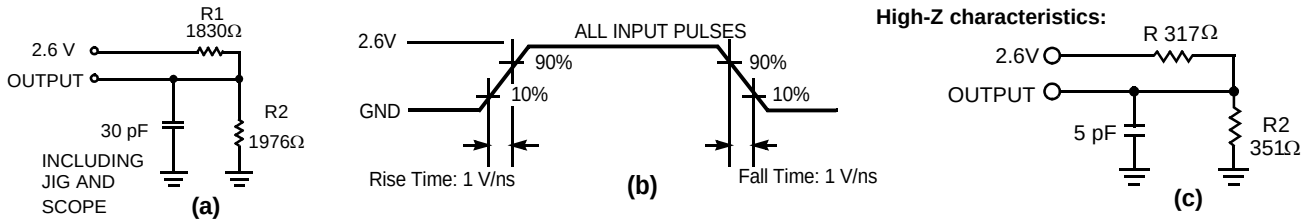
## Capacitance[4]

| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 2.6V | 8 | pF |
| $C_{OUT}$ | Output Capacitance | | 8 | pF |

## Thermal Resistance[4]

| Parameter | Description | Test Conditions | TSOP-II | Unit |
|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal Resistance (Junction to Ambient) | Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board | 76.92 | °C/W |
| $\Theta_{JC}$ | Thermal Resistance (Junction to Case) | | 15.86 | °C/W |

## AC Test Loads and Waveforms[5]




**Notes:**

3. $V_{IL}$ (min.) = –2.0V and $V_{IH}$(max) = $V_{CC}$ + 0.5V for pulse durations of less than 20 ns.
4. Tested initially and after any design or process changes that may affect these parameters
5. AC characteristics (except High-Z) are tested using the Thevenin load shown in Figure (a). High-Z characteristics are tested for all speeds using the test load shown in Figure (c)

## Switching Characteristics Over the Operating Range[6]

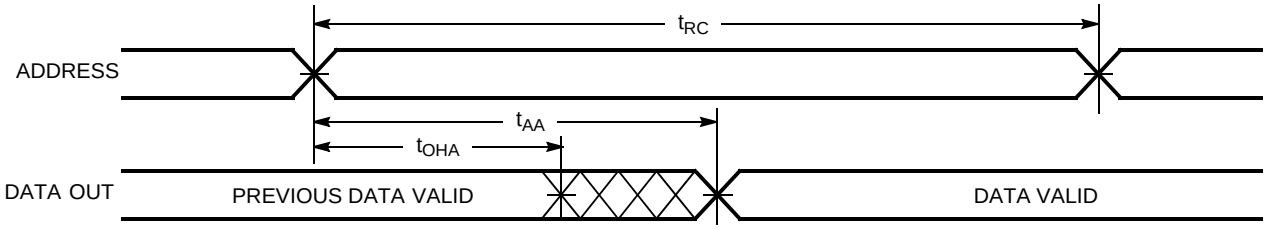
| Parameter | Description | -15 | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| **Read Cycle** | | | | |
| $t_{RC}$ | Read Cycle Time | 15 | | ns |
| $t_{AA}$ | Address to Data Valid | | 15 | ns |
| $t_{OHA}$ | Data Hold from Address Change | 3 | | ns |
| $t_{ACE}$ | $\overline{CE}$ LOW to Data Valid | | 15 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to Data Valid | | 7 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to Low-Z[7] | 0 | | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High-Z[7, 8] | | 7 | ns |
| $t_{LZCE}$ | $\overline{CE}$ LOW to Low-Z[7] | 3 | | ns |
| $t_{HZCE}$ | $\overline{CE}$ HIGH to High-Z[7, 8] | | 7 | ns |
| $t_{PU}$[9] | $\overline{CE}$ LOW to Power-Up | 0 | | ns |
| $t_{PD}$[9] | $\overline{CE}$ HIGH to Power-Down | | 15 | ns |
| $t_{DBE}$ | Byte Enable to Data Valid | | 7 | ns |
| $t_{LZBE}$ | Byte Enable to Low-Z | 0 | | ns |
| $t_{HZBE}$ | Byte Disable to High-Z | | 7 | ns |
| **Write Cycle**[10] | | | | |
| $t_{WC}$ | Write Cycle Time | 15 | | ns |
| $t_{SCE}$ | $\overline{CE}$ LOW to Write End | 10 | | ns |
| $t_{AW}$ | Address Set-Up to Write End | 10 | | ns |
| $t_{HA}$ | Address Hold from Write End | 0 | | ns |
| $t_{SA}$ | Address Set-Up to Write Start | 0 | | ns |
| $t_{PWE}$ | $\overline{WE}$ Pulse Width | 10 | | ns |
| $t_{SD}$ | Data Set-Up to Write End | 8 | | ns |
| $t_{HD}$ | Data Hold from Write End | 0 | | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low-Z[7] | 3 | | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High-Z[7, 8] | | 7 | ns |
| $t_{BW}$ | Byte Enable to End of Write | 9 | | ns |

**Notes:**

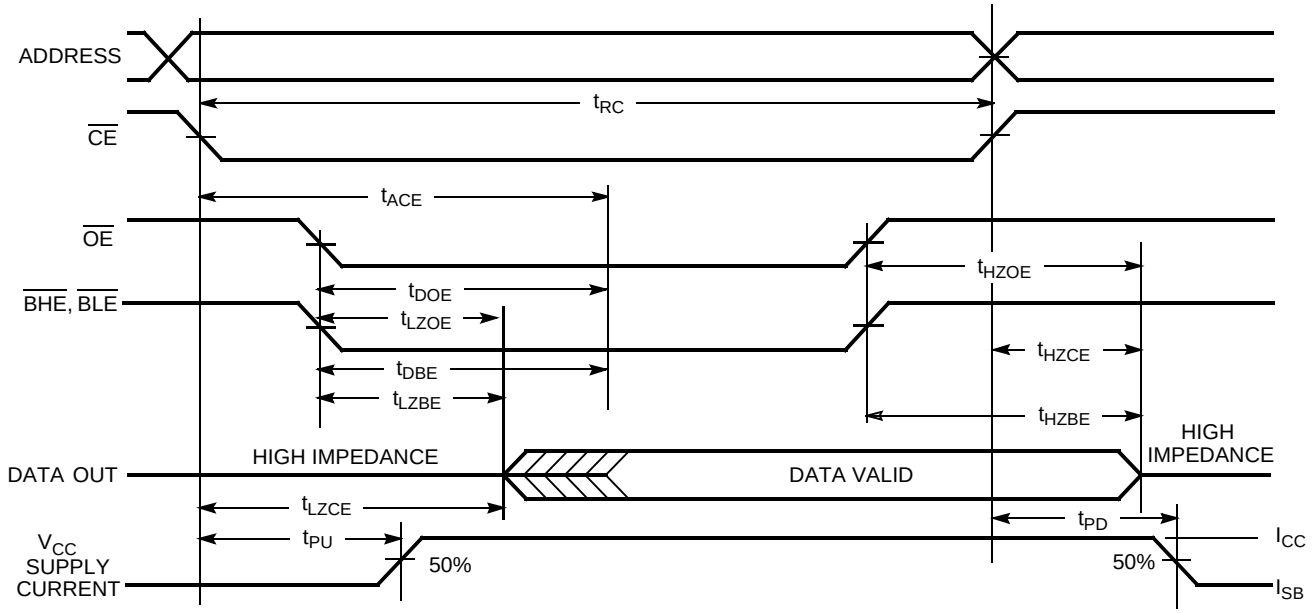
6. Test conditions assume signal transition time of 2.6 ns or less, timing reference levels of 1.3V, input pulse levels of 0 to 2.6V.
7. At any given temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any given device.
8. $t_{HZOE}$, $t_{HZBE}$, $t_{HZCE}$, and $t_{HZWE}$ are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
9. This parameter is guaranteed by design and is not tested.
10. The internal Write time of the memory is defined by the overlap of $\overline{CE}$ LOW, $\overline{WE}$ LOW and $\overline{BHE}/\overline{BLE}$ LOW. $\overline{CE}$, $\overline{WE}$ and $\overline{BHE}/\overline{BLE}$ must be LOW to initiate a Write, and the transition of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.

## Switching Waveforms

### Read Cycle No. 1[11, 12]



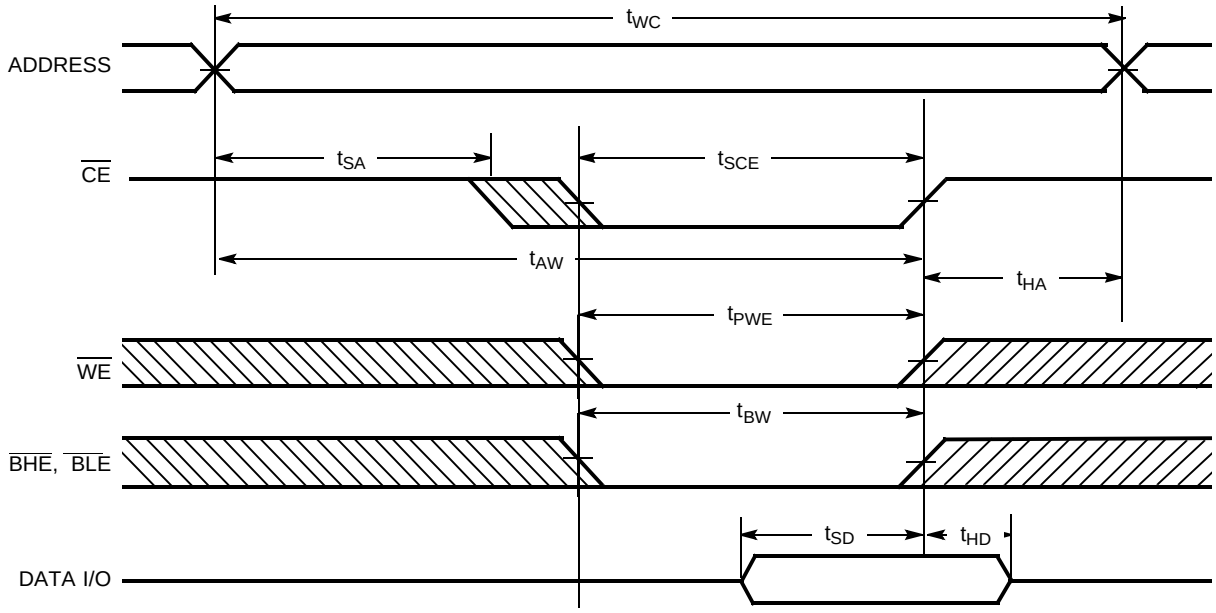

### Read Cycle No. 2 ($\overline{OE}$ Controlled)[12, 13]



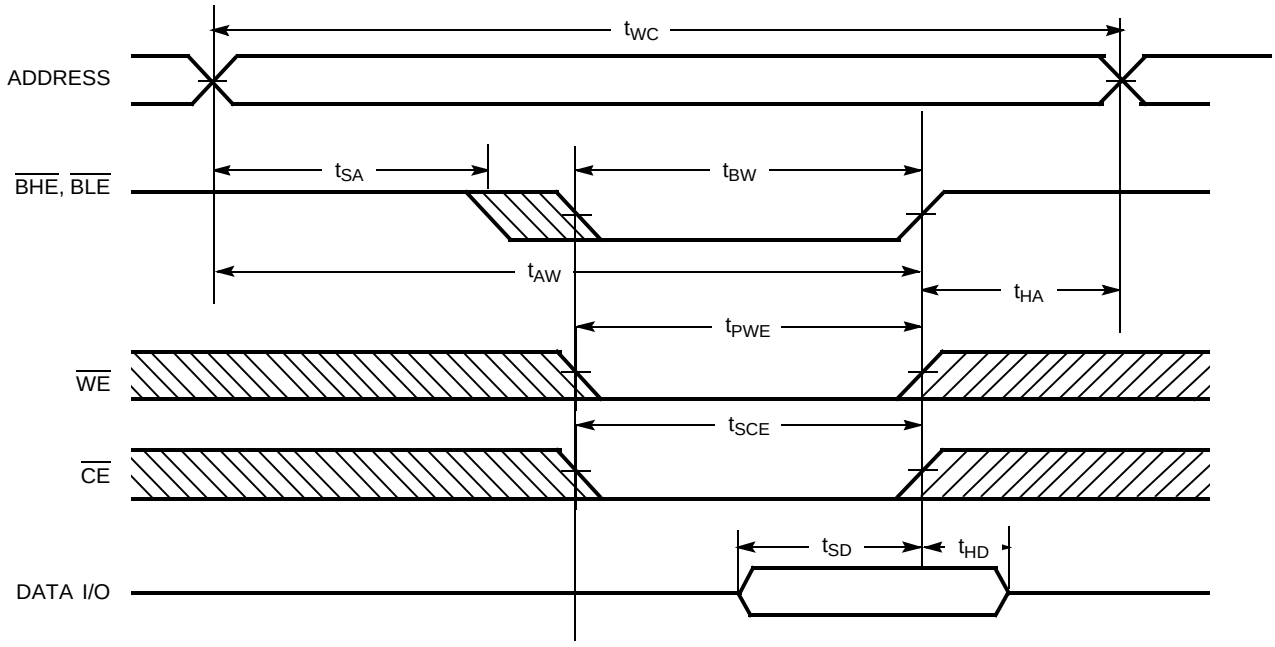

**Notes:**
11. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$ and/or $\overline{BLE}$ = $V_{IL}$.
12. $\overline{WE}$ is HIGH for Read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

## Switching Waveforms (continued)

### Write Cycle No. 1 ($\overline{CE}$ Controlled)[14, 15]



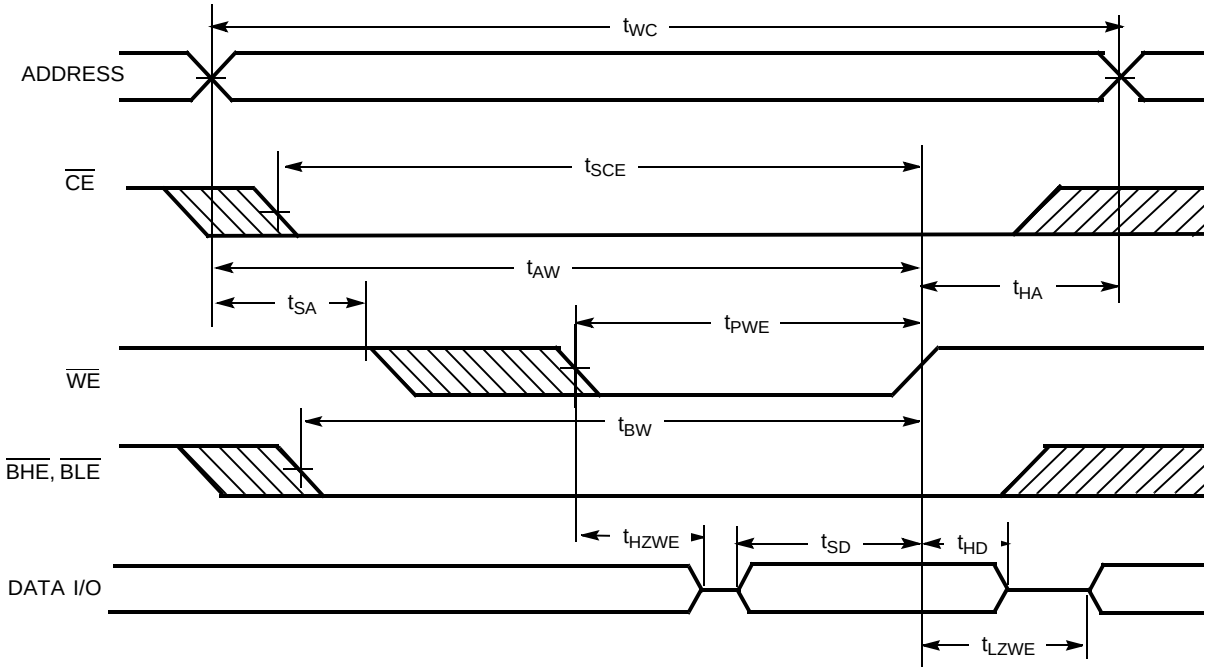

### Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)




**Notes:**
14. Data I/O is high-impedance if $\overline{OE}$ or $\overline{BHE}$ and/or $\overline{BLE}$= $V_{IH}$.
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

## Switching Waveforms (continued)

### Write Cycle No. 3 ($\overline{WE}$ Controlled, LOW)




## Truth Table

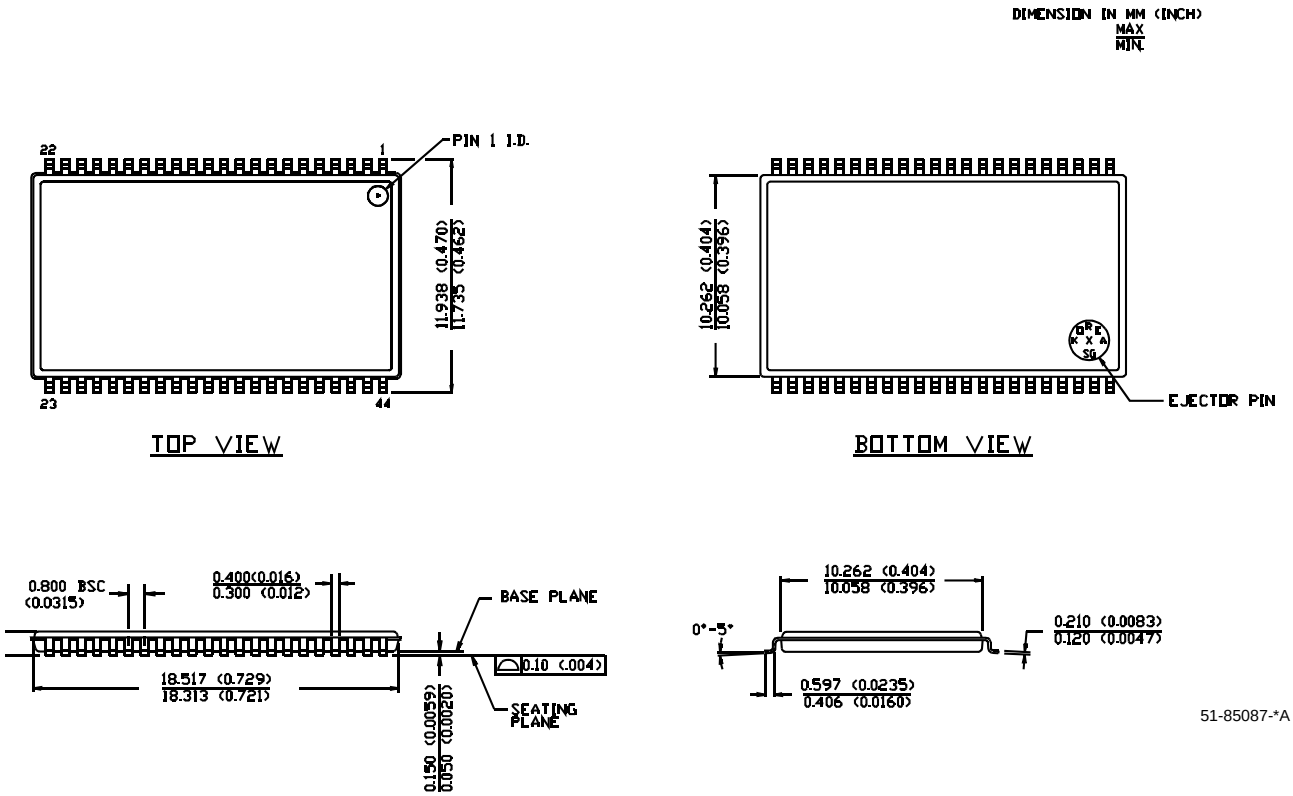
| $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | $\overline{BLE}$ | $\overline{BHE}$ | $I/O_1–I/O_8$ | $I/O_9–I/O_{16}$ | Mode | Power |
|---|---|---|---|---|---|---|---|---|
| H | X | X | X | X | High-Z | High-Z | Power-down | Standby ($I_{SB}$) |
| L | L | H | L | L | Data Out | Data Out | Read – All bits | Active ($I_{CC}$) |
| | | | L | H | Data Out | High-Z | Read – Lower bits only | Active ($I_{CC}$) |
| | | | H | L | High-Z | Data Out | Read – Upper bits only | Active ($I_{CC}$) |
| L | X | L | L | L | Data In | Data In | Write – All bits | Active ($I_{CC}$) |
| | | | L | H | Data In | High-Z | Write – Lower bits only | Active ($I_{CC}$) |
| | | | H | L | High-Z | Data In | Write – Upper bits only | Active ($I_{CC}$) |
| L | H | H | X | X | High-Z | High-Z | Selected, Outputs Disabled | Active ($I_{CC}$) |
| L | X | X | H | H | High-Z | High-Z | Selected, Outputs Disabled | Active ($I_{CC}$) |

## Ordering Information

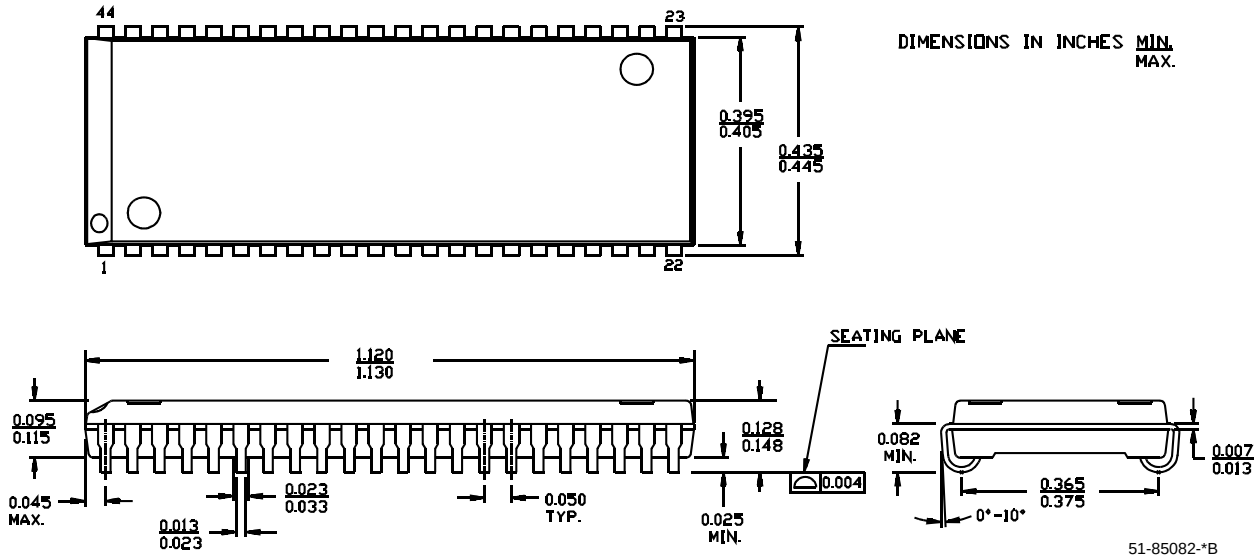
| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 15 | CY7C1021CV26-15ZE | 51-85087 | 44-pin TSOP Type II | Automotive |
| | CY7C1021CV26-15ZSXE | | 44-pin TSOP Type II (Pb-Free) | |
| | CY7C1021CV26-15VE | 51-85082 | 44-pin (400-Mil) Molded SOJ | |
| | CY7C1021CV26-15VXE | | 44-pin (400-Mil) Molded SOJ (Pb-Free) | |
| | CY7C1021CV26-15BAE | 51-85150 | 48-ball FPBGA (6 × 8 × 1 mm) (Pb-Free) | |

## Package Diagrams

**44-pin TSOP II (51-85087)**

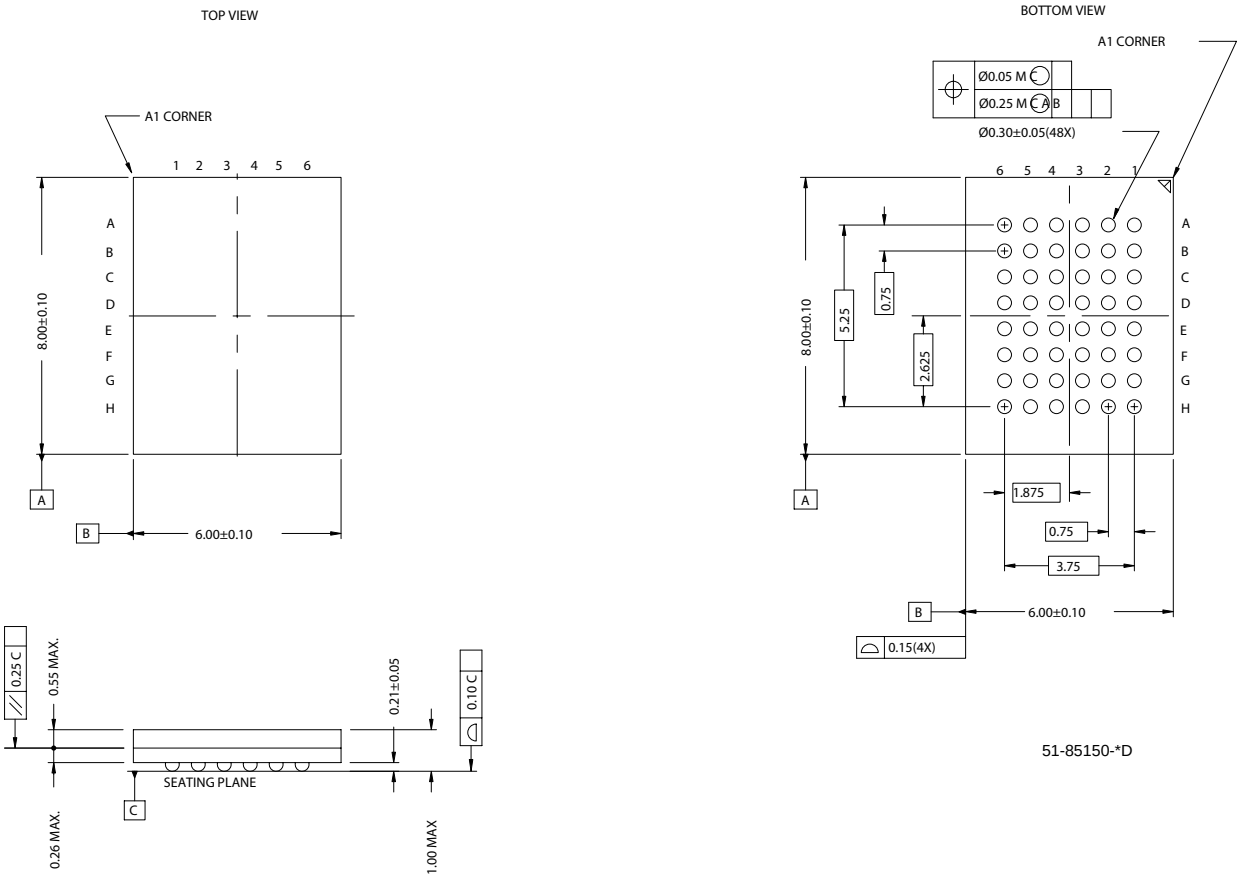



**44-pin (400-Mil) Molded SOJ (51-85082)**



## Package Diagrams (continued)

**48-ball FBGA (6 x 8 x 1 mm) (51-85150)**

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## Document History Page

| Document Title: CY7C1021CV26 1-Mbit (64K x 16) Static RAM<br>Document Number: 38-05589 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 238454 | See ECN | RKF | New data sheet for Automotive |
| *A | 335861 | See ECN | SYT | Added Lead-Free Product Information<br>Included the 44-Lead (400-Mil) Molded SOJ V34 Package |
| *B | 493543 | See ECN | NXR | Changed the description of $I_{IX}$ from Input Load Current to Input Leakage Current in DC Electrical Characteristics table<br>Removed $I_{OS}$ parameter from DC Electrical Characteristics table<br>Updated Ordering Information Table |