

256K (32K x 8) Static RAM

Features

- Pin- and function-compatible with CY7C199C
- High speed
 - $t_{AA} = 10 \text{ ns}$
- Low active power
 - $I_{CC} = 80 \text{ mA @ } 10 \text{ ns}$
- Low CMOS standby power
 - $I_{SB2} = 3 \text{ mA}$
- 2.0V Data Retention
- Automatic power-down when deselected
- CMOS for optimum speed/power
- TTL-compatible inputs and outputs
- Easy memory expansion with \overline{CE} and \overline{OE} features
- Available in Pb-free 28-pin 300-Mil wide Molded SOJ and 28-pin TSOP I packages

Functional Description ^[1]

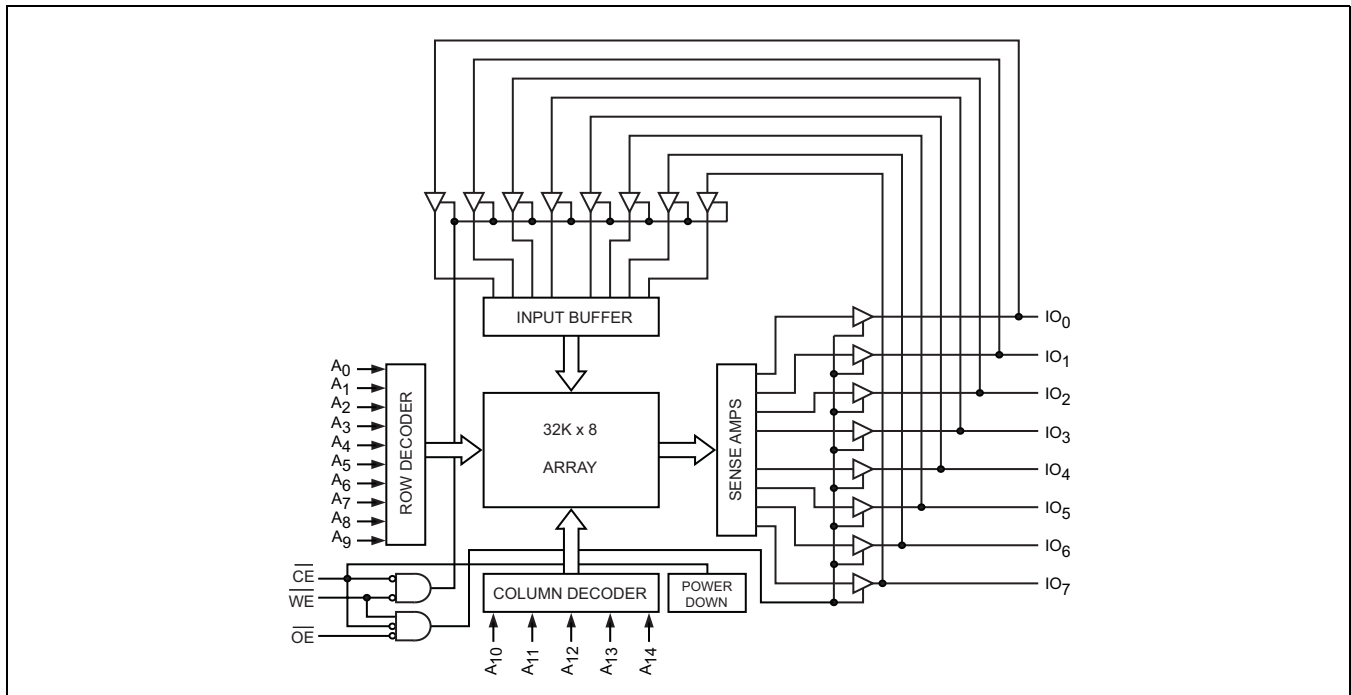
The CY7C199D is a high-performance CMOS static RAM organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable (\overline{CE}), an active LOW Output Enable (\overline{OE}) and tri-state drivers. This device has an automatic power-down feature, reducing the power consumption when deselected. The input and output pins (IO₀ through IO₇) are placed in a high-impedance state when:

- Deselected (\overline{CE} HIGH)
- Outputs are disabled (\overline{OE} HIGH)
- When the write operation is active (\overline{CE} LOW and \overline{WE} LOW)

Write to the device by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. Data on the eight IO pins (IO₀ through IO₇) is then written into the location specified on the address pins (A₀ through A₁₄).

Read from the device by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing Write Enable (\overline{WE}) HIGH. Under these conditions, the contents of the memory location specified by the address pins appears on the IO pins.

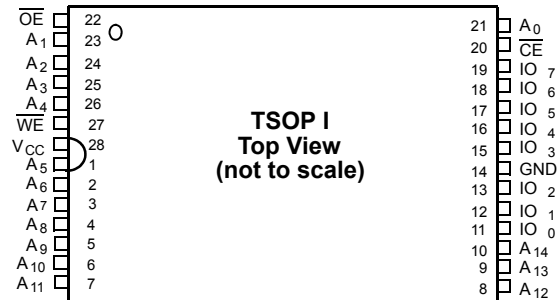
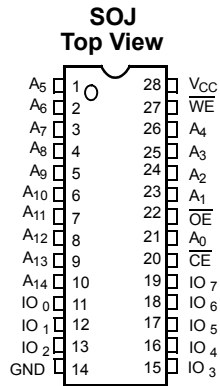
Logic Block Diagram



Note:

1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com.

Pin Configurations



Selection Guide

	CY7C199D-10	Unit
Maximum Access Time	10	ns
Maximum Operating Current	80	mA
Maximum CMOS Standby Current	3	mA

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature -65°C to +150°C

Ambient Temperature with

Power Applied..... -55°C to +125°C

Supply Voltage on V_{CC} to Relative GND ^[2] ... -0.5V to +6.0V

DC Voltage Applied to Outputs

in High-Z State ^[2] -0.5V to $V_{CC} + 0.5V$

DC Input Voltage ^[2] -0.5V to $V_{CC} + 0.5V$

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V
(per MIL-STD-883, Method 3015)

Latch-up Current > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}	Speed
Industrial	-40°C to +85°C	5V ± 0.5V	10 ns

Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions	7C199D-10		Unit
			Min	Max	
V_{OH}	Output HIGH Voltage	$I_{OH} = -4.0$ mA	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 8.0$ mA		0.4	V
V_{IH}	Input HIGH Voltage ^[2]		2.0	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage ^[2]		-0.5	0.8	V
I_{IX}	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1	+1	μA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$, Output Disabled	-1	+1	μA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max}$, $I_{OUT} = 0$ mA, $f = f_{max} = 1/t_{RC}$	100 MHz	80	mA
			83 MHz	72	mA
			66 MHz	58	mA
			40 MHz	37	mA
I_{SB1}	Automatic CE Power-down Current— TTL Inputs	Max V_{CC} , $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{max}$		10	mA
I_{SB2}	Automatic CE Power-down Current— CMOS Inputs	Max V_{CC} , $\overline{CE} \geq V_{CC} - 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$, $f = 0$		3	mA

Note:

2. $V_{IL}(\text{min}) = -2.0V$ and $V_{IH}(\text{max}) = V_{CC} + 1V$ for pulse durations of less than 5 ns.

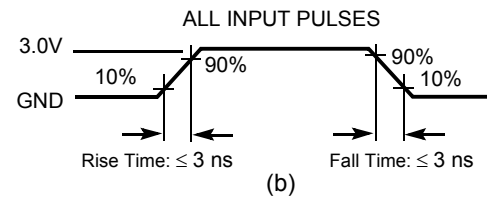
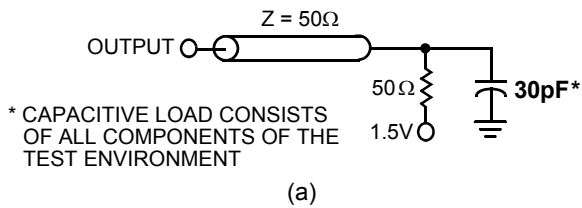
Capacitance ^[3]

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 5.0\text{V}$	8	pF
C_{OUT}	Output Capacitance		8	pF

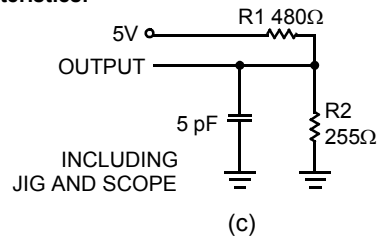
Thermal Resistance ^[3]

Parameter	Description	Test Conditions	SOJ	TSOP I	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	59.16	54.65	$^\circ\text{C/W}$
Θ_{JC}	Thermal Resistance (Junction to Case)		40.84	21.49	$^\circ\text{C/W}$

AC Test Loads and Waveforms ^[4]



High-Z characteristics:



Notes:

3. Tested initially and after any design or process changes that may affect these parameters.
4. AC characteristics (except High-Z) are tested using the load conditions shown in Figure (a). High-Z characteristics are tested for all speeds using the test load shown in Figure (c).

Switching Characteristics (Over the Operating Range) ^[5]

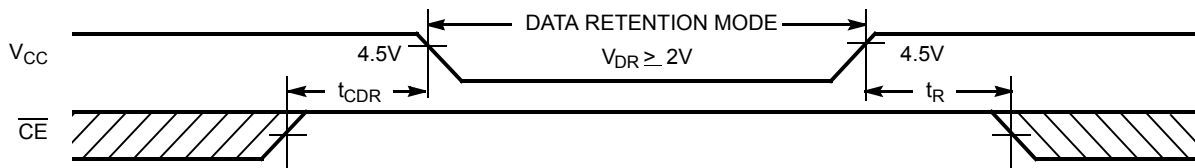
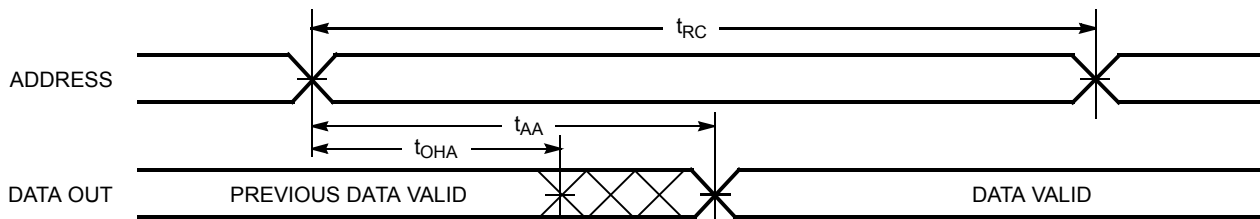
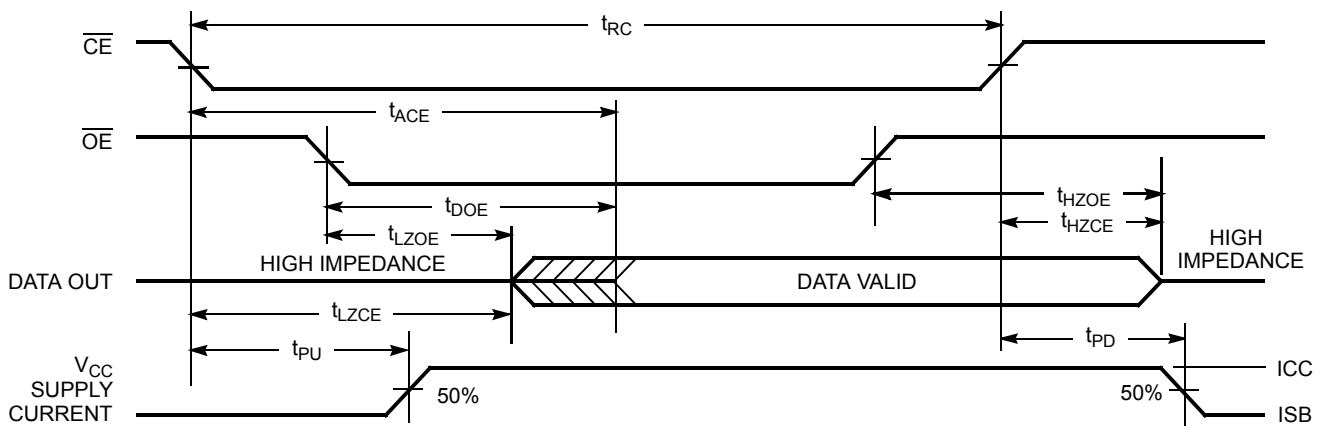
Parameter	Description	7C199D-10		Unit
		Min	Max	
Read Cycle				
$t_{\text{power}}^{[6]}$	V_{CC} (typical) to the first access	100		μs
t_{RC}	Read Cycle Time	10		ns
t_{AA}	Address to Data Valid		10	ns
t_{OHA}	Data Hold from Address Change	3		ns
t_{ACE}	$\overline{\text{CE}}$ LOW to Data Valid		10	ns
t_{DOE}	$\overline{\text{OE}}$ LOW to Data Valid		5	ns
$t_{\text{LZOE}}^{[7]}$	$\overline{\text{OE}}$ LOW to Low-Z	0		ns
$t_{\text{HZOE}}^{[7, 8]}$	$\overline{\text{OE}}$ HIGH to High-Z		5	ns
$t_{\text{LZCE}}^{[7]}$	$\overline{\text{CE}}$ LOW to Low-Z	3		ns
$t_{\text{HZCE}}^{[7, 8]}$	$\overline{\text{CE}}$ HIGH to High-Z		5	ns
$t_{\text{PU}}^{[9]}$	$\overline{\text{CE}}$ LOW to Power-up	0		ns
$t_{\text{PD}}^{[9]}$	$\overline{\text{CE}}$ HIGH to Power-down		10	ns
Write Cycle ^[10, 11]				
t_{WC}	Write Cycle Time	10		ns
t_{SCE}	$\overline{\text{CE}}$ LOW to Write End	7		ns
t_{AW}	Address Set-up to Write End	7		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-up to Write Start	0		ns
t_{PWE}	$\overline{\text{WE}}$ Pulse Width	7		ns
t_{SD}	Data Set-up to Write End	5		ns
t_{HD}	Data Hold from Write End	0		ns
$t_{\text{HZWE}}^{[7]}$	$\overline{\text{WE}}$ LOW to High-Z		6	ns
$t_{\text{LZWE}}^{[7, 8]}$	$\overline{\text{WE}}$ HIGH to Low-Z	3		ns

Notes:

- Test conditions assume signal transition time of 3 ns or less for all speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified $I_{\text{OL}}/I_{\text{OH}}$ and 30-pF load capacitance.
- t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with $C_{\text{L}} = 5 \text{ pF}$ as in part (b) of "AC Test Loads and Waveforms ^[4]" on page 4. Transition is measured $\pm 200 \text{ mV}$ from steady-state voltage.
- This parameter is guaranteed by design and is not tested.
- The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 ($\overline{\text{WE}}$ controlled, $\overline{\text{OE}}$ LOW) is the sum of t_{HZWE} and t_{SD} .

Data Retention Characteristics (Over the Operating Range)

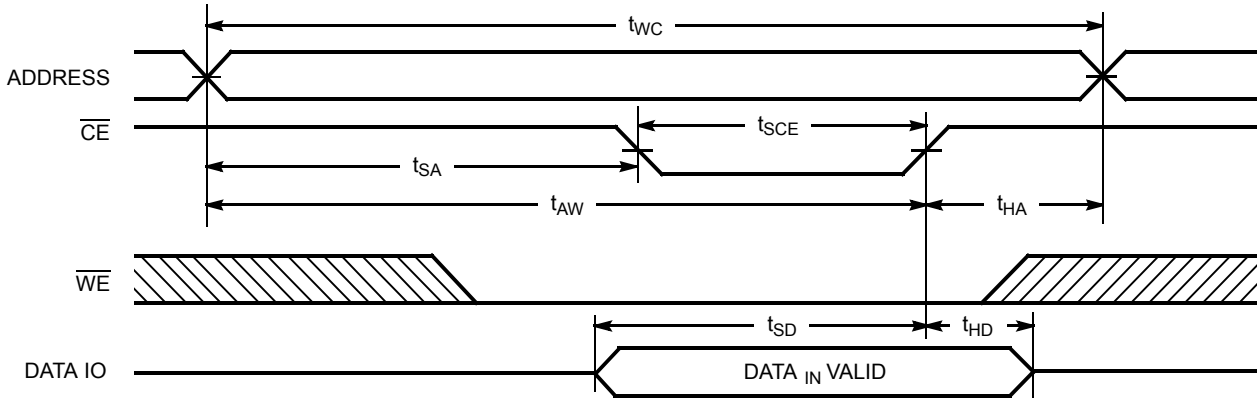
Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for Data Retention	$V_{CC} = V_{DR} = 2.0V, \overline{CE} \geq V_{CC} - 0.3V,$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	2.0		V
I_{CCDR}	Data Retention Current			3	mA
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time		0		ns
$t_R^{[12]}$	Operation Recovery Time		t_{RC}		ns

Data Retention Waveform

Switching Waveforms
Read Cycle No. 1 (Address Transition Controlled) [13, 14]

Read Cycle No. 2 (\overline{OE} Controlled) [14, 15]

Notes:

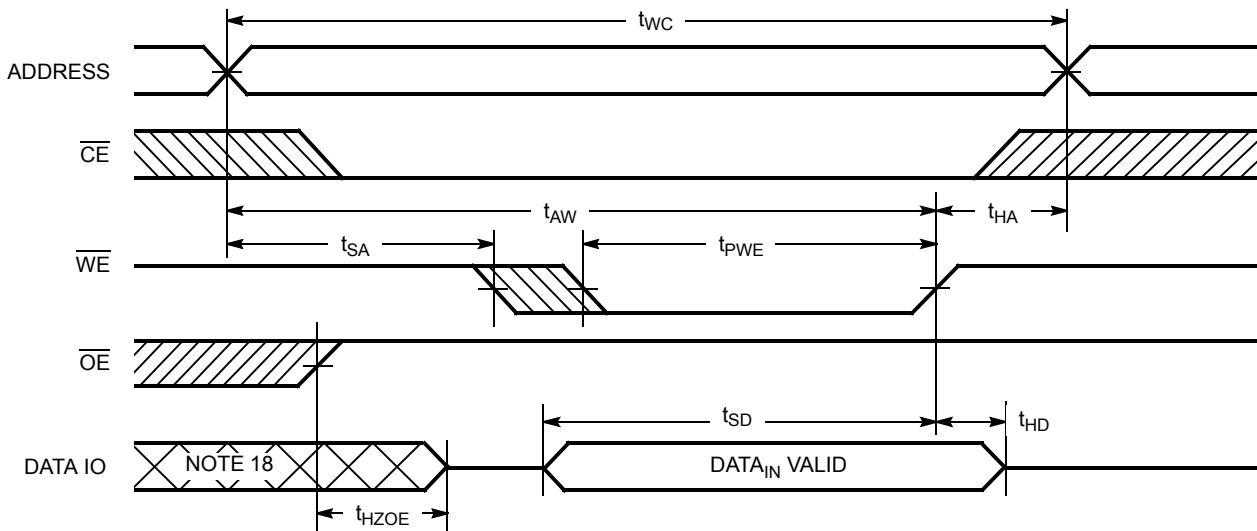
12. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 50 \mu s$ or stable at $V_{CC(min)} \geq 50 \mu s$.
13. Device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}$.
14. \overline{WE} is HIGH for read cycle.
15. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)

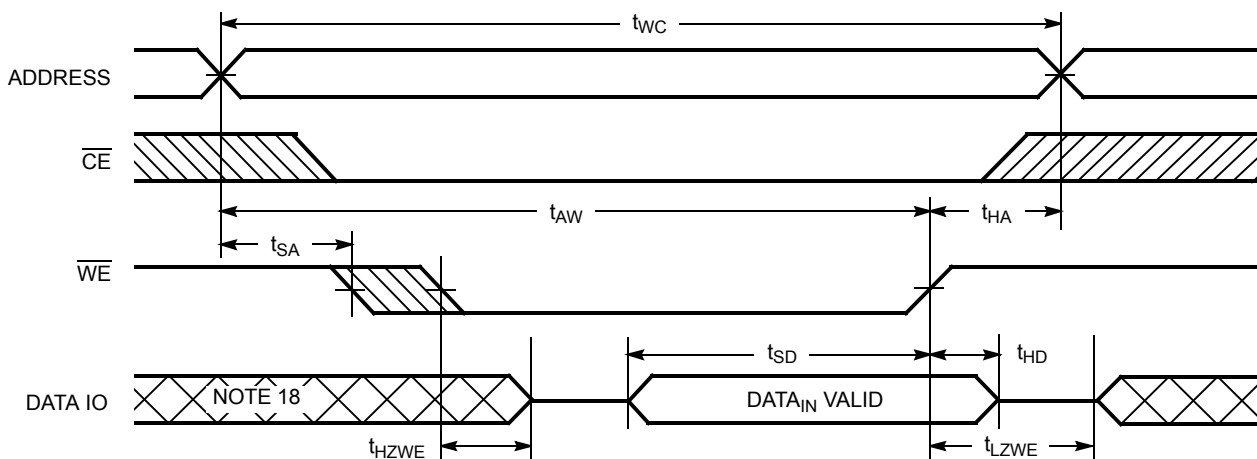
Write Cycle No. 1 (\overline{CE} Controlled) [10, 16, 17]



Write Cycle No. 2 (\overline{WE} Controlled) [10, 16, 17]



Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) [11, 17]



Notes:

- 16. Data IO is high impedance if $\overline{OE} = V_{IH}$.
- 17. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.
- 18. During this period the IOs are in the output state and input signals should not be applied.

Truth Table

\overline{CE}	\overline{WE}	\overline{OE}	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Deselect, Output disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C199D-10VXI	51-85031	28-pin (300-Mil) Molded SOJ (Pb-Free)	Industrial
	CY7C199D-10ZXI	51-85071	28-pin TSOP Type I (Pb-free)	

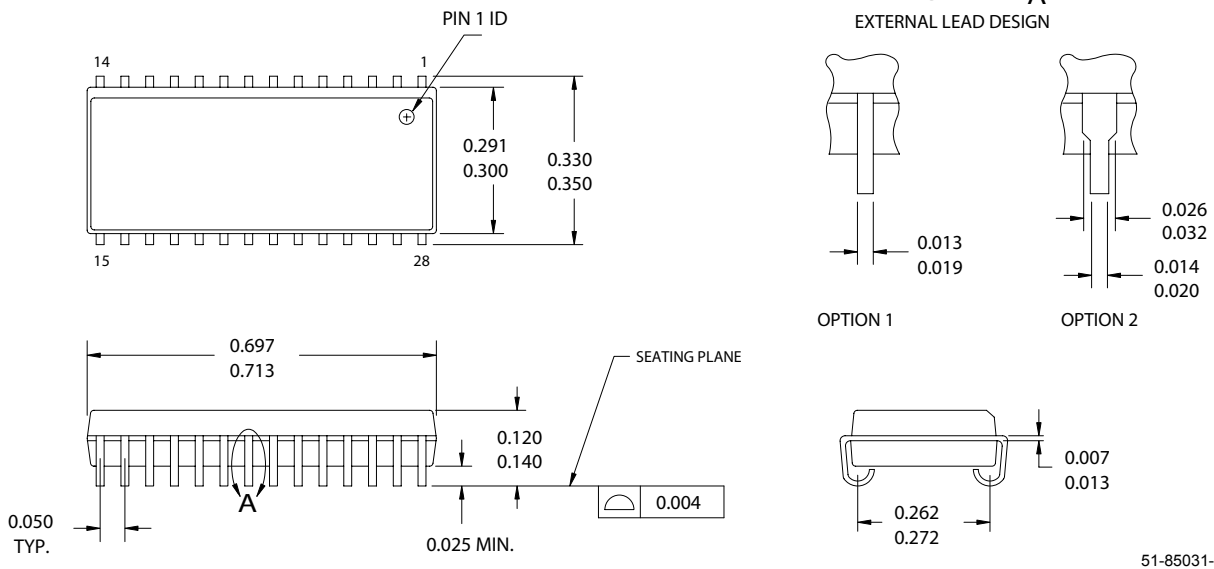
Please contact your local Cypress sales representative for availability of these parts.

Package Diagrams

Figure 1. 28-pin (300-Mil) Molded SOJ, 51-85031

NOTE :

1. JEDEC STD REF MO088
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.006 in (0.152 mm) PER SIDE
3. DIMENSIONS IN INCHES
MIN.
MAX.

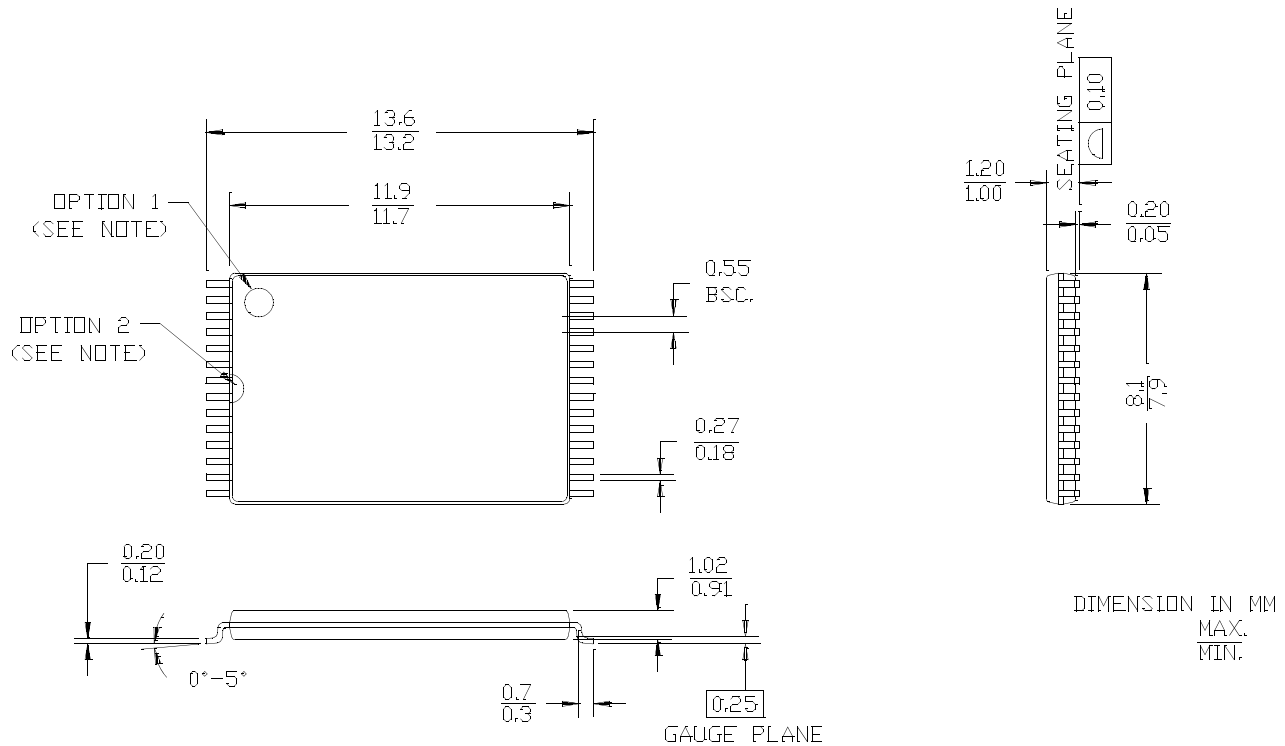


51-85031-°C

Package Diagrams (continued)

Figure 2. 28-pin Thin Small Outline Package Type 1 (8x13.4 mm), 51-85071

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2



51-85071-G

All products and company names mentioned in this document are the trademarks of their respective holders.

Document History Page

Document Title: CY7C199D, 256K (32K x 8) Static RAM				
Document Number: 38-05471				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	201560	See ECN	SWI	Advance Information data sheet for C9 IPP
*A	233728	See ECN	RKF	DC parameters modified as per EROS (Spec # 01-02165) Pb-free Offering in Ordering Information
*B	262950	See ECN	RKF	Removed 28-LCC Pinout and Package Diagrams Added Data Retention Characteristics table Added T _{power} Spec in Switching Characteristics table Shaded Ordering Information
*C	307594	See ECN	RKF	Reduced Speed bins to -10, -12 and -15 ns
*D	820660	See ECN	VKN	Converted from Preliminary to Final Removed 12 ns and 15 ns speed bin Removed Commercial Operating range Removed "L" part Removed 28-pin PDIP and 28-pin SOIC package Changed Overshoot spec from V _{CC} +2V to V _{CC} +1V in footnote #2 Changed I _{CC} spec from 60 mA to 80 mA for 100 MHz speed bin Added I _{CC} specs for 83 MHz, 66 MHz and 40 MHz speed bins Updated Thermal Resistance table Updated Ordering Information Table