# 2.5V CMOS Static RAM 1 Meg (64K x 16-Bit)

**IDT71T016SA**

## Features

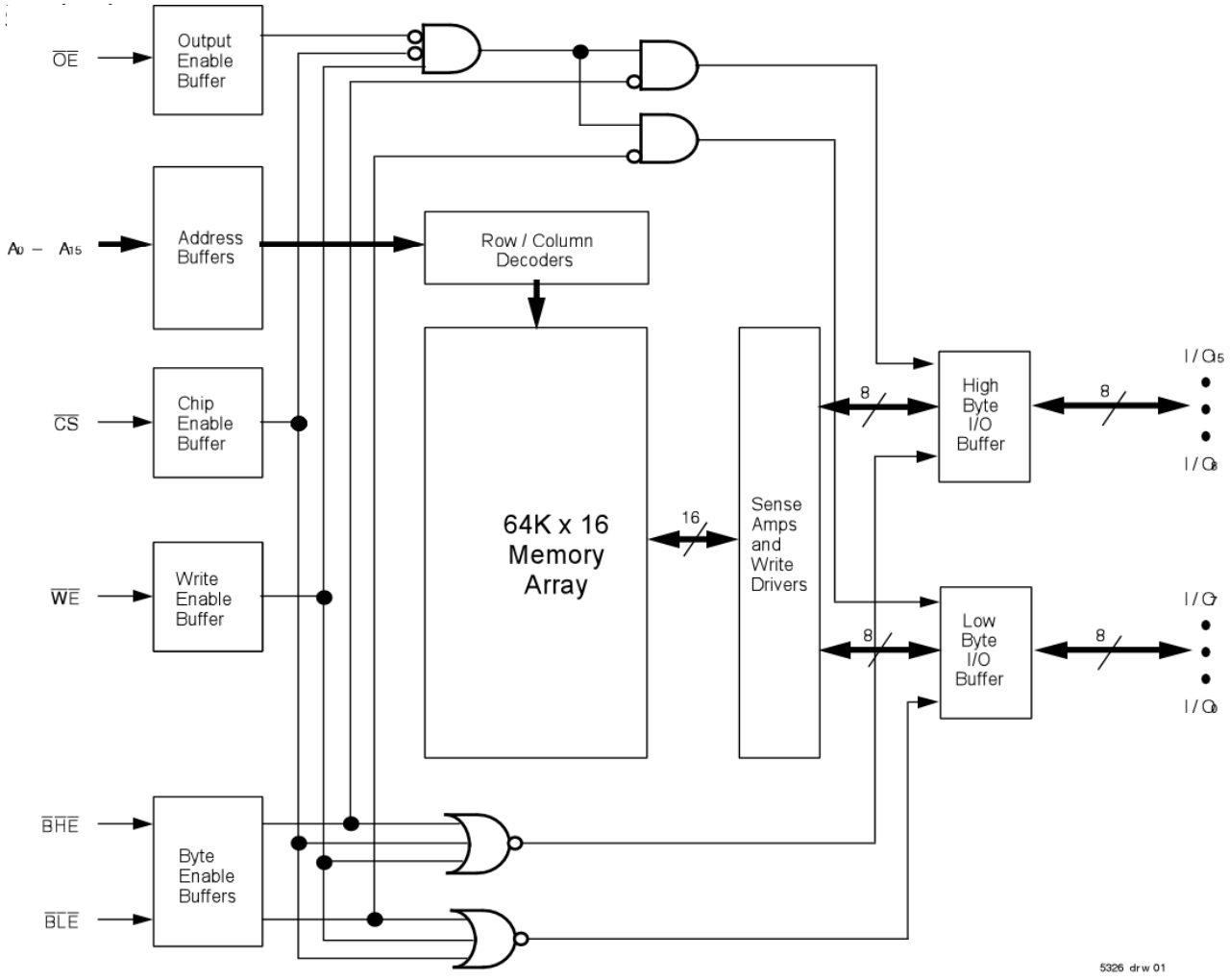
- **64K x 16 advanced high-speed CMOS Static RAM**
- **Equal access and cycle times**
  - *— Commercial and Industrial: 12/15/20ns*
- **One Chip Select plus one Output Enable pin**
- **Bidirectional data inputs and outputs directly LVTTL-compatible**
- **Low power consumption via chip deselect**
- **Upper and Lower Byte Enable Pins**
- **Single 2.5V power supply**
- **Available in 44-pin TSOP package**

The IDT71T016 is a 1,048,576-bit high-speed Static RAM organized as 64K x 16. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

The IDT71T016 has an output enable pin which operates as fast as 6ns, with address access times as fast as 12ns. All bidirectional inputs and outputs of the IDT71T016 are LVTTL-compatible and operation is from a single 2.5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

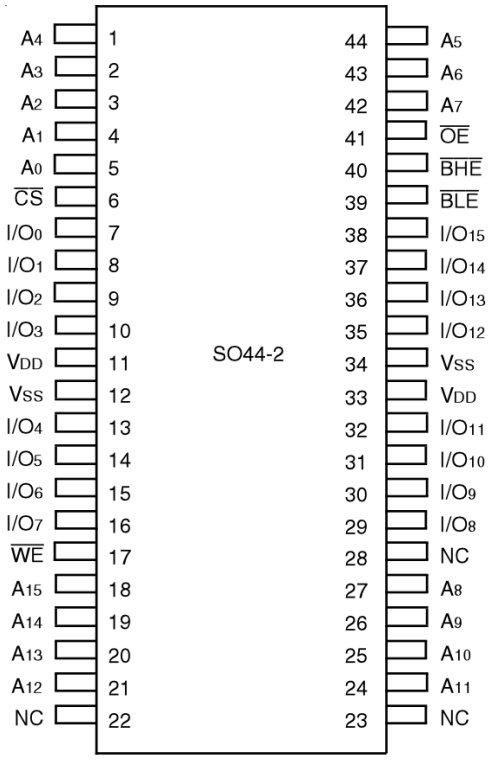
The IDT71T016 is packaged in a JEDEC standard 44-pin TSOP Type II.

## Functional Block Diagram




MAY 2009

## Pin Configurations




5326 drw 02

**TSOP**
**Top View**

## Pin Description

| | | |
|---|---|---|
| $A_0 - A_{15}$ | Address Inputs | Input |
| $\overline{CS}$ | Chip Select | Input |
| $\overline{WE}$ | Write Enable | Input |
| $\overline{OE}$ | Output Enable | Input |
| $\overline{BHE}$ | High Byte Enable | Input |
| $\overline{BLE}$ | Low Byte Enable | Input |
| $I/O_0 - I/O_{15}$ | Data Input/Output | I/O |
| $V_{DD}$ | 2.5V Power | Power |
| $V_{SS}$ | Ground | Gnd |

5326 tbl 01

## Truth Table(1)

| $\overline{CS}$ | $\overline{OE}$ | $\overline{WE}$ | $\overline{BLE}$ | $\overline{BHE}$ | $I/O_0$-$I/O_7$ | $I/O_8$-$I/O_{15}$ | Function |
|---|---|---|---|---|---|---|---|
| H | X | X | X | X | High-Z | High-Z | Deselected – Standby |
| L | L | H | L | H | $DATA_{OUT}$ | High-Z | Low Byte Read |
| L | L | H | H | L | High-Z | $DATA_{OUT}$ | High Byte Read |
| L | L | H | L | L | $DATA_{OUT}$ | $DATA_{OUT}$ | Word Read |
| L | X | L | L | L | $DATA_{IN}$ | $DATA_{IN}$ | Word Write |
| L | X | L | L | H | $DATA_{IN}$ | High-Z | Low Byte Write |
| L | X | L | H | L | High-Z | $DATA_{IN}$ | High Byte Write |
| L | H | H | X | X | High-Z | High-Z | Outputs Disabled |
| L | X | X | H | H | High-Z | High-Z | Outputs Disabled |

5326 tbl 02

**NOTE:**
1. H = $V_{IH}$, L = $V_{IL}$, X = Don't care.

## Absolute Maximum Ratings(1)

| Symbol | Rating | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage Relative to $V_{SS}$ | –0.3 to +3.6 | V |
| $V_{IN}$, $V_{OUT}$ | Terminal Voltage Relative to $V_{SS}$ | –0.3 to $V_{DD}$+0.3 | V |
| $T_{BIAS}$ | Temperature Under Bias | –55 to +125 | °C |
| $T_{STG}$ | Storage Temperature | –55 to +125 | °C |
| $P_T$ | Power Dissipation | 1.25 | W |
| $I_{OUT}$ | DC Output Current | 50 | mA |

5326 tbl 03

**NOTE:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Capacitance

**($T_A$ = +25°C, f = 1.0MHz)**

| Symbol | Parameter(1) | Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 3dV | 6 | pF |
| $C_{I/O}$ | I/O Capacitance | $V_{OUT}$ = 3dV | 7 | pF |

5326 tbl 06

**NOTE:**
1. This parameter is guaranteed by device characterization, but not production tested.

## Recommended Operating Temperature and Supply Voltage

| Grade | Temperature | Vss | $V_{DD}$ |
|---|---|---|---|
| Commercial | 0°C to +70°C | 0V | See Below |
| Industrial | -40°C to +85°C | 0V | See Below |

5326 tbl 04

## Recommended DC Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 2.375 | 2.5 | 2.625 | V |
| Vss | Ground | 0 | 0 | 0 | V |
| $V_{IH}$ | Input High Voltage | 1.7 | — | $V_{DD}$+0.3(1) | V |
| $V_{IL}$ | Input Low Voltage | –0.3(2) | — | 0.7 | V |

5326 tbl 05

**NOTES:**
1. $V_{IH}$ (max) = $V_{DD}$ + 1.0V a.c. (pulse width less than $t_{CYC}$/2) for I ≤ 20 mA, once per cycle.
2. $V_{IL}$ (min) = -1.0V a.c. (pulse width less than $t_{CYC}$/2) for I ≤ 20 mA, once per cycle.

## DC Electrical Characteristics

**($V_{DD}$ = Min. to Max., Commercial and Industrial Temperature Ranges)**

| Symbol | Parameter | Test Condition | IDT71T016SA | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| $\|I_{LI}\|$ | Input Leakage Current | $V_{DD}$ = Max., $V_{IN}$ = $V_{SS}$ to $V_{DD}$ | — | 5 | µA |
| $\|I_{LO}\|$ | Output Leakage Current | $V_{DD}$ = Max., $\overline{CS}$ = $V_{IH}$, $V_{OUT}$ = $V_{SS}$ to $V_{DD}$ | — | 5 | µA |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.0mA, $V_{DD}$ = Min. | — | 0.7 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = 2.0mA, $V_{DD}$ = Min. | 1.7 | — | V |

5326 tbl 07

## DC Electrical Characteristics(1,2)

**($V_{DD}$ = Min. to Max., $V_{LC}$ = 0.2V, $V_{HC}$ = $V_{DD}$ – 0.2V)**

| Symbol | Parameter | | 71T016SA12 | | 71T016SA15 | | 71T016SA20 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Com'l | Ind | Com'l | Ind | Com'l | Ind | |
| $I_{CC}$ | Dynamic Operating Current $\overline{CS}$ ≤ $V_{LC}$, Outputs Open, $V_{DD}$ = Max., f = $f_{MAX}$(3) | Max. | 150 | 160 | 130 | 130 | 120 | 120 | mA |
| | | Typ.(4) | 85 | — | 80 | — | 80 | — | |
| $I_{SB}$ | Dynamic Standby Power Supply Current $\overline{CS}$ ≥ $V_{HC}$, Outputs Open, $V_{DD}$ = Max., f = $f_{MAX}$(3) | | 40 | 45 | 35 | 35 | 30 | 30 | mA |
| $I_{SB1}$ | Full Standby Power Supply Current (static) $\overline{CS}$ ≥ $V_{HC}$, Outputs Open, $V_{DD}$ = Max., f = 0(3) | | 15 | 15 | 15 | 15 | 15 | 15 | mA |

5326 tbl 8

**NOTES:**
1. All values are maximum guaranteed values.
2. All inputs switch between 0.2V (Low) and $V_{DD}$ – 0.2V (High).
3. $f_{MAX}$ = 1/$t_{RC}$ (all address inputs are cycling at $f_{MAX}$); f = 0 means no address input lines are changing .
4. Typical values are measured at 2.5V, 25°C and with equal read and write cycles. This parameter is guaranteed by device characterization but is not production tested.

## AC Test Conditions

| | |
|---|---|
| Input Pulse Levels | 0V to 2.5V |
| Input Rise/Fall Times | 1.5ns |
| Input Timing Reference Levels | ($V_{DD}$/2) |
| Output Reference Levels | ($V_{DD}$/2) |
| AC Test Load | See Figure 1, 2 and 3 |

5326 tbl 09

## AC Test Loads

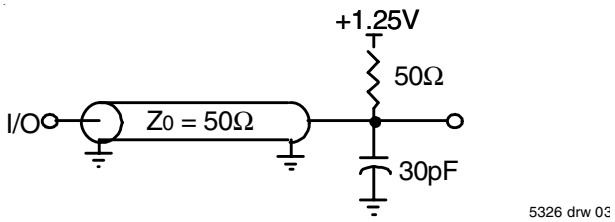
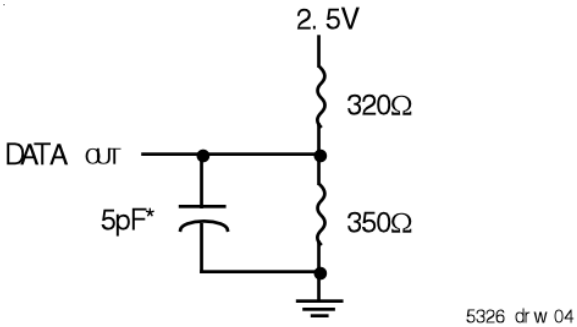



**Figure 1. AC Test Load**




*Including jig and scope capacitance.

**Figure 2. AC Test Load**
**(for $t_{CLZ}$, $t_{OLZ}$, $t_{CHZ}$, $t_{OHZ}$, $t_{OW}$, and $t_{WHZ}$)**

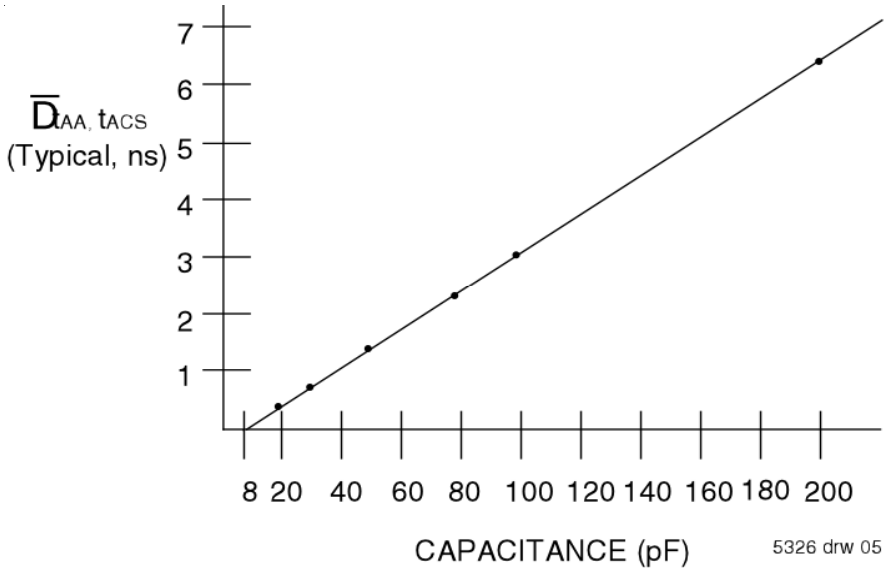



**Figure 3. Output Capacitive Derating**

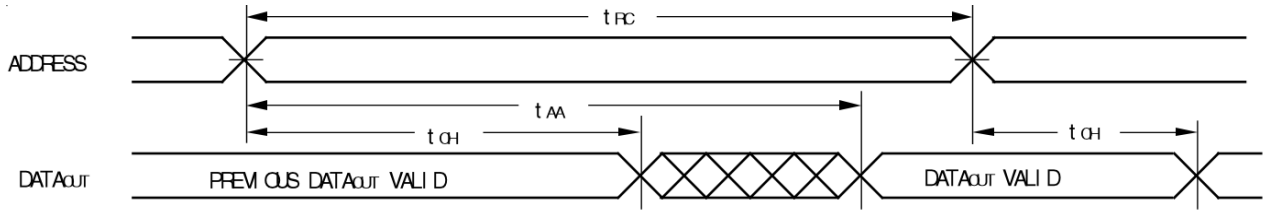
## AC Electrical Characteristics ($V_{DD}$ = Min. to Max., Commercial and Industrial Temperature Ranges)

| Symbol | Parameter | 71T016SA12 | | 71T016SA15 | | 71T016SA20 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **READ CYCLE** | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | 12 | — | 15 | — | 20 | — | ns |
| $t_{AA}$ | Address Access Time | — | 12 | — | 15 | — | 20 | ns |
| $t_{ACS}$ | Chip Select Access Time | — | 12 | — | 15 | — | 20 | ns |
| $t_{CLZ}$(1) | Chip Select Low to Output in Low-Z | 4 | — | 5 | — | 5 | — | ns |
| $t_{CHZ}$(1) | Chip Select High to Output in High-Z | — | 6 | — | 6 | — | 8 | ns |
| $t_{OE}$ | Output Enable Low to Output Valid | — | 6 | — | 7 | — | 8 | ns |
| $t_{OLZ}$(1) | Output Enable Low to Output in Low-Z | 0 | — | 0 | — | 0 | — | ns |
| $t_{OHZ}$(1) | Output Enable High to Output in High-Z | — | 6 | — | 6 | — | 8 | ns |
| $t_{OH}$ | Output Hold from Address Change | 4 | — | 4 | — | 4 | — | ns |
| $t_{BE}$ | Byte Enable Low to Output Valid | — | 6 | — | 7 | — | 8 | ns |
| $t_{BLZ}$(1) | Byte Enable Low to Output in Low-Z | 0 | — | 0 | — | 0 | — | ns |
| $t_{BHZ}$(1) | Byte Enable High to Output in High-Z | — | 6 | — | 6 | — | 8 | ns |
| **WRITE CYCLE** | | | | | | | | |
| $t_{WC}$ | Write Cycle Time | 12 | — | 15 | — | 20 | — | ns |
| $t_{AW}$ | Address Valid to End of Write | 8 | — | 10 | — | 12 | — | ns |
| $t_{CW}$ | Chip Select Low to End of Write | 8 | — | 10 | — | 12 | — | ns |
| $t_{BW}$ | Byte Enable Low to End of Write | 8 | — | 10 | — | 12 | — | ns |
| $t_{AS}$ | Address Set-up Time | 0 | — | 0 | — | 0 | — | ns |
| $t_{WR}$ | Address Hold from End of Write | 0 | — | 0 | — | 0 | — | ns |
| $t_{WP}$ | Write Pulse Width | 8 | — | 10 | — | 12 | — | ns |
| $t_{DW}$ | Data Valid to End of Write | 6 | — | 7 | — | 9 | — | ns |
| $t_{DH}$ | Data Hold Time | 0 | — | 0 | — | 0 | — | ns |
| $t_{OW}$(1) | Write Enable High to Output in Low-Z | 3 | — | 3 | — | 3 | — | ns |
| $t_{WHZ}$(1) | Write Enable Low to Output in High-Z | — | 6 | — | 6 | — | 8 | ns |

**NOTE:**
1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

5326 tbl 10

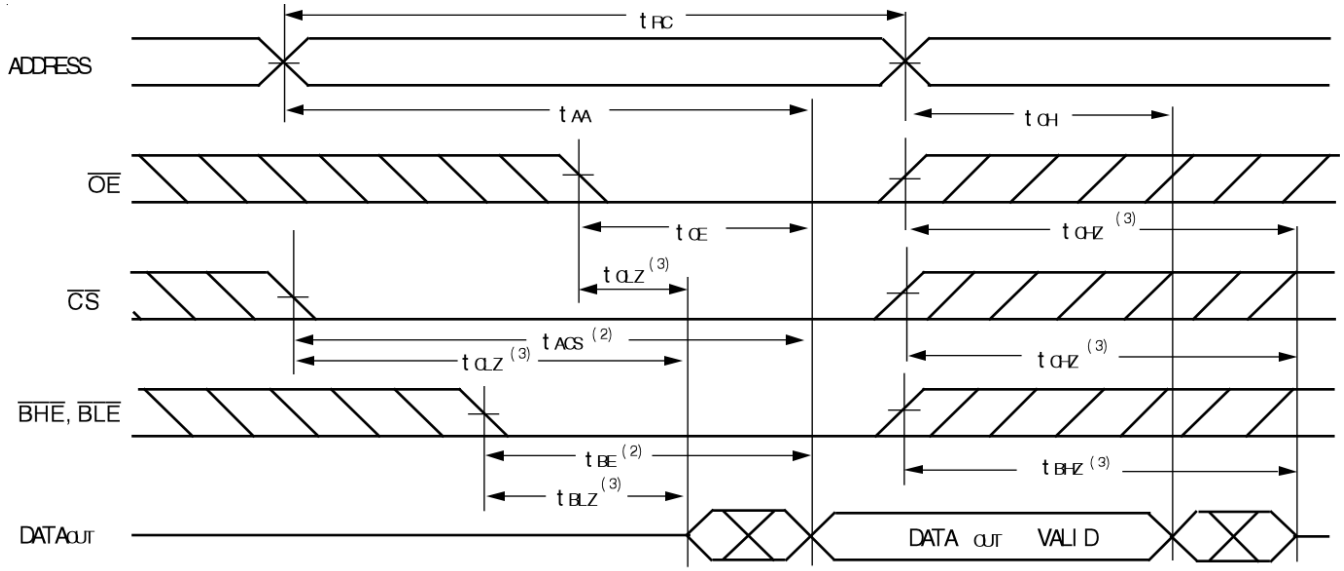
## Timing Waveform of Read Cycle No. 1(1,2,3)




**NOTES:**
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. $\overline{OE}$, $\overline{BHE}$, and $\overline{BLE}$ are LOW.

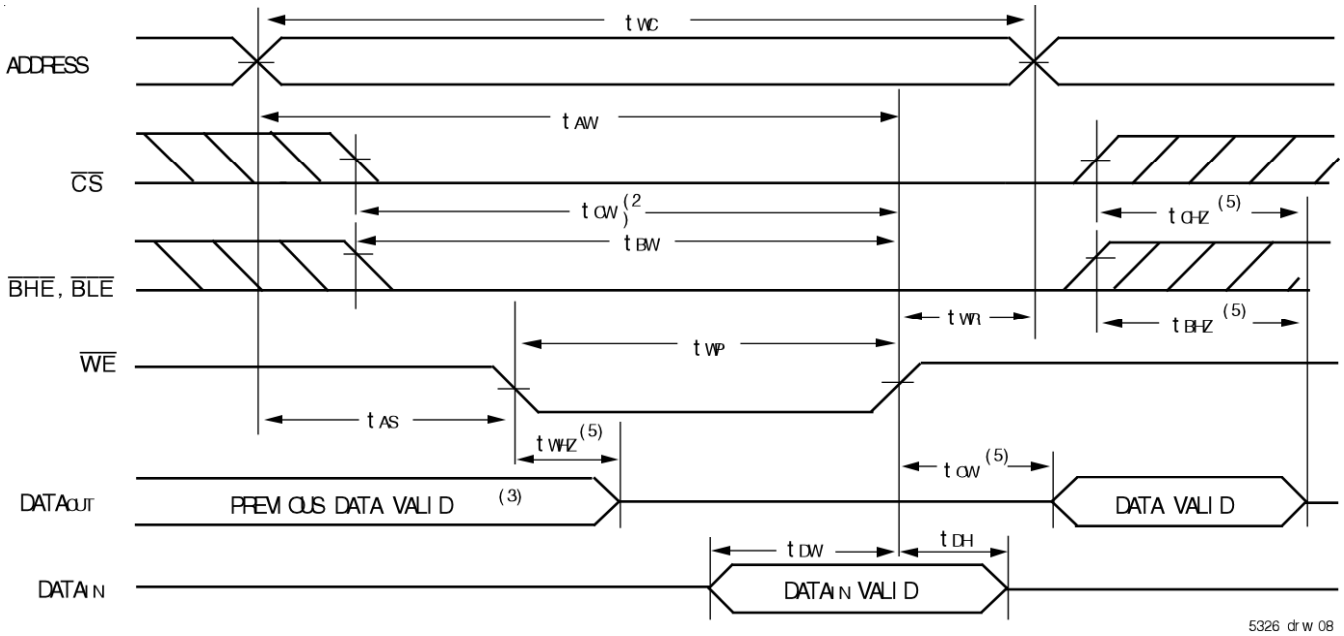
5326 drw 06

## Timing Waveform of Read Cycle No. 2(1)



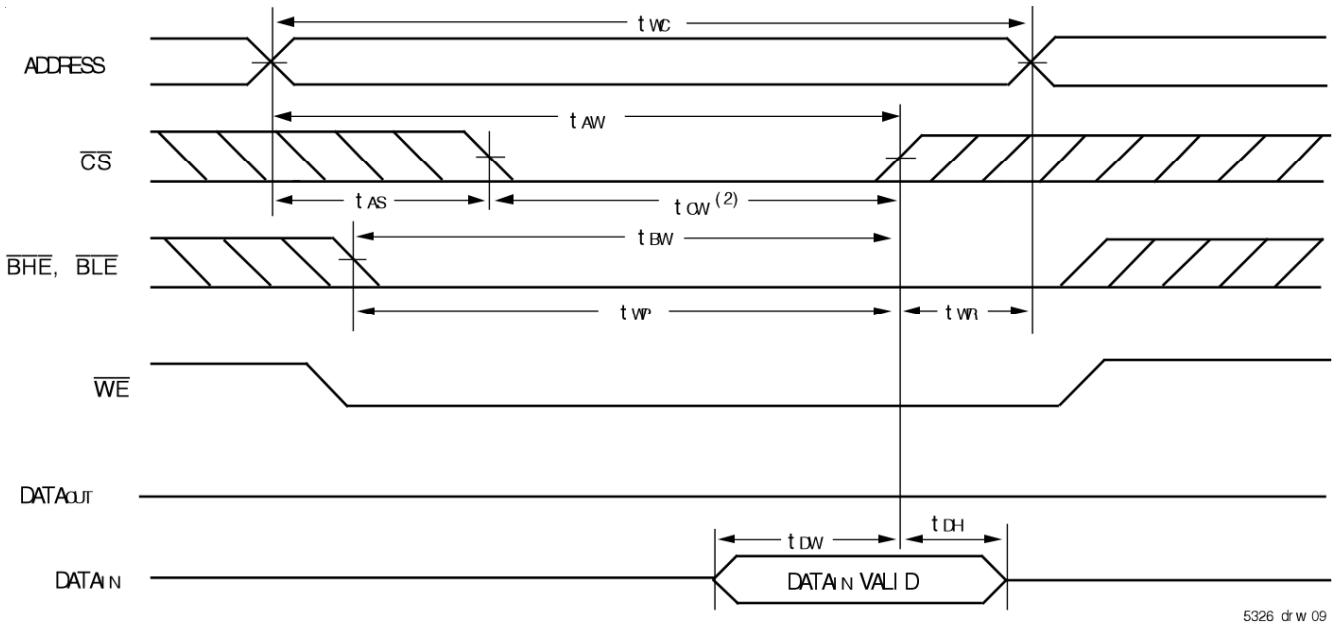

**NOTES:**
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Address must be valid prior to or coincident with the later of $\overline{CS}$, $\overline{BHE}$, or $\overline{BLE}$ transition LOW; otherwise $t_{AA}$ is the limiting parameter.
3. Transition is measured ±200mV from steady state.

## Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled Timing)(1,2,4)

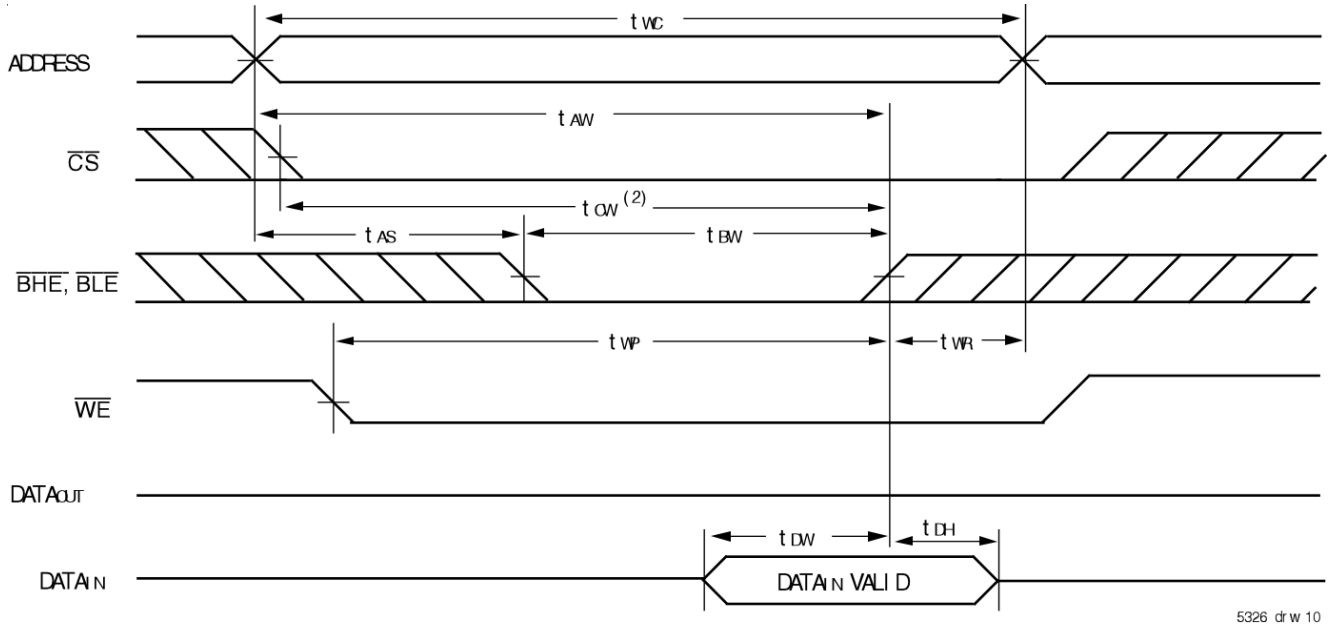



**NOTES:**
1. A write occurs during the overlap of a LOW $\overline{CS}$, LOW $\overline{BHE}$ or $\overline{BLE}$, and a LOW $\overline{WE}$.
2. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, $t_{WP}$ must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required $t_{DW}$. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified $t_{WP}$.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the $\overline{CS}$ LOW or $\overline{BHE}$ and $\overline{BLE}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
5. Transition is measured ±200mV from steady state.

## Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled Timing)(1,4)



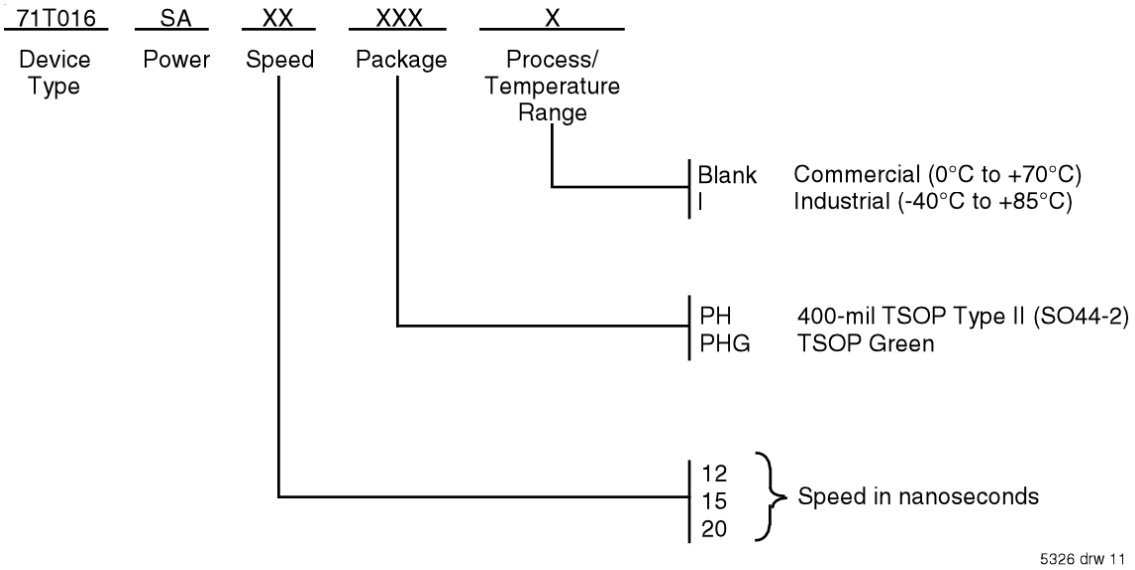

## Timing Waveform of Write Cycle No. 3 ($\overline{BHE}$, $\overline{BLE}$ Controlled Timing)(1,4)




**NOTES:**

1. A write occurs during the overlap of a LOW $\overline{CS}$, LOW $\overline{BHE}$ or $\overline{BLE}$, and a LOW $\overline{WE}$.
2. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, $t_{WP}$ must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required $t_{DW}$. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified $t_{WP}$.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the $\overline{CS}$ LOW or $\overline{BHE}$ and $\overline{BLE}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
5. Transition is measured ±200mV from steady state.

# Ordering Information



# Datasheet Document History

| Rev | Date | Page | Description |
|---|---|---|---|
| 0 | 08/23/01 | | Created new datasheet |
| 1 | 04/16/04 | p. 1-8 | Updated datasheet to full release version. |
| | | p. 3 | Updated overshoot and undershoot specifications and typical DC electrical characteristics. |
| 2 | 07/14/08 | p. 1,2,6,7 | Corrected pin labels output enable, chip select, write enable, high and low byte enables to be $\overline{OE}$, $\overline{CS}$, $\overline{WE}$, $\overline{BHE}$, $\overline{BLE}$ to reflect active low nature. |
| 3 | 05/12/09 | p. 1-3,5,8 | Deleted Y, BF packages, 10ns speed and Added PHG package. Updated the ordering information by removing the "IDT" notation. |

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