

## 200 mA LOAD SWITCH FEATURING PRE-BIASED PNP TRANSISTOR AND N-MOSFET WITH GATE PULL DOWN RESISTOR

### General Description

LMN200B02 is best suited for applications where the load needs to be turned on and off using control circuits like micro-controllers, comparators etc. particularly at a point of load. It features a discrete pass transistor with stable  $V_{CE(SAT)}$  which does not depend on the input voltage and can support continuous maximum current of 200 mA. It also contains a discrete N-MOSFET that can be used as control. This N-MOSFET also has a built-in pull down resistor at its gate. The component can be used as a part of a circuit or as a stand alone discrete device.

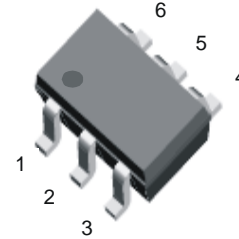


Fig. 1: SOT-363

### Features

- Voltage Controlled Small Signal Switch
- N-MOSFET with Gate Pull-Down Resistor
- Surface Mount Package
- Ideally Suited for Automated Assembly Processes
- **Lead Free By Design/RoHS Compliant (Note 1)**
- **"Green" Device (Note 2)**

### Mechanical Data

- Case: SOT-363
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish - Matte Tin annealed over Alloy 42 leadframe. Solderable per MIL-STD-202, Method 208
- Marking Information: See Page 8
- Ordering Information: See Page 8
- Weight: 0.006 grams (approximate)

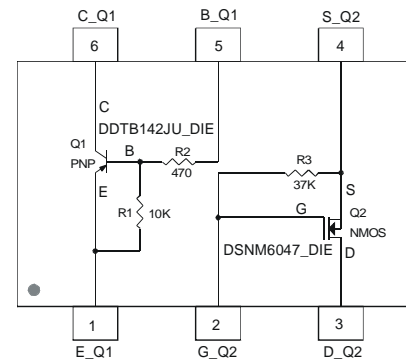


Fig. 2 Schematic and Pin Configuration

Sub-Component P/N	Reference	Device Type	R1 (NOM)	R2 (NOM)	R3 (NOM)	Figure
DDTB142JU_DIE	Q1	PNP Transistor	10K	470	—	2
DSNM6047_DIE (with Gate Pull-Down Resistor)	Q2	N-MOSFET	—	—	37K	2

### Maximum Ratings, Total Device @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 3)	$P_D$	200	mW
Power Derating Factor above $125^\circ\text{C}$	$P_{der}$	1.6	mW/ $^\circ\text{C}$
Output Current	$I_{out}$	200	mA

### Thermal Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Value	Unit
Operating and Storage Temperature Range	$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$
Thermal Resistance, Junction to Ambient Air (Equivalent to One Heated Junction of PNP Transistor) (Note 3)	$R_{\theta JA}$	625	$^\circ\text{C}/\text{W}$

- Notes:
1. No purposefully added lead.
  2. Diodes Inc.'s "Green" policy can be found on our website at [http://www.diodes.com/products/lead\\_free/index.php](http://www.diodes.com/products/lead_free/index.php).
  3. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch; pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at <http://www.diodes.com/datasheets/ap02001.pdf>.

### Maximum Ratings:

#### Sub-Component Device: Pre-Biased PNP Transistor (Q1)

@T<sub>A</sub> = 25°C unless otherwise specified

Characteristic	Symbol	Value	Unit
Collector-Base Voltage	V <sub>CB0</sub>	-50	V
Collector-Emitter Voltage	V <sub>CEO</sub>	-50	V
Supply Voltage	V <sub>CC</sub>	-50	V
Input Voltage	V <sub>in</sub>	+5 to -6	V
Output Current	I <sub>C</sub>	-200	mA

#### Sub-Component Device: N-MOSFET With Gate Pull-Down Resistor (Q2)

@T<sub>A</sub> = 25°C unless otherwise specified

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V <sub>DSS</sub>	60	V
Drain Gate Voltage (R <sub>GS</sub> ≤ 1M Ohm)	V <sub>DGR</sub>	60	V
Gate-Source Voltage	V <sub>GSS</sub>	Continuous	V
		Pulsed (tp < 50 uS)	
Drain Current (Page 1: Note 3)	I <sub>D</sub>	Continuous (V <sub>gs</sub> = 10V)	115
		Pulsed (tp < 10 uS, Duty Cycle < 1%)	800
Continuous Source Current	I <sub>S</sub>	115	mA

**Electrical Characteristics: Pre-Biased PNP Transistor (Q1)**

 @T<sub>A</sub> = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS</b>						
Collector-Base Cut Off Current	I <sub>CB0</sub>	—	—	-100	nA	V <sub>CB</sub> = -50V, I <sub>E</sub> = 0
Collector-Emitter Cut Off Current	I <sub>CEO</sub>	—	—	-500	nA	V <sub>CE</sub> = -50V, I <sub>B</sub> = 0
Emitter-Base Cut Off Current	I <sub>EB0</sub>	—	-0.5	-1	mA	V <sub>EB</sub> = -5V, I <sub>C</sub> = 0
Collector-Base Breakdown Voltage	V <sub>(BR)CBO</sub>	-50	—	—	V	I <sub>C</sub> = -10 uA, I <sub>E</sub> = 0
Collector-Emitter Breakdown Voltage	V <sub>(BR)CEO</sub>	-50	—	—	V	I <sub>C</sub> = -2 mA, I <sub>B</sub> = 0
Input Off Voltage	V <sub>I(OFF)</sub>	—	-0.55	-0.3	V	V <sub>CE</sub> = -5V, I <sub>C</sub> = -100uA
Output Voltage	V <sub>OH</sub>	-4.9	—	—	V	V <sub>CC</sub> = -5V, V <sub>B</sub> = -0.05V, R <sub>L</sub> = 1K
Output Current (leakage current same as I <sub>CEO</sub> )	I <sub>O(OFF)</sub>	—	—	-500	nA	V <sub>CC</sub> = -50V, V <sub>I</sub> = 0V
<b>ON CHARACTERISTICS</b>						
Collector-Emitter Saturation Voltage	V <sub>CE(SAT)</sub>	—	—	-0.15	V	I <sub>C</sub> = -10 mA, I <sub>B</sub> = -0.5 mA
		—	—	-0.2	V	I <sub>C</sub> = -50mA, I <sub>B</sub> = -5mA
		—	—	-0.2	V	I <sub>C</sub> = -20mA, I <sub>B</sub> = -1mA
		—	—	-0.25	V	I <sub>C</sub> = -100mA, I <sub>B</sub> = -10mA
		—	—	-0.25	V	I <sub>C</sub> = -200mA, I <sub>B</sub> = -10mA
		—	—	-0.3	V	I <sub>C</sub> = -200mA, I <sub>B</sub> = -20mA
Equivalent On-Resistance*	R <sub>CE(SAT)</sub>	—	—	1.5	Ω	I <sub>C</sub> = -200mA, I <sub>B</sub> = -10mA
DC Current Gain	h <sub>FE</sub>	60	150	—	—	V <sub>CE</sub> = -5V, I <sub>C</sub> = -20 mA
		60	215	—	—	V <sub>CE</sub> = -5V, I <sub>C</sub> = -50 mA
		60	245	—	—	V <sub>CE</sub> = -5V, I <sub>C</sub> = -100 mA
		60	250	—	—	V <sub>CE</sub> = -5V, I <sub>C</sub> = -200 mA
Input On Voltage	V <sub>I(ON)</sub>	-2.45	-0.7	—	V	V <sub>O</sub> = -0.3V, I <sub>C</sub> = -2 mA
Output Voltage (equivalent to V <sub>CE(SAT)</sub> or V <sub>O(ON)</sub> )	V <sub>OL</sub>	—	-0.065	-0.15	V	V <sub>CC</sub> = -5V, V <sub>B</sub> = -2.5V, I <sub>O</sub> /I <sub>I</sub> = -50mA / -2.5mA
Input Current	I <sub>i</sub>	—	-9	-28	mA	V <sub>I</sub> = -5V
Base-Emitter Turn-on Voltage	V <sub>BE(ON)</sub>	—	-1.13	-1.3	V	V <sub>CE</sub> = -5V, I <sub>C</sub> = 200mA
Base-Emitter Saturation Voltage	V <sub>BE(SAT)</sub>	—	-3.2	-3.6	V	I <sub>C</sub> = -50mA, I <sub>B</sub> = -5mA
		—	-4.6	-5.5		I <sub>C</sub> = -80mA, I <sub>B</sub> = -8mA
Input Resistor (Base), +/- 30%	R <sub>2</sub>	—	0.47	—	KΩ	—
Pull-up Resistor (Base to V <sub>CC</sub> supply), +/- 30%	R <sub>1</sub>	—	10	—	KΩ	—
Resistor Ratio (Input Resistor/Pull-up resistor) +/- 20%	R <sub>1</sub> /R <sub>2</sub>	—	21	—	—	—
<b>SMALL SIGNAL CHARACTERISTICS</b>						
Transition Frequency (Gain Bandwidth Product)	f <sub>T</sub>	—	200	—	MHz	V <sub>CE</sub> = -10V, I <sub>E</sub> = -5mA, f = 100MHz
Collector Capacitance, (C <sub>cb0</sub> -Output Capacitance)	C <sub>C</sub>	—	20	—	pF	V <sub>CB</sub> = -10V, I <sub>E</sub> = 0A, f = 1MHz

\* Pulse Test: Pulse width, tp &lt; 300 μs, Duty Cycle, d &lt;= 0.02

## Electrical Characteristics: N-MOSFET with Gate Pull-Down Resistor (Q2)

@T<sub>A</sub> = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 4)</b>						
Drain-Source Breakdown Voltage, BV <sub>DSS</sub>	V <sub>(BR)DSS</sub>	60	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 10μA
Zero Gate Voltage Drain Current (Drain Leakage Current)	I <sub>DSS</sub>	—	—	1	μA	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 60V
Gate-Body Leakage Current, Forward	I <sub>GSSF</sub>	—	—	0.95	mA	V <sub>GS</sub> = 20V, V <sub>DS</sub> = 0V
Gate-Body Leakage Current, Reverse	I <sub>GSSR</sub>	—	—	-0.95	mA	V <sub>GS</sub> = -20V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 4)</b>						
Gate Source Threshold Voltage (Control Supply Voltage)	V <sub>GS(th)</sub>	1	1.9	2.2	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 0.25mA
Static Drain-Source On-State Voltage	V <sub>DS(on)</sub>	—	0.10	1.5	V	V <sub>GS</sub> = 5V, I <sub>D</sub> = 50mA
		—	0.15	3.75		V <sub>GS</sub> = 10V, I <sub>D</sub> = 115mA
On-State Drain Current	I <sub>D(on)</sub>	500	—	—	mA	V <sub>GS</sub> = 10V, V <sub>DS</sub> ≥ 2xV <sub>DS(on)</sub>
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	—	1.6	3	Ω	V <sub>GS</sub> = 5V, I <sub>D</sub> = 50mA
		—	1.4	2		V <sub>GS</sub> = 10V, I <sub>D</sub> = 500mA
Forward Transconductance	g <sub>FS</sub>	80	240	—	mS	V <sub>DS</sub> ≥ 2xV <sub>DS(on)</sub> , I <sub>D</sub> = 115 mA
		80	350	—		V <sub>DS</sub> ≥ 2xV <sub>DS(on)</sub> , I <sub>D</sub> = 200 mA
Gate Pull-Down Resistor, +/- 30%	R3	—	37	—	KΩ	—
<b>DYNAMIC CHARACTERISTICS</b>						
Input Capacitance	C <sub>iss</sub>	—	—	50	pF	V <sub>DS</sub> = -25V, V <sub>GS</sub> = 0V, f = 1MHz
Output Capacitance	C <sub>oss</sub>	—	—	25	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>	—	—	5	pF	
<b>SWITCHING CHARACTERISTICS</b>						
Turn-On Delay Time	t <sub>D(on)</sub>	—	—	20	ns	V <sub>DD</sub> = 30V, V <sub>GS</sub> = 10V, I <sub>D</sub> = 200mA, R <sub>G</sub> = 25 Ohm, R <sub>L</sub> = 150 Ohm
Turn-Off Delay Time	t <sub>D(off)</sub>	—	—	40	ns	
<b>SOURCE-DRAIN (BODY) DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
Drain-Source Diode Forward On-Voltage	V <sub>SD</sub>	—	0.90	1.5	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 115 mA
Maximum Continuous Drain-Source Diode Forward Current (Reverse Drain Current)	I <sub>S</sub>	—	—	115	mA	—
Maximum Pulsed Drain-Source Diode Forward Current	I <sub>SM</sub>	—	—	800	mA	—

Notes: 4. Short duration pulse test used to minimize self-heating effect.

### Typical Characteristics

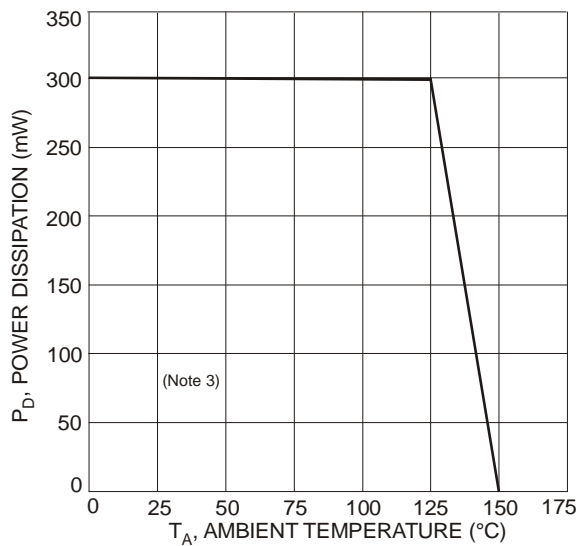


Fig. 3 Max Power Dissipation vs. Ambient Temperature (Total Device)

**Typical Pre-Biased PNP Transistor (Q1) Characteristics**

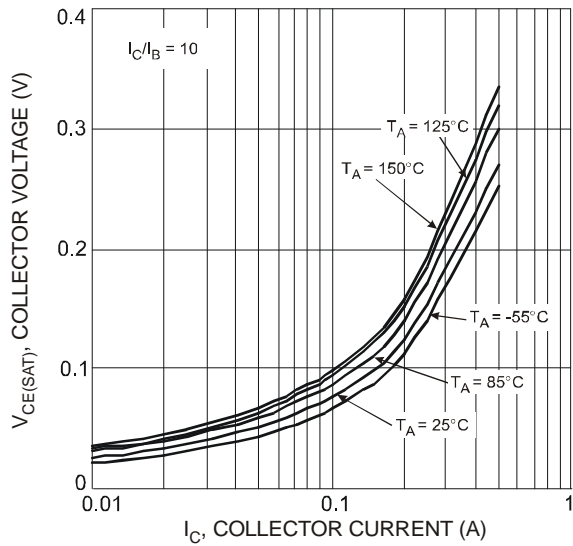


Fig. 4  $V_{CE(SAT)}$  vs.  $I_C$

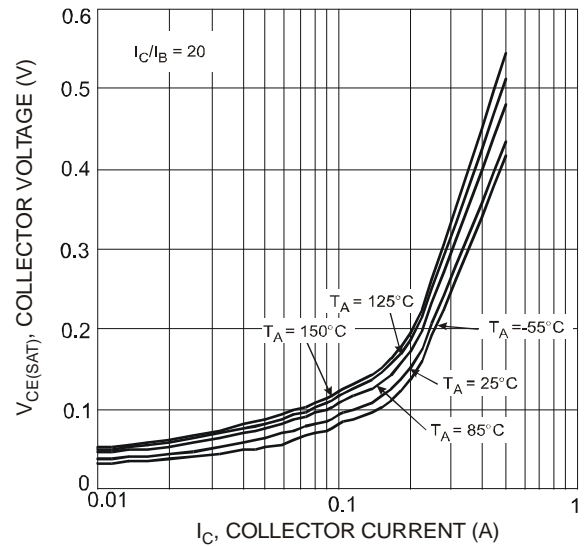


Fig. 5  $V_{CE(SAT)}$  vs.  $I_C$

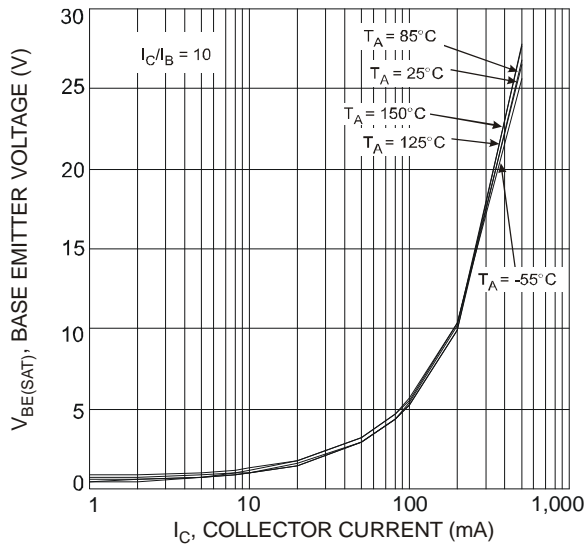


Fig. 6  $V_{BE(SAT)}$  vs.  $I_C$

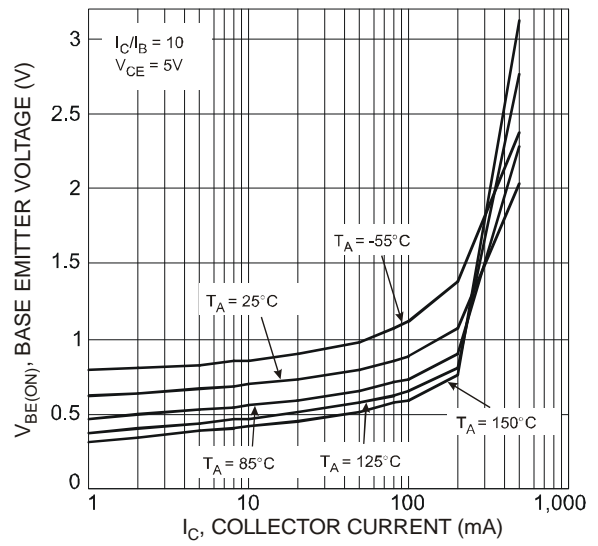


Fig. 7  $V_{BE(ON)}$  vs.  $I_C$

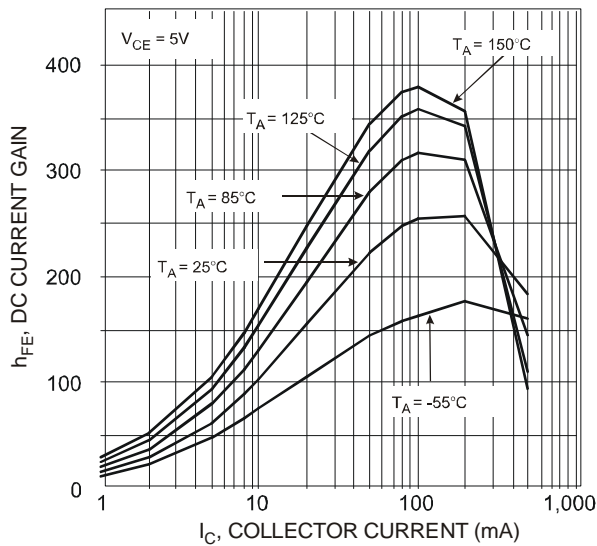


Fig. 8  $h_{FE}$  vs.  $I_C$

### Typical N-Channel MOSFET (Q2) Characteristics

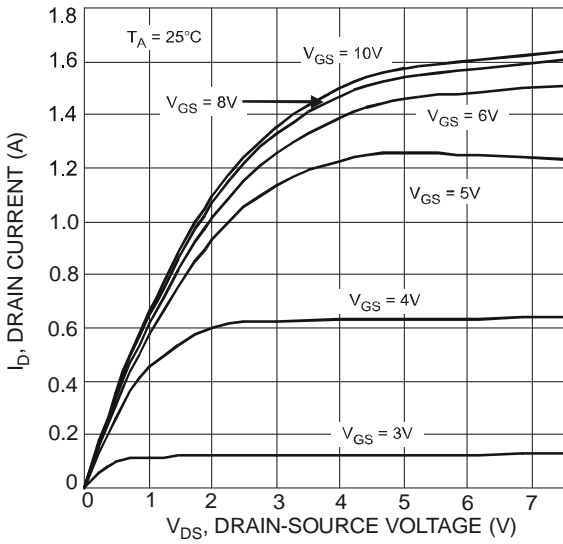


Fig. 9 Output Characteristics

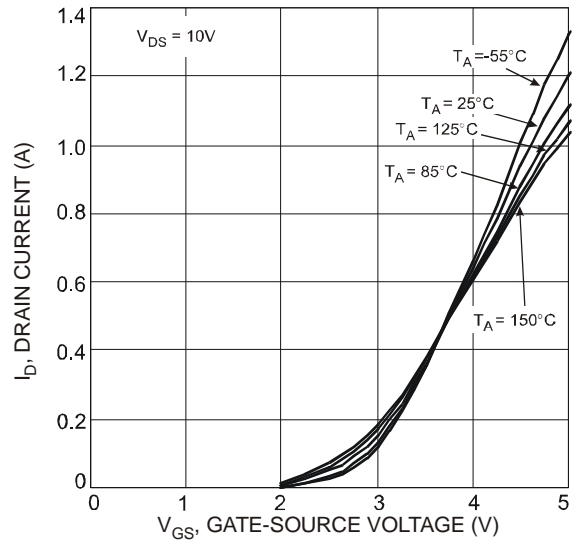


Fig. 10 Transfer Characteristics

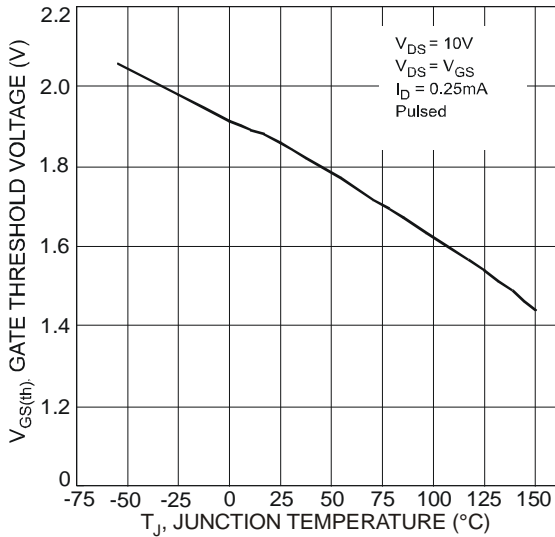


Fig. 11 Gate Threshold Voltage vs. Junction Temperature

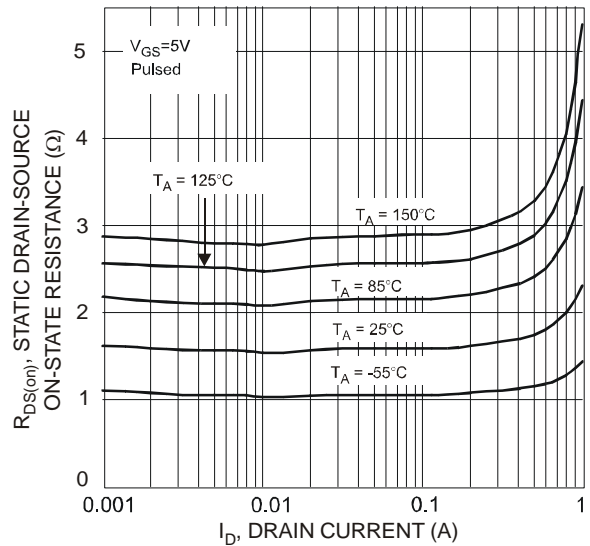


Fig. 12 Static Drain-Source On-Resistance vs. Drain Current

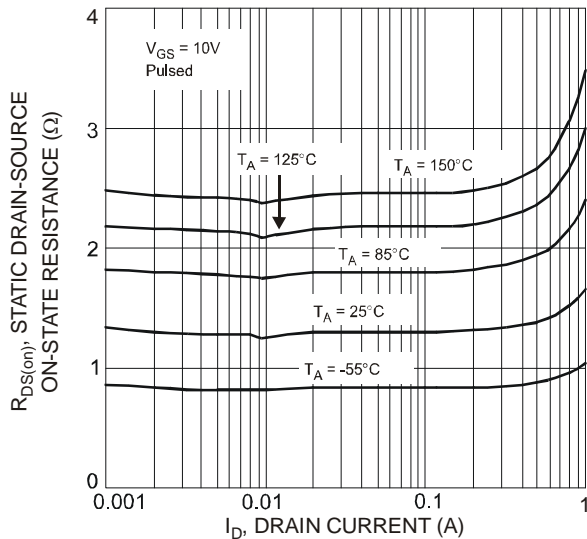


Fig. 13 Static Drain-Source On-Resistance vs. Drain Current

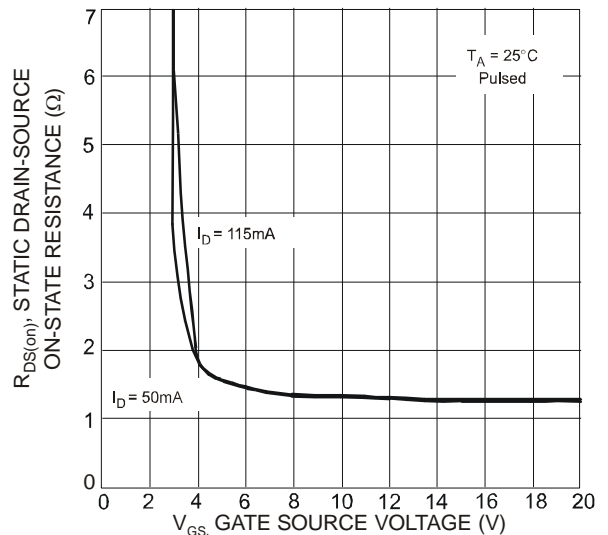


Fig. 14 Static Drain-Source On-Resistance vs. Gate-Source Voltage

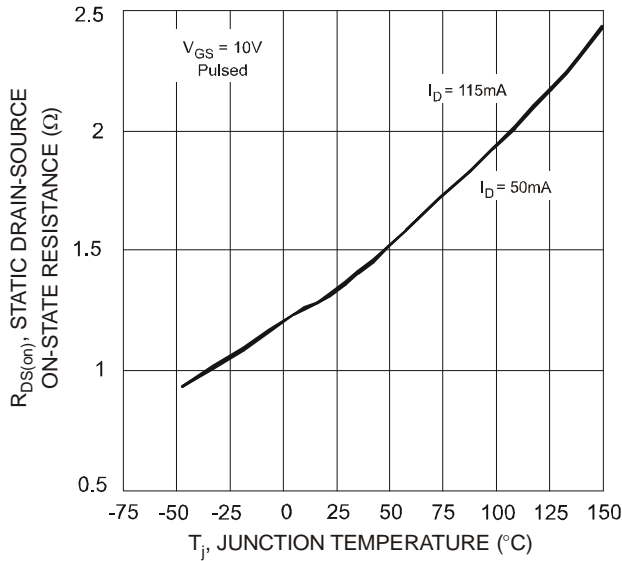


Fig. 15 Static Drain-Source On-State Resistance vs. Junction Temperature

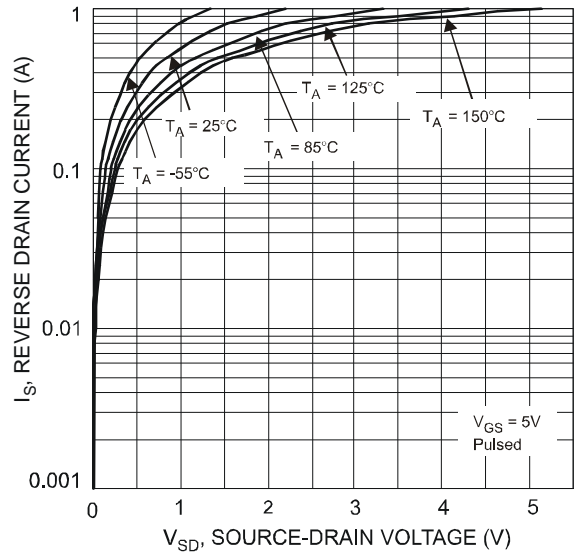


Fig. 16 Reverse Drain Current vs. Source-Drain Voltage

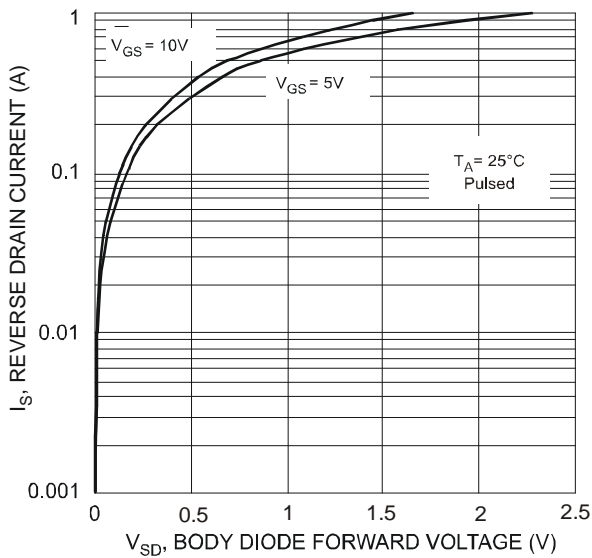


Fig. 17 Reverse Drain Current vs. Body Diode Forward Voltage

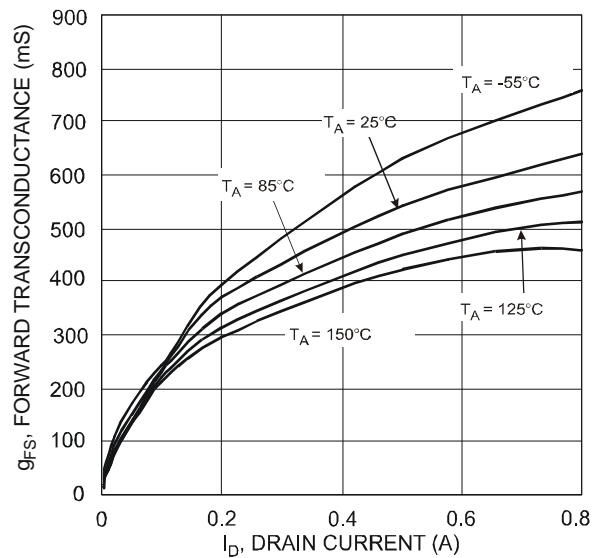


Fig. 18 Forward Transfer Conductance vs. Drain Current ( $V_{DS} > I_D R_{DS(ON)}$ )

## Application Details

PNP Transistor (DDTB142JU) and N-MOSFET (DSNM6047) with gate pull-down resistor integrated as one in LMN200B02 can be used as a discrete entity for general purpose applications or as an integrated circuit to function as a Load Switch. When it is used as the latter as shown in Fig 19, various input voltage sources can be used as long as it does not exceed the maximum ratings of the device. These devices are designed to deliver continuous output load current up to a maximum of 200 mA. The MOSFET Switch draws no current, hence loading of control circuit is prevented. Care must be taken for higher levels of dissipation while designing for higher load conditions. These devices provide high power and also consume less space. The product mainly helps in optimizing power usage, thereby conserving battery life in a controlled load system like portable battery powered applications. (Please see Fig. 20 for one example of a typical application circuit used in conjunction with voltage regulator as a part of a power management system)

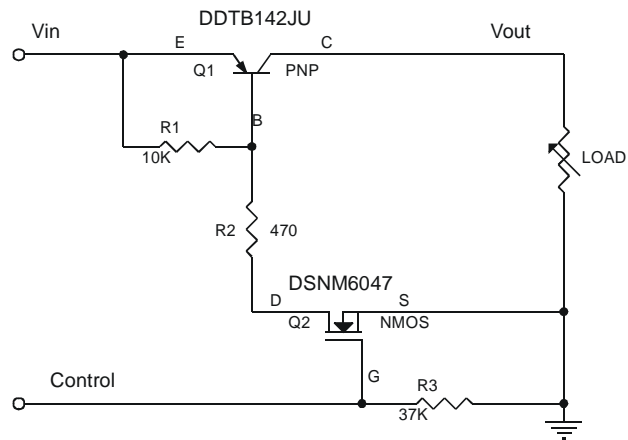


Fig. 19 Circuit Diagram

## Typical Application Circuit

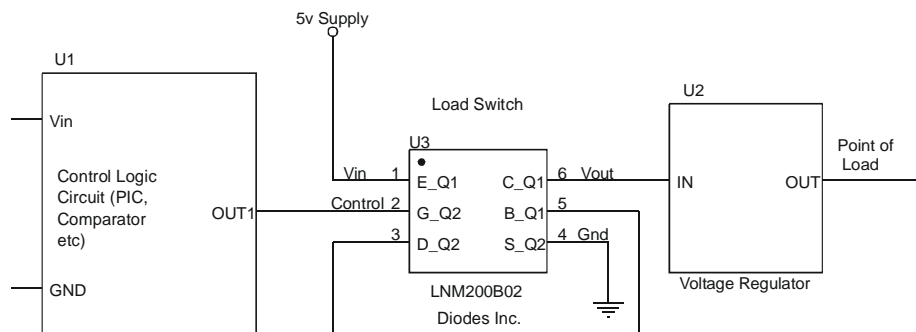


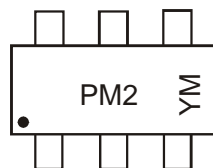
Fig. 20

## Ordering Information (Note 5)

Device	Packaging	Shipping
LMN200B02-7	SOT-363	3000/Tape & Reel

Notes: 5. For packaging details, go to our website at <http://www.diodes.com/datasheets/ap02007.pdf>.

## Marking Information



PM2 = Product Type Marking Code,  
 YM = Date Code Marking  
 Y = Year (ex: T = 2006)  
 M = Month (ex: 9 = September)

### Date Code Key

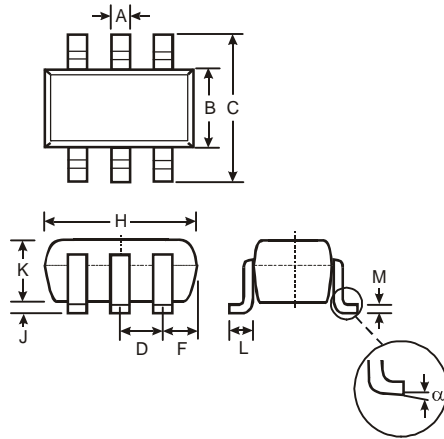
Year	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015
Code	T	U	V	W	X	Y	Z	A	B	C

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

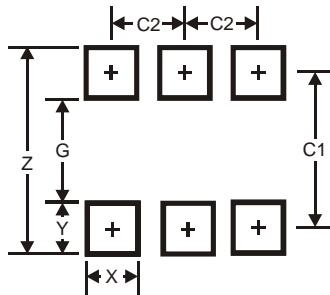


## Mechanical Details



SOT-363		
Dim	Min	Max
A	0.10	0.30
B	1.15	1.35
C	2.00	2.20
D	0.65 Typ	
F	0.40	0.45
H	1.80	2.20
J	0	0.10
K	0.90	1.00
L	0.25	0.40
M	0.10	0.22
$\alpha$	0°	8°
All Dimensions in mm		

## Suggested Pad Layout



Dimensions	Value (in mm)
Z	2.5
G	1.3
X	0.42
Y	0.6
C1	1.9
C2	0.65

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2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

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