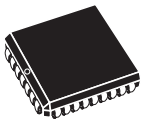
M50FLW040A
M50FLW040B

4-Mbit (5 × 64 Kbyte blocks + 3 × 16 × 4 Kbyte sectors)
3-V supply Firmware Hub / low-pin count Flash memory

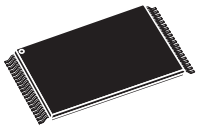
Feature summary

- Flash memory
  - Compatible with either the LPC interface or the FWH interface (Intel Spec rev1.1) used in PC BIOS applications
  - 5 Signal Communication Interface supporting Read and Write Operations
  - 5 Additional General Purpose Inputs for platform design flexibility
  - Synchronized with 33MHz PCI clock
- 8 blocks of 64 Kbytes
  - 5 blocks of 64 KBytes each
  - 3 blocks, subdivided into 16 uniform sectors of 4 KBytes each
    Two blocks at the top and one at the bottom (M50FLW040A)
    One block at the top and two at the bottom (M50FLW040B)
- Enhanced security
  - Hardware Write Protect Pins for Block Protection
  - Register-based Read and Write Protection
- Supply voltage
  - V_{CC} = 3 to 3.6V for Program, Erase and Read Operations
  - V_{PP} = 12V for Fast Program and Erase
- Two interfaces
  - Auto Detection of Firmware Hub (FWH) or Low Pin Count (LPC) Memory Cycles for Embedded Operation with PC Chipsets
  - Address/Address Multiplexed (A/A Mux) Interface for programming equipment compatibility.
- Programming time: 10 µs typical
- Program/Erase Controller
  - Embedded Program and Erase algorithms
  - Status Register Bits



PLCC32 (K)

TSOP32 (NB)
8 x 14mm



TSOP40 (N)
10 x 20mm

- Program/Erase Suspend
  - Read other Blocks/Sectors during Program Suspend
  - Program other Blocks/Sectors during Erase Suspend
- Electronic signature
  - Manufacturer Code: 20h
  - Device Code (M50FLW040A): 08h
  - Device Code (M50FLW040B): 28h
- Packages
  - ECOPACK® (RoHS compliant)

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1 Summary description

The M50FLW040 is a 4 Mbit (512 Kb x8) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (3.0 to 3.6V) supply. For fast programming and fast erasing in production lines, an optional 12 V power supply can be used to reduce the erasing and programming time.

The memory is divided into 8 Uniform Blocks of 64 KBytes each, three of which are divided into 16 uniform sectors of 4 KBytes each (see *Appendix A* for details). All blocks and sectors can be erased independently. So, it is possible to preserve valid data while old data is erased. Blocks can be protected individually to prevent accidental program or erase commands from modifying their contents.

Program and erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a program or erase operation can be detected and any error conditions identified. The command set to control the memory is consistent with the JEDEC standards.

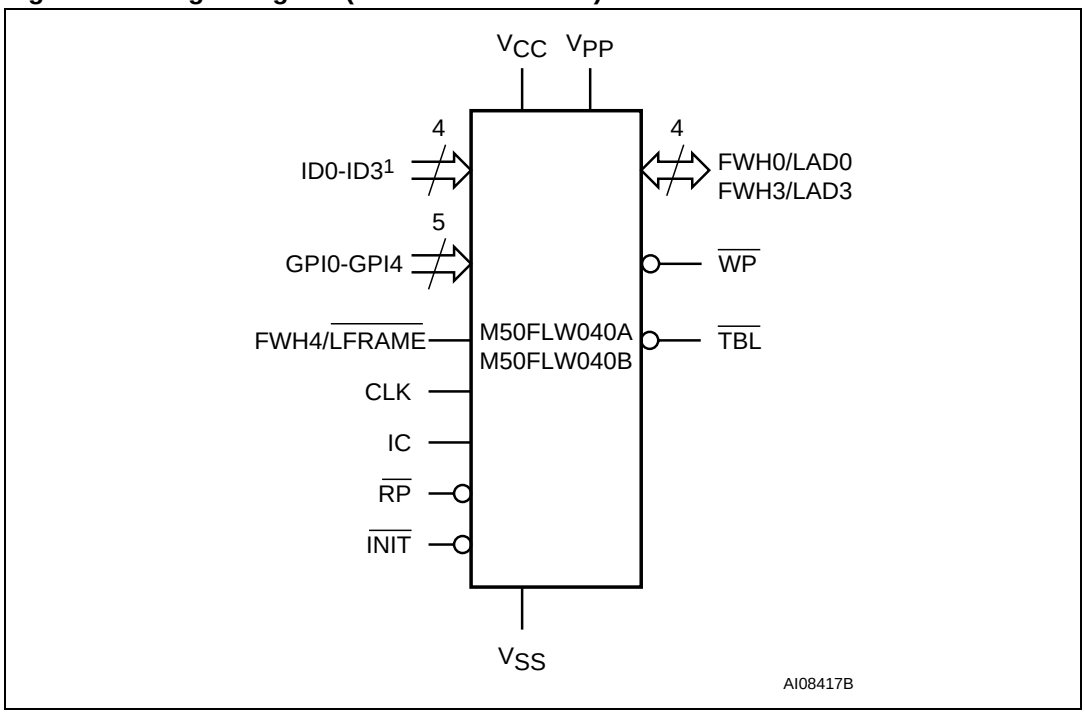
Two different bus interfaces are supported by the memory:

- The primary interface, the FWH/LPC Interface, uses Intel's proprietary Firmware Hub (FWH) and Low Pin Count (LPC) protocol. This has been designed to remove the need for the ISA bus in current PC Chipsets. The M50FLW040 acts as the PC BIOS on the Low Pin Count bus for these PC Chipsets.
- The secondary interface, the Address/Address Multiplexed (or A/A Mux) Interface, is designed to be compatible with current Flash Programmers, for production line programming prior to fitting the device in a PC Motherboard.

The memory is supplied with all the bits erased (set to '1').

In order to meet environmental requirements, ST offers the M50FLW040A and M50FLW040B in ECOPACK® packages. ECOPACK® packages are Lead-free and RoHS compliant. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*.

Figure 1. Logic diagram (FWH/LPC interface)



1. ID3 is Reserved for Future Use (RFU) in LPC mode.

Table 1. Signal names (FWH/LPC Interface)

FWH0/LAD0-FWH3/LAD3	Input/Output Communications
FWH4/$\overline{\text{LFRAME}}$	Input Communication Frame
ID0-ID3	Identification Inputs
GPI0-GPI4	General Purpose Inputs
IC	Interface Configuration
$\overline{\text{RP}}$	Interface Reset
$\overline{\text{INIT}}$	CPU Reset
CLK	Clock
$\overline{\text{TBL}}$	Top Block Lock
$\overline{\text{WP}}$	Write Protect
RFU	Reserved for Future Use. Leave disconnected
V_{CC}	Supply Voltage
V_{PP}	Optional Supply Voltage for Fast Program and Erase Operations
V_{SS}	Ground
NC	Not Connected Internally

Figure 2. Logic diagram (A/A Mux interface)

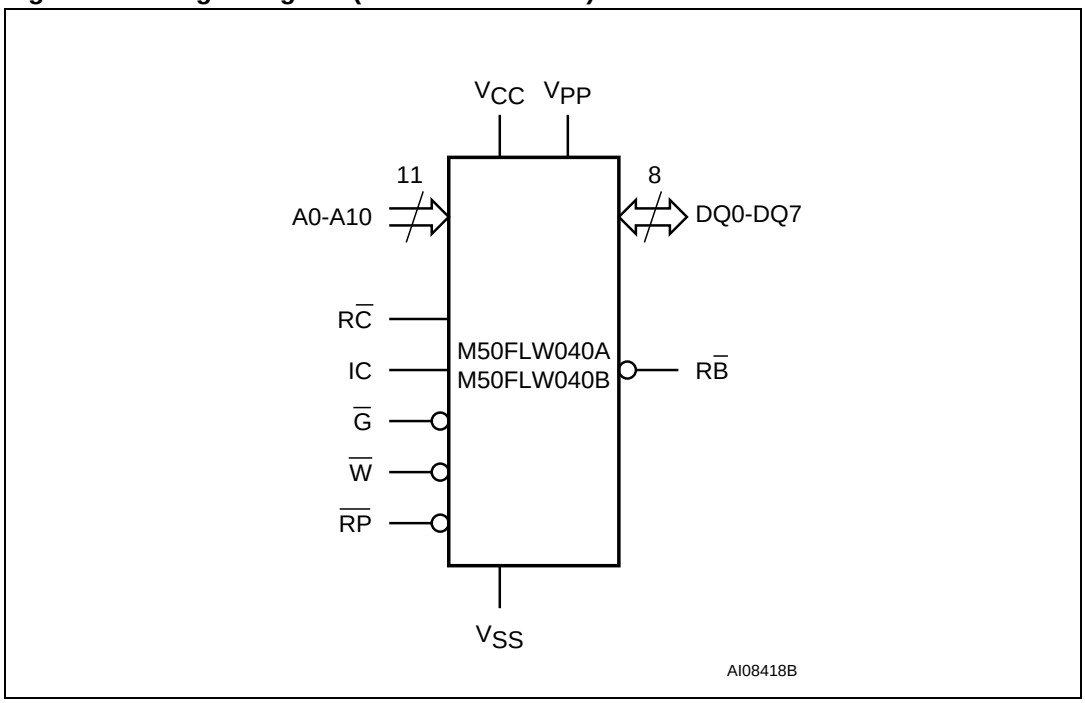
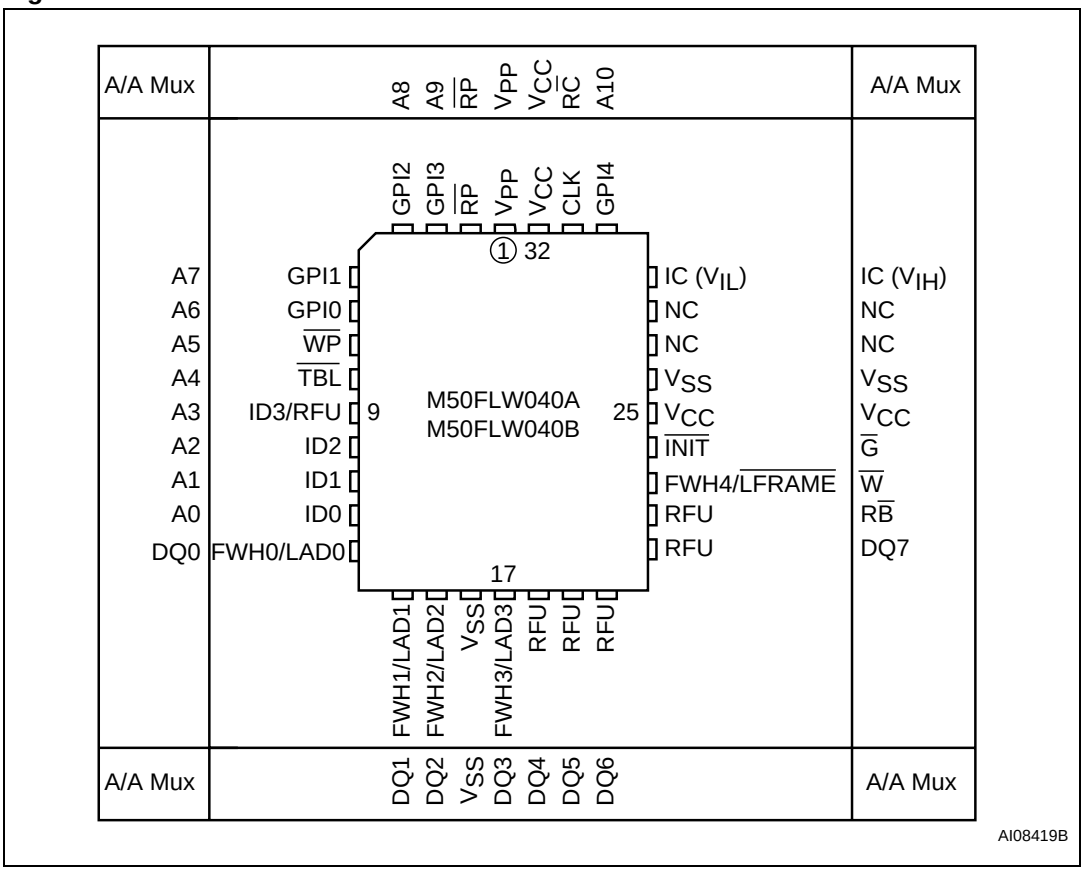


Table 2. Signal names (A/A Mux interface)

IC	Interface Configuration
A0-A10	Address Inputs
DQ0-DQ7	Data Inputs/Outputs
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$R\overline{C}$	Row/Column Address Select
$R\overline{B}$	Ready/Busy Output
$\overline{RP}$	Interface Reset
V_{CC}	Supply Voltage
V_{PP}	Optional Supply Voltage for Fast Program and Erase Operations
V_{SS}	Ground
NC	Not Connected Internally

Figure 3. PLCC connections



1. Pins 27 and 28 are not internally connected.

Figure 4. TSOP32 connections

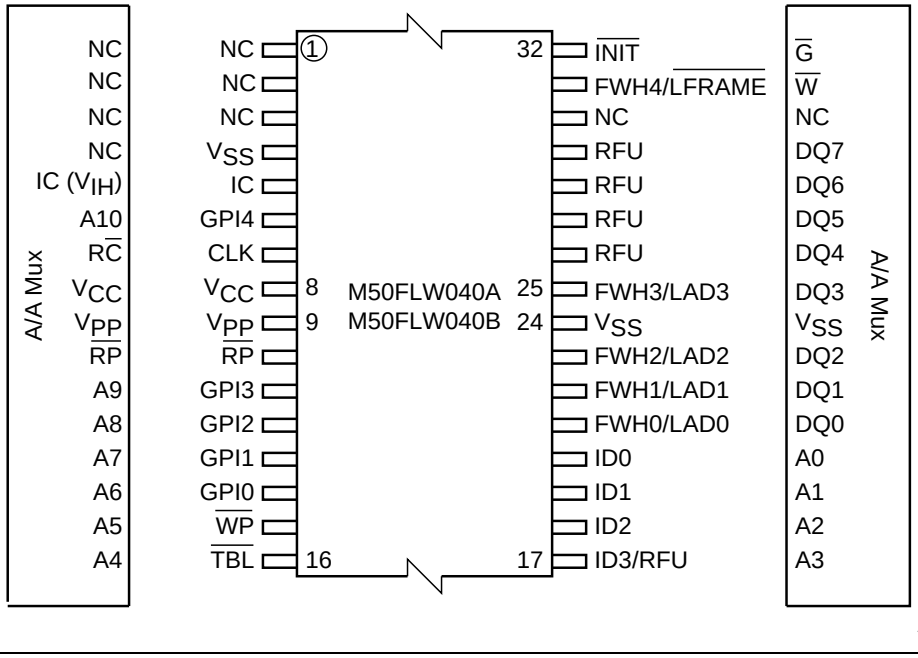


Figure 5. TSOP40 connections

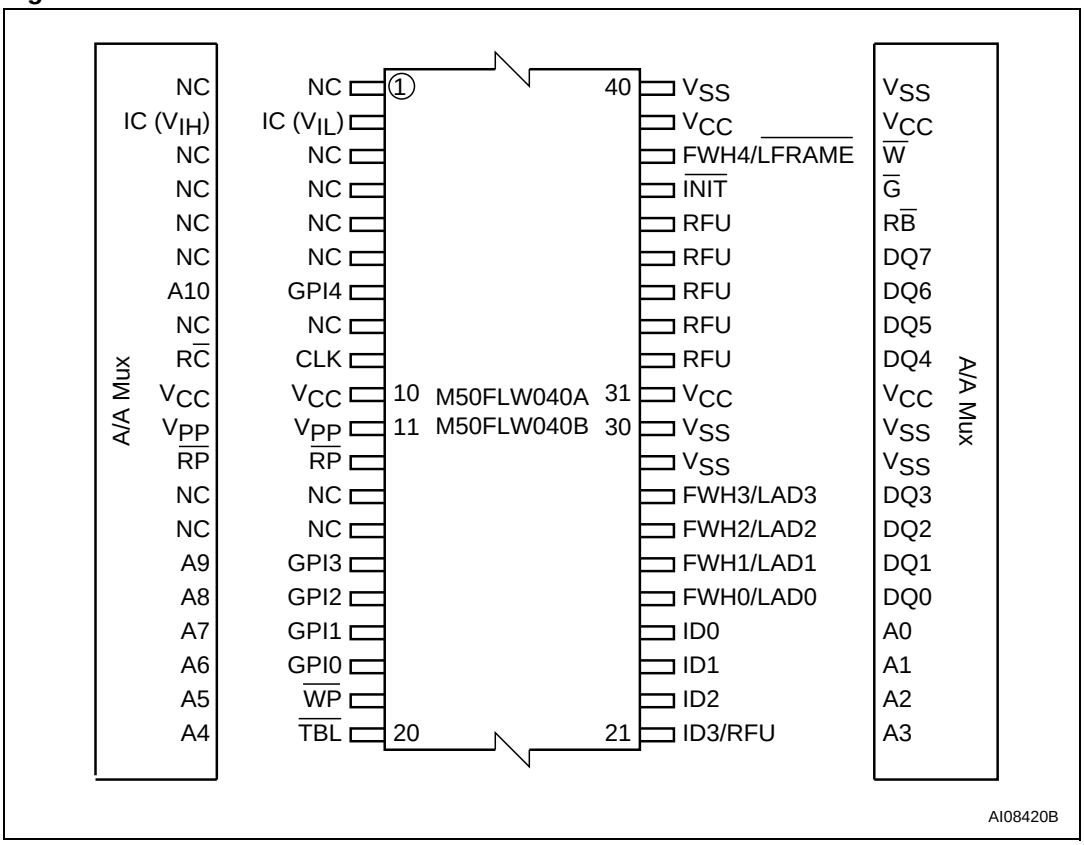


Table 3. Addresses (M50FLW040A)

Block Size (KByte)	Address Range	Sector Size (KByte)
64	70000h-7FFFFh	16 x 4KBytes
64	60000h-6FFFFh	16 x 4KBytes
64	50000h- 5FFFFh	5 x 64KBytes
64	40000h- 4FFFFh	
64	30000h-3FFFFh	
64	20000h-2FFFFh	
64	10000h-1FFFFh	
64	00000h-0FFFFh	16 x 4KBytes

Table 4. Addresses (M50FLW040B)

Block Size (KByte)	Address Range	Sector Size (KByte)
64	70000h-7FFFFh	16 x 4KBytes
64	60000h- 6FFFFh	5 x 64KBytes
64	50000h- 5FFFFh	
64	40000h- 4FFFFh	
64	30000h-3FFFFh	
64	20000h-2FFFFh	
64	10000h-1FFFFh	16 x 4KBytes
64	00000h-0FFFFh	16 x 4KBytes

1. Also see *Appendix A*, *Table 34* and *Table 35* for a full listing of the Block Addresses.

2 Signal descriptions

There are two distinct bus interfaces available on this device. The active interface is selected before power-up, or during Reset, using the Interface Configuration Pin, IC.

The signals for each interface are discussed in the *Firmware Hub/low-pin count (FWH/LPC) signal descriptions* section and the *Address/Address Multiplexed (A/A Mux) signal descriptions* section, respectively, while the supply signals are discussed in the *Supply signal descriptions* section.

2.1 Firmware Hub/low-pin count (FWH/LPC) signal descriptions

Please see *Figure 1* and *Table 1*.

2.1.1 Input/Output communications (FWH0/LAD0-FWH3/LAD3)

All Input and Output Communications with the memory take place on these pins. Addresses and Data for Bus Read and Bus Write operations are encoded on these pins.

2.1.2 Input communication frame (FWH4/$\overline{\text{LFRAME}}$)

The Input Communication Frame (FWH4/$\overline{\text{LFRAME}}$) signal indicates the start of a bus operation. When Input Communication Frame is Low, V_{IL}, on the rising edge of the Clock, a new bus operation is initiated. If Input Communication Frame is Low, V_{IL}, during a bus operation then the operation is aborted. When Input Communication Frame is High, V_{IH}, the current bus operation is either proceeding or the bus is idle.

2.1.3 Identification inputs (ID0-ID3)

Up to 16 memories can be addressed on a bus, in the Firmware Hub (FWH) mode. The Identification Inputs allow each device to be given a unique 4-bit address. A ‘0’ is signified on a pin by driving it Low, V_{IL}, or leaving it floating (since there is an internal pull-down resistor, with a value of R_{IL}). A ‘1’ is signified on a pin by driving it High, V_{IH} (and there will be a leakage current of I_{LI2} through the pin).

By convention, the boot memory must have address ‘0000’, and all additional memories are given addresses, allocated sequentially, from ‘0001’.

In the Low Pin Count (LPC) mode, the identification Inputs (ID0-ID2) can address up to 8 memories on a bus. In the LPC mode, the ID3 pin is Reserved for Future Use (RFU). The value on address A19-A21 is compared to the hardware strapping on the ID0-ID2 pins to select the memory that is being addressed. For an address bit to be ‘1’, the corresponding ID pin can be left floating or driven Low, V_{IL} (again, with the internal pull-down resistor, with a value of R_{IL}). For an address bit to be ‘0’, the corresponding ID pin must be driven High, V_{IH} (and there will be a leakage current of I_{LI2} through the pin, as specified in *Table 24*). For details, see *Table 5*.

2.1.4 General-purpose inputs (GPI0-GPI4)

The General Purpose Inputs can be used as digital inputs for the CPU to read, with their contents being available in the General Purpose Inputs Register. The pins must have stable data throughout the entire cycle that reads the General Purpose Input Register. These pins should be driven Low, $V_{IL,}$ or High, V_{IH}, and must not be left floating.

2.1.5 Interface Configuration (IC)

The Interface Configuration input selects whether the FWH/LPC interface or the Address/Address Multiplexed (A/A Mux) Interface is used. The state of the Interface Configuration, IC, should not be changed during operation of the memory device, except for selecting the desired interface in the period before power-up or during a Reset.

To select the FWH/LPC Interface, the Interface Configuration pin should be left to float or driven Low, V_{IL}. To select the Address/Address Multiplexed (A/A Mux) Interface, the pin should be driven High, V_{IH}. An internal pull-down resistor is included with a value of R_{IL}; there will be a leakage current of I_{LI2} through each pin when pulled to V_{IH}.

2.1.6 Interface Reset ($\overline{RP}$)

The Interface Reset ($\overline{RP}$) input is used to reset the device. When Interface Reset ($\overline{RP}$) is driven Low, V_{IL}, the memory is in Reset mode (the outputs go to high impedance, and the current consumption is minimized). When $\overline{RP}$ is driven High, V_{IH}, the device is in normal operation. After exiting Reset mode, the memory enters Read mode.

2.1.7 CPU Reset ($\overline{INIT}$)

The CPU Reset, $\overline{INIT}$, signal is used to Reset the device when the CPU is reset. It behaves identically to Interface Reset, $\overline{RP}$, and the internal Reset line is the logical OR (electrical AND) of $\overline{RP}$ and $\overline{INIT}$.

2.1.8 Clock (CLK)

The Clock, CLK, input is used to clock the signals in and out of the Input/Output Communication Pins, FWH0/LAD0-FWH3/LAD3. The Clock conforms to the PCI specification.

2.1.9 Top Block Lock ($\overline{TBL}$)

The Top Block Lock input is used to prevent the Top Block (Block 7) from being changed. When Top Block Lock, $\overline{TBL}$, is driven Low, V_{IL}, program and erase operations in the Top Block have no effect, regardless of the state of the Lock Register. When Top Block Lock, $\overline{TBL}$, is driven High, V_{IH}, the protection of the Block is determined by the Lock Register. The state of Top Block Lock, $\overline{TBL}$, does not affect the protection of the Main Blocks (Blocks 0 to 6). For details, see *Appendix A*.

Top Block Lock, $\overline{TBL}$, must be set prior to a program or erase operation being initiated, and must not be changed until the operation has completed, otherwise unpredictable results may occur. Similarly, unpredictable behavior is possible if $\overline{WP}$ is changed during Program or Erase Suspend, and care should be taken to avoid this.

2.1.10 Write Protect ($\overline{WP}$)

The Write Protect input is used to prevent the Main Blocks (Blocks 0 to 6) from being changed. When Write Protect, $\overline{WP}$, is driven Low, V_{IL}, Program and Erase operations in the Main Blocks have no effect, regardless of the state of the Lock Register. When Write Protect, $\overline{WP}$, is driven High, V_{IH}, the protection of the Block is determined by the Lock Register. The state of Write Protect, $\overline{WP}$, does not affect the protection of the Top Block (Block 7). For details, see *Appendix A*.

Write Protect, $\overline{WP}$, must be set prior to a Program or Erase operation is initiated, and must not be changed until the operation has completed otherwise unpredictable results may occur. Similarly, unpredictable behavior is possible if $\overline{WP}$ is changed during Program or Erase Suspend, and care should be taken to avoid this.

2.1.11 Reserved for Future Use (RFU)

These pins do not presently have assigned functions. They must be left disconnected, except for ID3 (when in LPC mode) which can be left connected. The electrical characteristics for this signal are as described in the "*Identification inputs (ID0-ID3)*" section.

2.2 Address/Address Multiplexed (A/A Mux) signal descriptions

Please see *Figure 2* and *Table 2*.

2.2.1 Address inputs (A0-A10)

The Address Inputs are used to set the Row Address bits (A0-A10) and the Column Address bits (A11-A18). They are latched during any bus operation by the Row/Column Address Select input, $\overline{RC}$.

2.2.2 Data Inputs/Outputs (DQ0-DQ7)

The Data Inputs/Outputs hold the data that is to be written to or read from the memory. They output the data stored at the selected address during a Bus Read operation. During Bus Write operations they carry the commands that are sent to the Command Interface of the internal state machine. The Data Inputs/Outputs, DQ0-DQ7, are latched during a Bus Write operation.

2.2.3 Output Enable ($\overline{G}$)

The Output Enable signal, $\overline{G}$, controls the output buffers during a Bus Read operation.

2.2.4 Write Enable ($\overline{W}$)

The Write Enable signal, $\overline{W}$, controls the Bus Write operation of the Command Interface.

2.2.5 Row/Column Address Select ($\overline{RC}$)

The Row/Column Address Select input selects whether the Address Inputs are to be latched into the Row Address bits (A0-A10) or the Column Address bits (A11-A18). The Row Address bits are latched on the falling edge of $\overline{RC}$ whereas the Column Address bits are latched on its rising edge.

2.2.6 Ready/Busy output ($R\overline{B}$)

The Ready/Busy pin gives the status of the device's Program/Erase Controller. When Ready/Busy is Low, V_{OL}, the device is busy with a program or erase operation, and it will not accept any additional program or erase command (except for the Program/Erase Suspend command). When Ready/Busy is High, V_{OH}, the memory is ready for any read, program or erase operation.

2.3 Supply signal descriptions

The Supply Signals are the same for both interfaces.

2.3.1 V_{CC} supply voltage

The V_{CC} Supply Voltage supplies the power for all operations (read, program, erase, etc.).

The Command Interface is disabled when the V_{CC} Supply Voltage is less than the Lockout Voltage, V_{LKO}. This is to prevent Bus Write operations from accidentally damaging the data during power up, power down and power surges. If the Program/Erase Controller is programming or erasing during this time, the operation aborts, and the memory contents that were being altered will be invalid. After V_{CC} becomes valid, the Command Interface is reset to Read mode.

A 0.1µF capacitor should be connected between the V_{CC} Supply Voltage pins and the V_{SS} Ground pin to decouple the current surges from the power supply. Both V_{CC} Supply Voltage pins must be connected to the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.

2.3.2 V_{PP} optional supply voltage

The V_{PP} Optional Supply Voltage pin is used to select the Fast Program (see the Quadruple Byte Program command description in A/A Mux interface and the Double/Quadruple Byte Program command description in FWH mode) and Fast Erase options of the memory.

When $V_{PP} = V_{CC}$, program and erase operations take place as normal. When $V_{PP} = V_{PPH}$, Fast Program and Erase operations are used. Any other voltage input to V_{PP} will result in undefined behavior, and should not be used.

V_{PP} should not be set to V_{PPH} for more than 80 hours during the life of the memory.

2.3.3 V_{SS} ground

V_{SS} is the reference for all the voltage measurements.

Table 5. Memory identification input configuration (LPC mode)

Memory number	ID2	ID1	ID0	A21	A20	A19
1 (Boot memory)	V_{IL} or float	V_{IL} or float	V_{IL} or float	1	1	1
2	V_{IL} or float	V_{IL} or float	V_{IH}	1	1	0
3	V_{IL} or float	V_{IH}	V_{IL} or float	1	0	1
4	V_{IL} or float	V_{IH}	V_{IH}	1	0	0
5	V_{IH}	V_{IL} or float	V_{IL} or float	0	1	1
6	V_{IH}	V_{IL} or float	V_{IH}	0	1	0
7	V_{IH}	V_{IH}	V_{IL} or float	0	0	1
8	V_{IH}	V_{IH}	V_{IH}	0	0	0

3 Bus operations

The two interfaces, A/A Mux and FWH/LPC, support similar operations, but with different bus signals and timings. The Firmware Hub/Low Pin Count (FWH/LPC) Interface offers full functionality, while the Address/Address Multiplexed (A/A Mux) Interface is orientated for erase and program operations.

See the sections below, The *Firmware hub/low-pin count (FWH/LPC) bus operations* and *Address/Address Multiplexed (A/A Mux) bus operations*, for details of the bus operations on each interface.

3.1 Firmware hub/low-pin count (FWH/LPC) bus operations

The M50FLW040 automatically identifies the type of FWH/LPC protocol from the first received nibble (START nibble) and decodes the data that it receives afterwards, according to the chosen FWH or LPC mode. The Firmware Hub/Low Pin Count (FWH/LPC) Interface consists of four data signals (FWH0/LAD0-FWH3/LAD3), one control line (FWH4/$\overline{\text{LFRAME}}$) and a clock (CLK).

Protection against accidental or malicious data corruption is achieved using two additional signals ($\overline{\text{TBL}}$ and $\overline{\text{WP}}$). And two reset signals ($\overline{\text{RP}}$ and $\overline{\text{INIT}}$) are available to put the memory into a known state.

The data, control and clock signals are designed to be compatible with PCI electrical specifications. The interface operates with clock speeds of up to 33MHz.

The following operations can be performed using the appropriate bus cycles: Bus Read, Bus Write, Standby, Reset and Block Protection.

3.1.1 Bus Read

Bus Read operations are used to read from the memory cells, specific registers in the Command Interface or Firmware Hub/Low Pin Count Registers. A valid Bus Read operation starts on the rising edge of the Clock signal when the Input Communication Frame, FWH4/$\overline{\text{LFRAME}}$, is Low, V_{IL}, and the correct Start cycle is present on FWH0/LAD0-FWH3/LAD3. On subsequent clock cycles the Host will send to the memory:

- ID Select, Address and other control bits on FWH0-FWH3 in FWH mode.
- Type+Dir Address and other control bits on LAD0-LAD3 in LPC mode.

The device responds by outputting Sync data until the wait states have elapsed, followed by Data0-Data3 and Data4-Data7.

See *Table 6* and *Table 8*, and *Figure 6* and *Figure 8*, for a description of the Field definitions for each clock cycle of the transfer. See *Table 26*, and *Figure 14*, for details on the timings of the signals.

3.1.2 Bus Write

Bus Write operations are used to write to the Command Interface or Firmware Hub/Low Pin Count Registers. A valid Bus Write operation starts on the rising edge of the Clock signal when Input Communication Frame, FWH4/$\overline{\text{LFRAME}}$, is Low, V_{IL}, and the correct Start cycle is present on FWH0/LAD0-FWH3/LAD3. On subsequent Clock cycles the Host will send to the memory:

- ID Select, Address, other control bits, Data0-Data3 and Data4-Data7 on FWH0-FWH3 in FWH mode.
- Cycle Type + Dir, Address, other control bits, Data0-Data3 and Data4-Data7 on LAD0-LAD3.

The device responds by outputting Sync data until the wait states have elapsed.

See *Table 7* and *Table 9*, and *Figure 7* and *Figure 9*, for a description of the Field definitions for each clock cycle of the transfer. See *Table 26*, and *Figure 14*, for details on the timings of the signals.

3.1.3 Bus Abort

The Bus Abort operation can be used to abort the current bus operation immediately. A Bus Abort occurs when FWH4/$\overline{\text{LFRAME}}$ is driven Low, V_{IL}, during the bus operation. The device puts the Input/Output Communication pins, FWH0/LAD0-FWH3/LAD3, to high impedance.

Note that, during a Bus Write operation, the Command Interface starts executing the command as soon as the data is fully received. A Bus Abort during the final TAR cycles is not guaranteed to abort the command. The bus, however, will be released immediately.

3.1.4 Standby

When FWH4/$\overline{\text{LFRAME}}$ is High, V_{IH}, the device is put into Standby mode, where FWH0/LAD0-FWH3/LAD3 are put into a high-impedance state and the Supply Current is reduced to the Standby level, I_{CC1}.

3.1.5 Reset

During the Reset mode, all internal circuits are switched off, the device is deselected, and the outputs are put to high-impedance. The device is in the Reset mode when Interface Reset, $\overline{\text{RP}}$, or CPU Reset, $\overline{\text{INIT}}$, is driven Low, V_{IL}. $\overline{\text{RP}}$ or $\overline{\text{INIT}}$ must be held Low, V_{IL}, for t_{PLPH}. The memory reverts to the Read mode upon return from the Reset mode, and the Lock Registers return to their default states regardless of their states before Reset. If $\overline{\text{RP}}$ or $\overline{\text{INIT}}$ goes Low, V_{IL}, during a Program or Erase operation, the operation is aborted and the affected memory cells no longer contain valid data. The device can take up to t_{PLRH} to abort a Program or Erase operation.

3.1.6 Block Protection

Block Protection can be forced using the signals Top Block Lock, $\overline{\text{TBL}}$, and Write Protect, $\overline{\text{WP}}$, regardless of the state of the Lock Registers.

3.2 Address/Address Multiplexed (A/A Mux) bus operations

The Address/Address Multiplexed (A/A Mux) Interface has a more traditional-style interface. The signals consist of a multiplexed address signals (A0-A10), data signals, (DQ0-DQ7) and three control signals ($\overline{RC}$, $\overline{G}$, $\overline{W}$). An additional signal, $\overline{RP}$, can be used to reset the memory.

The Address/Address Multiplexed (A/A Mux) Interface is included for use by Flash Programming equipment for faster factory programming. Only a subset of the features available to the Firmware Hub (FWH)/Low Pin Count (LPC) Interface are available; these include all the Commands but exclude the Security features and other registers.

The following operations can be performed using the appropriate bus cycles: Bus Read, Bus Write, Output Disable and Reset.

When the Address/Address Multiplexed (A/A Mux) Interface is selected, all the blocks are unprotected. It is not possible to protect any blocks through this interface.

3.2.1 Bus Read

Bus Read operations are used to read the contents of the Memory Array, the Electronic Signature or the Status Register. A valid Bus Read operation begins by latching the Row Address and Column Address signals into the memory using the Address Inputs, A0-A10, and the Row/Column Address Select $\overline{RC}$. Write Enable ($\overline{W}$) and Interface Reset ($\overline{RP}$) must be High, V_{IH}, and Output Enable, $\overline{G}$, Low, V_{IL}. The Data Inputs/Outputs will output the value, according to the timing constraints specified in *Figure 16*, and *Table 28*.

3.2.2 Bus Write

Bus Write operations are used to write to the Command Interface. A valid Bus Write operation begins by latching the Row Address and Column Address signals into the memory using the Address Inputs, A0-A10, and the Row/Column Address Select $\overline{RC}$. The data should be set up on the Data Inputs/Outputs; Output Enable, $\overline{G}$, and Interface Reset, $\overline{RP}$, must be High, V_{IH}; and Write Enable, $\overline{W}$, must be Low, V_{IL}. The Data Inputs/Outputs are latched on the rising edge of Write Enable, $\overline{W}$. See *Figure 17*, and *Table 29*, for details of the timing requirements.

3.2.3 Output Disable

The data outputs are high-impedance when the Output Enable, $\overline{G}$, is at V_{IH}.

3.2.4 Reset

During the Reset mode, all internal circuits are switched off, the device is deselected, and the outputs are put at high-impedance. The device is in the Reset mode when $\overline{RP}$ is Low, V_{IL}. $\overline{RP}$ must be held Low, V_{IL} for t_{PLPH}. If $\overline{RP}$ goes Low, V_{IL}, during a Program or Erase operation, the operation is aborted, and the affected memory cells no longer contain valid data. The memory can take up to t_{PLRH} to abort a Program or Erase operation.

Table 6. FWH bus read field definitions

Clock Cycle Number	Clock Cycle Count	Field	FWH0-FWH3	Memory I/O	Description
1	1	START	1101b	I	On the rising edge of CLK with FWH4 Low, the contents of FWH0-FWH3 indicate the start of a FWH Read cycle.
2	1	IDSEL	XXXX	I	Indicates which FWH Flash Memory is selected. The value on FWH0-FWH3 is compared to the IDSEL strapping on the FWH Flash Memory pins to select which FWH Flash Memory is being addressed.
3-9	7	ADDR	XXXX	I	A 28-bit address is transferred, with the most significant nibble first. For the multi-byte read operation, the least significant bits (MSIZE of them) are treated as Don't Care, and the read operation is started with each of these bits reset to 0. Address lines A19-21 and A23-27 are treated as Don't Care during a normal memory array access, with A22=1, but are taken into account for a register access, with A22=0. (See *Table 15*)
10	1	MSIZE	XXXX	I	This one clock cycle is driven by the host to determine the number of Bytes that will be transferred. M50FLW040 supports: single Byte transfer (0000b), 2-Byte transfer (0001b), 4-Byte transfer (0010b), 16-Byte transfer (0100b) and 128-Byte transfer (0111b).
11	1	TAR	1111b	I	The host drives FWH0-FWH3 to 1111b to indicate a turnaround cycle.
12	1	TAR	1111b (float)	O	The FWH Flash Memory takes control of FWH0-FWH3 during this cycle.
13-14	2	WSYNC	0101b	O	The FWH Flash Memory drives FWH0-FWH3 to 0101b (short wait-sync) for two clock cycles, indicating that the data is not yet available. Two wait-states are always included.
15	1	RSYNC	0000b	O	The FWH Flash Memory drives FWH0-FWH3 to 0000b, indicating that data will be available during the next clock cycle.
16-17	M=2n	DATA	XXXX	O	Data transfer is two CLK cycles, starting with the least significant nibble. If multi-Byte read operation is enabled, repeat cycle-16 and cycle-17 *n* times, where $n = 2^{MSIZE}$.
previous +1	1	TAR	1111b	O	The FWH Flash Memory drives FWH0-FWH3 to 1111b to indicate a turnaround cycle.
previous +1	1	TAR	1111b (float)	N/A	The FWH Flash Memory floats its outputs, the host takes control of FWH0-FWH3.

Figure 6. FWH bus read waveforms

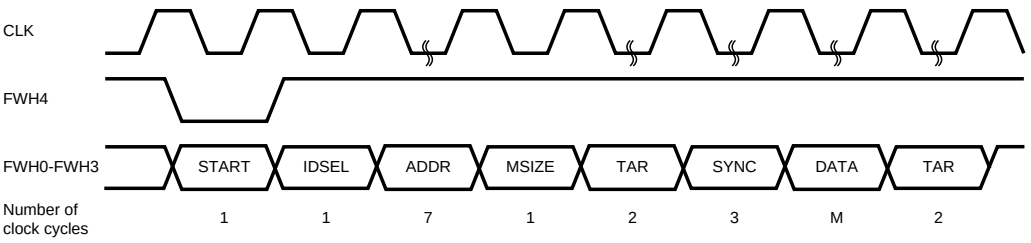


Table 7. FWH bus write field definitions

Clock Cycle Number	Clock Cycle Count	Field	FWH0-FWH3	Memory I/O	Description
1	1	START	1110b	I	On the rising edge of CLK with FWH4 Low, the contents of FWH0-FWH3 indicate the start of a FWH Write Cycle.
2	1	IDSEL	XXXX	I	Indicates which FWH Flash Memory is selected. The value on FWH0-FWH3 is compared to the IDSEL strapping on the FWH Flash Memory pins to select which FWH Flash Memory is being addressed.
3-9	7	ADDR	XXXX	I	A 28-bit address is transferred, with the most significant nibble first. Address lines A19-21 and A23-27 are treated as Don't Care during a normal memory array access, with A22=1, but are taken into account for a register access, with A22=0. (See *Table 15*)
10	1	MSIZE	XXXX	I	0000(Single Byte Transfer) 0001 (Double Byte Transfer) 0010b (Quadruple Byte Transfer).
11-18	M=2/4/8	DATA	XXXX	I	Data transfer is two cycles, starting with the least significant nibble. (The first pair of nibbles is that at the address with A1- A0 set to 00, the second pair with A1-A0 set to 01, the third pair with A1-A0 set to 10, and the fourth pair with A1-A0 set to 11. In Double Byte Program the first pair of nibbles is that at the address with A0 set to 0, the second pair with A0 set to 1)
previous +1	1	TAR	1111b	I	The host drives FWH0-FWH3 to 1111b to indicate a turnaround cycle.
previous +1	1	TAR	1111b (float)	O	The FWH Flash Memory takes control of FWH0-FWH3 during this cycle.
previous +1	1	SYNC	0000b	O	The FWH Flash Memory drives FWH0-FWH3 to 0000b, indicating it has received data or a command.
previous +1	1	TAR	1111b	O	The FWH Flash Memory drives FWH0-FWH3 to 1111b, indicating a turnaround cycle.
previous +1	1	TAR	1111b (float)	N/A	The FWH Flash Memory floats its outputs and the host takes control of FWH0-FWH3.

Figure 7. FWH bus write waveforms

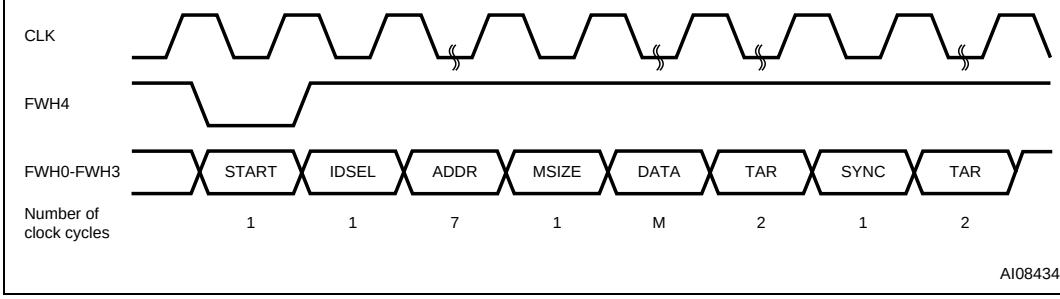


Table 8. LPC bus read field definitions (1-byte)

Clock Cycle Number	Clock Cycle Count	Field	LAD0-LAD3	Memory I/O	Description
1	1	START	0000b	I	On the rising edge of CLK with $\overline{\text{LFRAME}}$ Low, the contents of LAD0-LAD3 must be 0000b to indicate the start of a LPC cycle.
2	1	CYCTYPE + DIR	0100b	I	Indicates the type of cycle and selects 1-byte reading. Bits 3:2 must be 01b. Bit 1 indicates the direction of transfer: 0b for read. Bit 0 is Don't Care.
3-10	8	ADDR	XXXX	I	A 32-bit address is transferred, with the most significant nibble first. A23-A31 must be set to 1. A22=1 for memory access, and A22=0 for register access. *Table 5* shows the appropriate values for A21-A19.
11	1	TAR	1111b	I	The host drives LAD0-LAD3 to 1111b to indicate a turnaround cycle.
12	1	TAR	1111b (float)	O	The LPC Flash Memory takes control of LAD0-LAD3 during this cycle.
13-14	2	WSYNC	0101b	O	The LPC Flash Memory drives LAD0-LAD3 to 0101b (short wait-sync) for two clock cycles, indicating that the data is not yet available. Two wait-states are always included.
15	1	RSYNC	0000b	O	The LPC Flash Memory drives LAD0-LAD3 to 0000b, indicating that data will be available during the next clock cycle.
16-17	2	DATA	XXXX	O	Data transfer is two CLK cycles, starting with the least significant nibble.
18	1	TAR	1111b	O	The LPC Flash Memory drives LAD0-LAD3 to 1111b to indicate a turnaround cycle.
19	1	TAR	1111b (float)	N/A	The LPC Flash Memory floats its outputs, the host takes control of LAD0-LAD3.

Figure 8. LPC bus read waveforms (1-byte)

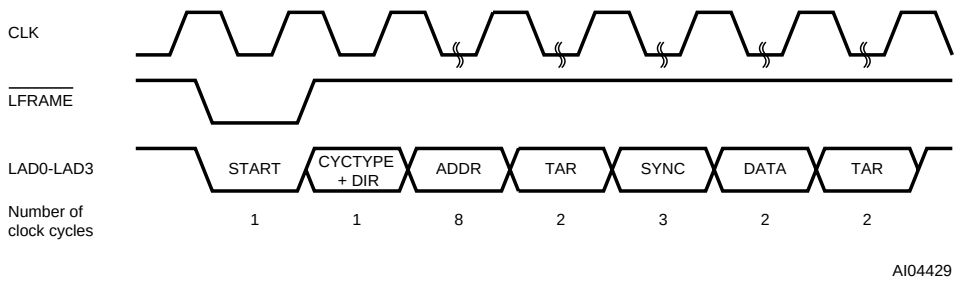


Table 9. LPC bus write field definitions (1 byte)

Clock Cycle Number	Clock Cycle Count	Field	LAD0-LAD3	Memory I/O	Description
1	1	START	0000b	I	On the rising edge of CLK with $\overline{\text{LFRAME}}$ Low, the contents of LAD0-LAD3 must be 0000b to indicate the start of a LPC cycle.
2	1	CYCTYPE + DIR	011Xb	I	Indicates the type of cycle. Bits 3:2 must be 01b. Bit 1 indicates the direction of transfer: 1b for write. Bit 0 is don't care (X).
3-10	8	ADDR	XXXX	I	A 32-bit address is transferred, with the most significant nibble first. A23-A31 must be set to 1. A22=1 for memory access, and A22=0 for register access. *Table 5* shows the appropriate values for A21-A19.
11-12	2	DATA	XXXX	I	Data transfer is two cycles, starting with the least significant nibble.
13	1	TAR	1111b	I	The host drives LAD0-LAD3 to 1111b to indicate a turnaround cycle.
14	1	TAR	1111b (float)	O	The LPC Flash Memory takes control of LAD0-LAD3 during this cycle.
15	1	SYNC	0000b	O	The LPC Flash Memory drives LAD0-LAD3 to 0000b, indicating it has received data or a command.
16	1	TAR	1111b	O	The LPC Flash Memory drives LAD0-LAD3 to 1111b, indicating a turnaround cycle.
17	1	TAR	1111b (float)	N/A	The LPC Flash Memory floats its outputs and the host takes control of LAD0-LAD3.

Figure 9. LPC bus write waveforms (1 byte)

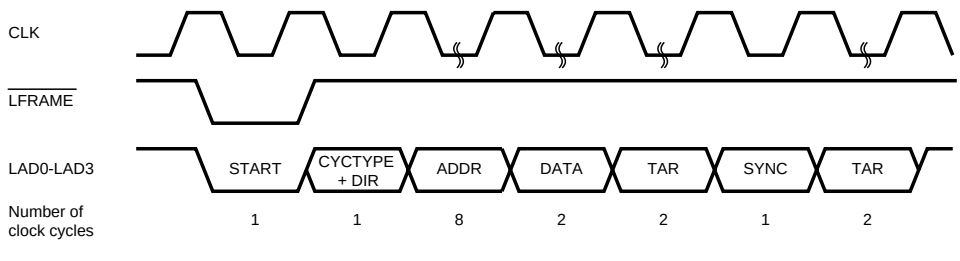


Table 10. A/A Mux bus operations

Operation	$\overline{G}$	$\overline{W}$	$\overline{RP}$	V_{PP}	DQ7-DQ0
Bus Read	V_{IL}	V_{IH}	V_{IH}	Don't Care	Data Output
Bus Write	V_{IH}	V_{IL}	V_{IH}	V_{CC} or V_{PPH}	Data Input
Output Disable	V_{IH}	V_{IH}	V_{IH}	Don't Care	Hi-Z
Reset	V_{IL} or V_{IH}	V_{IL} or V_{IH}	V_{IL}	Don't Care	Hi-Z

4 Command interface

All Bus Write operations to the device are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. An internal Program/Erase Controller handles all timings, and verifies the correct execution of the Program and Erase commands. The Program/Erase Controller provides a Status Register whose output may be read at any time to monitor the progress or the result of the operation.

The Command Interface reverts to the Read mode when power is first applied, or when exiting from Reset. Command sequences must be followed exactly. Any invalid combination of commands will be ignored. See *Table 11* for the available Command Codes.

Table 11. Command codes

Hexadecimal	Command
10h	Alternative Program Setup, Double/Quadruple Byte Program Setup, Chip Erase Confirm
20h	Block Erase Setup
32h	Sector Erase Setup
40h	Program, Double/Quadruple Byte Program Setup
50h	Clear Status Register
70h	Read Status Register
80h	Chip Erase Setup
90h	Read Electronic Signature
B0h	Program/Erase Suspend
D0h	Program/Erase Resume, Block Erase Confirm, Sector Erase Confirm
FFh	Read Memory Array

The following commands are the basic commands used to read from, write to, and configure the device. The following text descriptions should be read in conjunction with *Table 13*.

4.0.1 Read Memory Array command

The Read Memory Array command returns the device to its Read mode, where it behaves like a ROM or EPROM. One Bus Write cycle is required to issue the Read Memory Array command and return the device to Read mode. Once the command is issued, the device remains in Read mode until another command is issued. From Read mode, Bus Read operations access the memory array.

If the Program/Erase Controller is executing a Program or Erase operation, the device will not accept any Read Memory Array commands until the operation has completed.

For a multibyte read, in the FWH mode, the address, that was transmitted with the command, will be automatically aligned, according to the MSIZE granularity. For example, if MSIZE=7, regardless of any values that are provided for A6-A0, the first output will be from the location for which A6-A0 are all ‘0’s.

4.0.2 Read Status Register command

The Read Status Register command is used to read the Status Register. One Bus Write cycle is required to issue the Read Status Register command. Once the command is issued, subsequent Bus Read operations read the Status Register until another command is issued. See the section on the Status Register for details on the definitions of the Status Register bits.

4.0.3 Read Electronic Signature command

The Read Electronic Signature command is used to read the Manufacturer Code and the Device Code. One Bus Write cycle is required to issue the Read Electronic Signature command. Once the command is issued, the Manufacturer Code and Device Code can be read using conventional Bus Read operations, and the addresses shown in *Table 12*.

Table 12. Electronic signature codes

Code		Address(1)	Data
Manufacturer Code		...00000h	20h
Device Code	M50FLW040A M50FLW040B	...00001h	08h 28h

1. A22 should be '1', and the ID lines and upper address bits should be set according to the rules illustrated in *Table 5*, *Table 6* and *Table 8*.

The device remains in this mode until another command is issued. That is, subsequent Bus Read operations continue to read the Manufacturer Code, or the Device Code, and not the Memory Array.

4.0.4 Program command

The Program command can be used to program a value to one address in the memory array at a time.

The Program command works by changing appropriate bits from '1' to '0'. (It cannot change a bit from '0' back to '1'. Attempting to do so will not modify the value of the bit. Only the Erase command can set bits back to '1'. and does so for all of the bits in the block.)

Two Bus Write operations are required to issue the Program command. The second Bus Write cycle latches the address and data, and starts the Program/Erase Controller.

Once the command is issued, subsequent Bus Read operations read the value in the Status Register. (See the section on the Status Register for details on the definitions of the Status Register bits.)

If the address falls in a protected block, the Program operation will abort, the data in the memory array will not be changed, and the Status Register will indicate the error.

During the Program operation, the memory will only accept the Read Status Register command and the Program/Erase Suspend command. All other commands are ignored.

See *Figure 21*, for a suggested flowchart on using the Program command. Typical Program times are given in *Table 18*.

4.0.5 Quadruple Byte Program command (A/A Mux interface)

The Quadruple Byte Program Command is used to program four adjacent Bytes in the memory array at a time. The four Bytes must differ only for addresses A0 and A1. Programming should not be attempted when V_{PP} is not at V_{PPH}.

Five Bus Write operations are required to issue the command. The second, third and fourth Bus Write cycles latch the respective addresses and data of the first, second and third Bytes in the Program/Erase Controller. The fifth Bus Write cycle latches the address and data of the fourth Byte and starts the Program/Erase Controller. Once the command is issued, subsequent Bus Read operations read the value in the Status Register. (See the section on the Status Register for details on the definitions of the Status Register bits.)

During the Quadruple Byte Program operation, the memory will only accept the Read Status Register and Program/Erase Suspend commands. All other commands are ignored.

Note that the Quadruple Byte Program command cannot change a bit set to '0' back to '1' and attempting to do so will not modify its value. One of the erase commands must be used to set all of the bits in the block to '1'.

See *Figure 23*, for a suggested flowchart on using the Quadruple Byte Program command. Typical Quadruple Byte Program times are given in *Table 18*.

4.0.6 Double/Quadruple Byte Program command (FWH mode)

The Double/Quadruple Byte Program Command can be used to program two/four adjacent Bytes to the memory array at a time. The two Bytes must differ only for address A0; the four Bytes must differ only for addresses A0 and A1.

Two Bus Write operations are required to issue the command. The second Bus Write cycle latches the start address and two/four data Bytes and starts the Program/Erase Controller. Once the command is issued, subsequent Bus Read operations read the contents of the Status Register. (See the section on the Status Register for details on the definitions of the Status Register bits.)

During the Double/Quadruple Byte Program operation the memory will only accept the Read Status register and Program/Erase Suspend commands. All other commands are ignored.

Note that the Double/Quadruple Byte Program command cannot change a bit set to '0' back to '1' and attempting to do so will not modify its value. One of the erase commands must be used to set all of the bits in the block to '1'.

See *Figure 22*, for a suggested flowchart on using the Double/Quadruple Byte Program command. Typical Double/Quadruple Byte Program times are given in *Table 18*.

4.0.7 Chip Erase command

The Chip Erase Command erases the entire memory array, setting all of the bits to '1'. All previous data in the memory array are lost. This command, though, is only available under the A/A Mux interface.

Two Bus Write operations are required to issue the command, and to start the Program/Erase Controller. Once the command is issued, subsequent Bus Read operations read the contents of the Status Register. (See the section on the Status Register for details on the definitions of the Status Register bits.)

Erasing should not be attempted when V_{PP} is not at V_{PPH}, otherwise the result is uncertain.

During the Chip Erase operation, the memory will only accept the Read Status Register command. All other commands are ignored.

See *Figure 25*, for a suggested flowchart on using the Chip Erase command. Typical Chip Erase times are given in *Table 18*.

4.0.8 Block Erase command

The Block Erase command is used to erase a block, setting all of the bits to '1'. All previous data in the block are lost.

Two Bus Write operations are required to issue the command. The second Bus Write cycle latches the block address and starts the Program/Erase Controller. Once the command is issued, subsequent Bus Read operations read the contents of the Status Register. (See the section on the Status Register for details on the definitions of the Status Register bits.)

If the block is protected (FWH/LPC only) then the Block Erase operation will abort, the data in the block will not be changed, and the Status Register will indicate the error.

During the Block Erase operation the memory will only accept the Read Status Register and Program/Erase Suspend commands. All other commands are ignored.

See *Figure 26*, for a suggested flowchart on using the Block Erase command. Typical Block Erase times are given in *Table 18*.

4.0.9 Sector Erase command

The Sector Erase command is used to erase a Uniform 4-KByte Sector, setting all of the bits to '1'. All previous data in the sector are lost.

Two Bus Write operations are required to issue the command. The second Bus Write cycle latches the Sector address and starts the Program/Erase Controller. Once the command is issued, subsequent Bus Read operations read the contents of the Status Register. (See the section on the Status Register for details on the definitions of the Status Register bits.)

If the Block to which the Sector belongs is protected (FWH/LPC only) then the Sector Erase operation will abort, the data in the Sector will not be changed, and the Status Register will indicate the error.

During the Sector Erase operation the memory will only accept the Read Status Register and Program/Erase Suspend commands. All other commands are ignored.

See *Figure 26*, for a suggested flowchart on using the Sector Erase Command. Typical Sector Erase times are given in *Table 18*.

4.0.10 Clear Status Register command

The Clear Status Register command is used to reset Status Register bits SR1, SR3, SR4 and SR5 to '0'. One Bus Write is required to issue the command. Once the command is issued, the device returns to its previous mode, subsequent Bus Read operations continue to output the data from the same area, as before.

Once set, these Status Register bits remain set. They do *not* automatically return to '0', for example, when a new program or erase command is issued. If an error has occurred, it is essential that any error bits in the Status Register are cleared, by issuing the Clear Status Register command, before attempting a new program or erase command.

4.0.11 Program/Erase Suspend command

The Program/Erase Suspend command is used to pause the Program/Erase Controller during a program or Sector/Block Erase operation. One Bus Write cycle is required to issue the command.

Once the command has been issued, it is necessary to poll the Program/Erase Controller Status bit until the Program/Erase Controller has paused. No other commands are accepted until the Program/Erase Controller has paused. After the Program/Erase Controller has paused, the device continues to output the contents of the Status Register until another command is issued.

During the polling period, between issuing the Program/Erase Suspend command and the Program/Erase Controller pausing, it is possible for the operation to complete. Once the Program/Erase Controller Status bit indicates that the Program/Erase Controller is no longer active, the Program Suspend Status bit or the Erase Suspend Status bit can be used to determine if the operation has completed or is suspended.

During Program/Erase Suspend, the Read Memory Array, Read Status Register, Read Electronic Signature and Program/Erase Resume commands will be accepted by the Command Interface. Additionally, if the suspended operation was Sector Erase or Block Erase then the program command will also be accepted. However, it should be noted that only the Sectors/Blocks not being erased may be read or programmed correctly.

See *Figure 24*, and *Figure 27*, for suggested flowcharts on using the Program/Erase Suspend command. Typical times and delay durations are given in *Table 18*.

4.0.12 Program/Erase Resume command

The Program/Erase Resume command can be used to restart the Program/Erase Controller after a Program/Erase Suspend has paused it. One Bus Write cycle is required to issue the command. Once the command is issued, subsequent Bus Read operations read the contents of the Status Register.

Table 13. Commands

Command	Cycle	Bus operations(1)									
		1st		2nd		3rd		4th		5th	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read Memory Array(2),(3),(4)	1+	X	FFh	Read Addr	Read Data	(Read Addr2)	(Read Data2)	(Read Addr3)	(Read Data3)	(Read Addr4)	(Read Data4)
Read Status Register(5),(3)	1+	X	70h	X	Status Reg	(X)	(Status Reg)	(X)	(Status Reg)	(X)	(Status Reg)
Read Electronic Signature(3)	1+	X	90h or 98h	Sig Addr	Signature	(Sig Addr)	(Signature)	(Sig Addr)	(Signature)	(Sig Addr)	(Signature)
Program / Multiple Byte program (FWH)(6),(7),(4)	2	X	40h or 10h	Prog Addr	Prog Data						
Quadruple Byte Program (A/A Mux)(6),(8)	5	X	30h	A1	Prog Data1	A2	Prog Data2	A3	Prog Data3	A4	Prog Data4
Chip Erase(6)	2	X	80h	X	10h						
Block Erase(6)	2	X	20h	BA	D0h						
Sector Erase(6)	2	X	32h	SA	D0h						
Clear Status Register(9)	1	X	50h								
Program/Erase suspend(10)	1	X	B0h								
Program/Erase resume(11)	1	X	D0h								
Invalid reserved(12)	1	X	00h								
	1	X	01h								
	1	X	60h								
	1	X	2Fh								
	1	X	C0h								

1. For all commands: the first cycle is a Write. For the first three commands (Read Memory, Read Status Register, Read Electronic Signature), the second and next cycles are READ. For the remaining commands, the second and next cycles are WRITE.
   BA = Any address in the Block, SA = Any address in the Sector. X = Don't Care, except that A22=1 (for FWH or LPC mode), and A21, A20 and A19 are set according to the rules shown in *Table 5* (for LPC mode)
2. After a Read Memory Array command, read the memory as normal until another command is issued.
3. "1+" indicates that there is one write cycle, followed by any number of read cycles.
4. Configuration registers are accessed directly without using any specific command code. A single Bus Write or Bus Read Operation is all that is needed.
5. After a Read Status Register command, read the Status Register as normal until another command is issued.
6. After the erase and program commands read the Status Register until the command completes and another command is issued.
7. Multiple Byte Program PA= start address, A0 (Double Byte Program) A0 and A1 (Quadruple Byte Program) are Don`t Care. PD is two or four Bytes depending on Msize code.
8. Addresses A1, A2, A3 and A4 must be consecutive addresses, differing only in address bits A0 and A1.
9. After the Clear Status Register command bits SR1, SR3, SR4 and SR5 in the Status Register are reset to '0'.
10. While an operation is being Program/Erase Suspended, the Read Memory Array, Read Status Register, Program (during Erase Suspend) and Program/Erase Resume commands can be issued.
11. The Program/Erase Resume command causes the Program/Erase suspended operation to resume. Read the Status Register until the Program/Erase Controller completes and the memory returns to Read Mode.
12. Do not use Invalid or Reserved commands.

5 Status Register

The Status Register provides information on the current or previous Program or Erase operation. The bits in the Status Register convey specific information about the progress of the operation.

To read the Status Register, the Read Status Register command can be issued. The Status Register is automatically read after Program, Erase and Program/Erase Resume commands are issued. The Status Register can be read from any address.

The text descriptions, below, should be read in conjunction with *Table 14*, where the meanings of the Status Register bits are summarized.

5.1 Program/Erase Controller status (Bit SR7)

This bit indicates whether the Program/Erase Controller is active or inactive. When the Program/Erase Controller Status bit is '0', the Program/Erase Controller is active; when the bit is '1', the Program/Erase Controller is inactive.

The Program/Erase Controller Status is '0' immediately after a Program/Erase Suspend command is issued, until the Program/Erase Controller pauses. After the Program/Erase Controller pauses, the bit is '1'.

The end of a Program and Erase operation can be found by polling the Program/Erase Controller Status bit can be polled. The other bits in the Status Register should not be tested until the Program/Erase Controller has completed the operation (and the Program/Erase Controller Status bit is '1').

After the Program/Erase Controller has completed its operation, the Erase Status, Program Status, V_{PP} Status and Block Protection Status bits should be tested for errors.

5.2 Erase Suspend status (Bit SR6)

This bit indicates that an Erase operation has been suspended, and that it is waiting to be resumed. The Erase Suspend Status should only be considered valid when the Program/Erase Controller Status bit is '1' (Program/Erase Controller inactive). After a Program/Erase Suspend command is issued, the memory may still complete the operation rather than entering the Suspend mode.

When the Erase Suspend Status bit is '0', the Program/Erase Controller is active or has completed its operation. When the bit is '1', a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command.

When a Program/Erase Resume command is issued, the Erase Suspend Status bit returns to '0'.

5.3 Erase status (Bit SR5)

This bit indicates if a problem has occurred during the erasing of a Sector or Block. The Erase Status bit should be read once the Program/Erase Controller Status bit is ‘1’ (Program/Erase Controller inactive).

When the Erase Status bit is ‘0’, the memory has successfully verified that the Sector/Block has been erased correctly. When the Erase Status bit is ‘1’, the Program/Erase Controller has applied the maximum number of pulses to the Sector/Block and still failed to verify that the Sector/Block has been erased correctly.

Once the Erase Status bit is set to ‘1’, it can only be reset to ‘0’ by a Clear Status Register command, or by a hardware reset. If it is set to ‘1’, it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to have failed, too.

5.3.1 Program status (Bit SR4)

This bit indicates if a problem has occurred during the programming of a byte. The Program Status bit should be read once the Program/Erase Controller Status bit is ‘1’ (Program/Erase Controller inactive).

When the Program Status bit is ‘0’, the memory has successfully verified that the byte has been programmed correctly. When the Program Status bit is ‘1’, the Program/Erase Controller has applied the maximum number of pulses to the byte and still failed to verify that the byte has been programmed correctly.

Once the Program Status bit is set to ‘1’, it can only be reset to ‘0’ by a Clear Status Register command, or by a hardware reset. If it is set to ‘1’, it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to have failed, too.

5.3.2 V_{PP} status (Bit SR3)

This bit indicates whether an invalid voltage was detected on the V_{PP} pin at the beginning of a Program or Erase operation. The V_{PP} pin is only sampled at the beginning of the operation. Indeterminate results can occur if V_{PP} becomes invalid during a Program or Erase operation.

Once the V_{PP} Status bit set to ‘1’, it can only be reset to ‘0’ by a Clear Status Register command, or by a hardware reset. If it is set to ‘1’, it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to have failed, too.

5.3.3 Program Suspend status (Bit SR2)

This bit indicates that a Program operation has been suspended, and that it is waiting to be resumed. The Program Suspend Status should only be considered valid when the Program/Erase Controller Status bit is ‘1’ (Program/Erase Controller inactive). After a Program/Erase Suspend command is issued, the memory may still complete the operation instead of entering the Suspend mode.

When the Program Suspend Status bit is ‘0’, the Program/Erase Controller is active, or has completed its operation. When the bit is ‘1’, a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command.

When a Program/Erase Resume command is issued, the Program Suspend Status bit returns to ‘0’.

5.3.4 Block Protection status (Bit SR1)

The Block Protection Status bit can be used to identify if the Program or Erase operation has tried to modify the contents of a protected block. When the Block Protection Status bit is to '0', no Program or Erase operations have been attempted to protected blocks since the last Clear Status Register command or hardware reset. When the Block Protection Status bit is '1', a Program or Erase operation has been attempted on a protected block.

Once it is set to '1', the Block Protection Status bit can only be reset to '0' by a Clear Status Register command or by a hardware reset. If it is set to '1', it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to have failed, too.

Using the A/A Mux Interface, the Block Protection Status bit is always '0'.

5.3.5 Reserved (Bit SR0)

Bit 0 of the Status Register is reserved. Its value should be masked.

Table 14. Status Register bits

Operation	SR7	SR6	SR5	SR4	SR3	SR2	SR1
Program active	'0'	X(1)	'0'	'0'	'0'	'0'	'0'
Program suspended	'1	X(1)	'0'	'0'	'0'	'1'	'0'
Program completed successfully	'1'	X(1)	'0'	'0'	'0'	'0'	'0'
Program failure due to V_{PP} Error	'1'	X(1)	'0'	'1'	'1'	'0'	'0'
Program failure due to Block Protection (FWH/LPC Interface only)	'1'	X(1)	'0'	'1'	'0'	'0'	'1'
Program failure due to cell failure	'1'	X(1))	'0'	'1'	'0'	'0'	'0'
Erase active	'0'	'0'	'0'	'0'	'0'	'0'	'0'
Erase suspended	'1'	'1'	'0'	'0'	'0'	'0'	'0'
Erase completed successfully	'1'	'0'	'0'	'0'	'0'	'0'	'0'
Erase failure due to V_{PP} Error	'1'	'0'	'1'	'0'	'1'	'0'	'0'
Erase failure due to Block Protection (FWH/LPC Interface only)	'1'	'0'	'1'	'0'	'0'	'0'	'1'
Erase failure due to failed cell(s) in block	'1'	'0'	'1'	'0'	'0'	'0'	'0'

1. For Program operations during Erase Suspend Bit SR6 is '1', otherwise Bit SR6 is '0'.

6 Firmware hub/low pin count (FWH/LPC) interface Configuration Registers

When the Firmware Hub Interface/Low Pin Count is selected, several additional registers can be accessed. These registers control the protection status of the Blocks, read the General Purpose Input pins and identify the memory using the manufacturer code. See *Table 15* for the memory map of the Configuration Registers. The Configuration registers are accessed directly without using any specific command code. A single Bus Write or Bus Read Operation, with the appropriate address (including A22=0), is all that is needed.

6.1 Lock Registers

The Lock Registers control the protection status of the Blocks. Each Block has its own Lock Register. Three bits within each Lock Register control the protection of each block: the Write Lock Bit, the Read Lock Bit and the Lock Down Bit.

The Lock Registers can be read and written. Care should be taken, though, when writing. Once the Lock Down Bit is set, ‘1’, further modifications to the Lock Register cannot be made until it is cleared again by a reset or power-up.

See *Table 16* for details on the bit definitions of the Lock Registers.

6.1.1 Write Lock

The Write Lock Bit determines whether the contents of the Block can be modified (using the Program or Erase Command). When the Write Lock Bit is set, ‘1’, the block is write protected – any operations that attempt to change the data in the block will fail, and the Status Register will report the error. When the Write Lock Bit is reset, ‘0’, the block is not write protected by the Lock Register, and may be modified, unless it is write protected by some other means.

If the Top Block Lock signal, $\overline{TBL}$, is Low, V_{IL}, then the Top Block (Block 7) is write protected, and cannot be modified. Similarly, if the Write Protect signal, $\overline{WP}$, is Low, V_{IL}, then the Main Blocks (Blocks 0 to 6) are write protected, and cannot be modified.

After power-up, or reset, the Write Lock Bit is always set to ‘1’ (write-protected).

6.1.2 Read Lock

The Read Lock bit determines whether the contents of the Block can be read (in Read mode). When the Read Lock Bit is set, ‘1’, the block is read protected – any operation that attempts to read the contents of the block will read 00h instead. When the Read Lock Bit is reset, ‘0’, read operations are allowed in the Block, and return the value of the data that had been programmed in the block.

After power-up, or reset, the Read Lock Bit is always reset to ‘0’ (not read-protected).

6.1.3 Lock Down

The Lock Down Bit provides a mechanism for protecting software data from simple hacking and malicious attack. When the Lock Down Bit is set, '1', further modification to the Write Lock, Read Lock and Lock Down Bits cannot be performed. A reset, or power-up, is required before changes to these bits can be made. When the Lock Down Bit is reset, '0', the Write Lock, Read Lock and Lock Down Bits can be changed.

Table 15. Configuration Register map

Mnemonic	Register Name	Memory Address	Default Value	Access
Lock Registers (For details, see *Appendix A*)				
GPI_REG	Firmware Hub/Low Pin Count (FWH/LPC) General Purpose Input Register	FBC0100h	N/A	R
MANU_REG	Manufacturer Code Register	FBC0000h	20h	R

1. In LPC mode, a most significant nibble, F, must be added to the memory address. For all registers, A22=0, and the remaining address bits should be set according to the rules shown in the ADDR field of *Table 6* to *Table 9*.

Table 16. Lock Register bit definitions

Bit	Bit Name	Value	Function(1)
7-3			Reserved
2	Read-Lock	'1'	Bus Read operations in this Block always return 00h.
		'0'	Bus read operations in this Block return the Memory Array contents. (Default value).
1	Lock-Down	'1'	Changes to the Read-Lock bit and the Write-Lock bit cannot be performed. Once a '1' is written to the Lock-Down bit it cannot be cleared to '0'; the bit is always reset to '0' following a Reset (using $\overline{RP}$ or $\overline{INIT}$) or after power-up.
		'0'	Read-Lock and Write-Lock can be changed by writing new values to them. (Default value).
0	Write-Lock	'1'	Program and Erase operations in this Block will set an error in the Status Register. The memory contents will not be changed. (Default value).
		'0'	Program and Erase operations in this Block are executed and will modify the Block contents.

1. Applies to Top Block Lock Register (T_BLOCK_LK) and Top Block [-1] Lock Register (T_MINUS01_LK) to Top Block [-7] Lock Register (T_MINUS07_LK).

Table 17. General-Purpose Input Register definition

Bit	Bit Name	Value	Function(1)
7-5			Reserved
4	GPI4	'1'	Input Pin GPI4 is at V_{IH}
		'0'	Input Pin GPI4 is at V_{IL}
3	GPI3	'1'	Input Pin GPI3 is at V_{IH}
		'0'	Input Pin GPI3 is at V_{IL}
2	GPI2	'1'	Input Pin GPI2 is at V_{IH}
		'0'	Input Pin GPI2 is at V_{IL}
1	GPI1	'1'	Input Pin GPI1 is at V_{IH}
		'0'	Input Pin GPI1 is at V_{IL}
0	GPI0	'1'	Input Pin GPI0 is at V_{IH}
		'0'	Input Pin GPI0 is at V_{IL}

1. Applies to the General Purpose Inputs Register (GPI-REG).

6.2 Firmware hub/low-pin count (FWH/LPC) General-Purpose Input Register

The FWH/LPC General Purpose Input Register holds the state of the General Purpose Input pins, GPI0-GPI4. When this register is read, the state of these pins is returned. This register is read-only. Writing to it has no effect.

The signals on the FWH/LPC Interface General Purpose Input pins should remain constant throughout the whole Bus Read cycle.

6.3 Manufacturer Code Register

Reading the Manufacturer Code Register returns the value 20h, which is the Manufacturer Code for STMicroelectronics. This register is read-only. Writing to it has no effect.

7 Program and Erase times

The Program and Erase times are shown in *Table 18*.

Table 18. Program and Erase times

Parameter	Interface	Test Condition	Min	Typ(1)	Max	Unit
Byte Program				10	200	µs
Double Byte Program	FWH	V_{PP} = 12 V ± 5%		10(2)	200	µs
Quadruple Byte Program	A/A Multiplexed FWH	V_{PP} = 12 V ± 5%		10(3)	200	µs
Block Program		V_{PP} = 12 V ± 5%		0.1(4)	5	s
		V_{PP} = V_{CC}		0.4	5	
Sector Erase (4 KBytes)(5)		V_{PP} = 12 V ± 5%		0.4	4	s
		V_{PP} = V_{CC}		0.5	5	
Block Erase (64 KBytes)		V_{PP} = 12 V ± 5%		0.75	8	s
		V_{PP} = V_{CC}		1	10	
Chip Erase	A/A Multiplexed	V_{PP} = 12 V ± 5%		5		s
Program/Erase Suspend to Program pause(5)					5	µs
Program/Erase Suspend to Block Erase/Sector Erase pause(5)					30	µs

1. T_A = 25°C, V_{CC} = 3.3V
2. Time to program two Bytes.
3. Time to program four Bytes.
4. Time obtained executing the Quadruple Byte Program command.
5. Sampled only, not 100% tested.

8 Maximum rating

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 19. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_{STG}	Storage Temperature	–65	150	°C
V_{IO}	Input or Output range (1)	–0.50	V_{CC} + 0.6	V
V_{CC}	Supply Voltage	–0.50	4	V
V_{PP}	Program Voltage	–0.6	13	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)(2)	–2000	2000	V

1. Minimum voltage may undershoot to –2 V for less than 20ns during transitions. Maximum voltage may overshoot to V_{CC} + 2 V for less than 20 ns during transitions.
2. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω)

9 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in *Table 20*, *Table 21* and *Table 22*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 20. Operating conditions

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.6	V
T_A	Ambient Operating Temperature (Device Grade 5)	–20	85	°C

Table 21. FWH/LPC interface AC measurement conditions

Parameter	Value	Unit
Load Capacitance (C_L)	10	pF
Input Rise and Fall Times	≤1.4	ns
Input Pulse Voltages	0.2 V_{CC} and 0.6 V_{CC}	V
Input and Output Timing Ref. Voltages	0.4 V_{CC}	V

Table 22. A/A Mux interface AC measurement conditions

Parameter	Value	Unit
Load Capacitance (C_L)	30	pF
Input Rise and Fall Times	≤10	ns
Input Pulse Voltages	0 to 3	V
Input and Output Timing Ref. Voltages	1.5	V

Figure 10. FWH/LPC interface AC measurement I/O waveforms

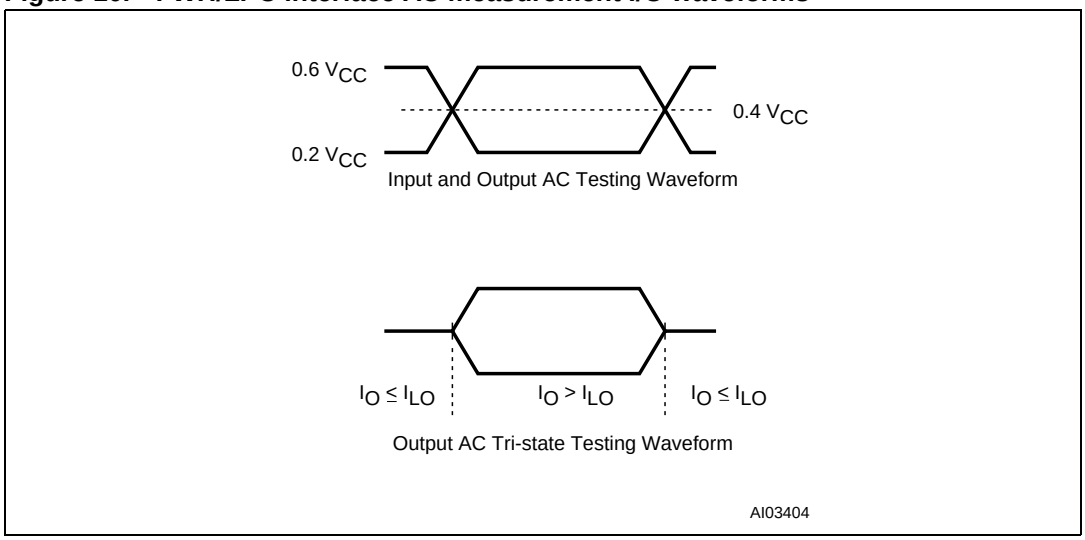


Figure 11. A/A Mux interface AC measurement I/O waveform

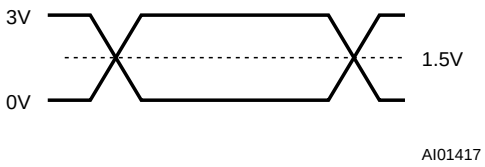


Figure 12. AC measurement load circuit

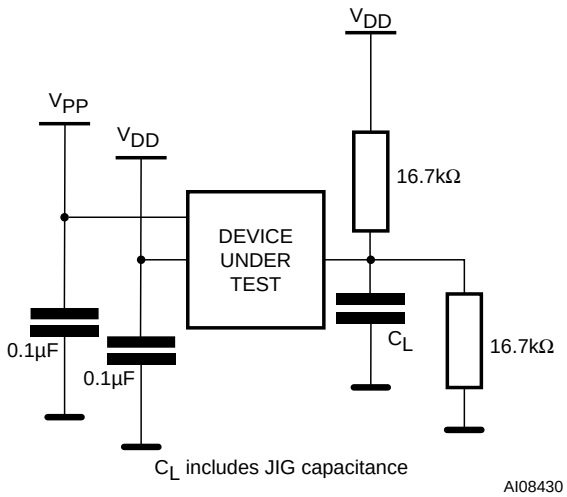


Table 23. Impedance(1)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}(2)	Input Capacitance	V_{IN} = 0V		13	pF
C_{CLK}(2)	Clock Capacitance	V_{IN} = 0V	3	12	pF
L_{PIN}(3)	Recommended Pin Inductance			20	nH

1. T_A = 25°C, f = 1MHz.
2. Sampled only, not 100% tested.
3. See PCI Specification.

Table 24. DC characteristics

Symbol	Parameter	Interface	Test Condition	Min	Max	Unit
V_{IH}	Input High Voltage	FWH		0.5 V_{CC}	V_{CC} + 0.5	V
		A/A Mux		0.7 V_{CC}	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	FWH/LPC		–0.5	0.3 V_{CC}	V
		A/A Mux		-0.5	0.8	V
$V_{IH}(\overline{INIT})$	$\overline{INIT}$ Input High Voltage	FWH/LPC		1.1	V_{CC} + 0.5	V
$V_{IL}(\overline{INIT})$	$\overline{INIT}$ Input Low Voltage	FWH/LPC		–0.5	0.2 V_{CC}	V
I_{LI}(1)	Input Leakage Current		0 V ≤V_{IN} ≤V_{CC}		±10	µA
I_{LI2}	IC, IDx Input Leakage Current		IC, ID0, ID1, ID2, ID3(2) = V_{CC}		200	µA
R_{IL}	IC, IDx Input Pull Low Resistor			20	100	kΩ
V_{OH}	Output High Voltage	FWH/LPC	I_{OH} = –500 µA	0.9 V_{CC}		V
		A/A Mux	I_{OH} = –100 µA	V_{CC} – 0.4		V
V_{OL}	Output Low Voltage	FWH/LPC	I_{OL} = 1.5 mA		0.1 V_{CC}	V
		A/A Mux	I_{OL} = 1.8 mA		0.45	V
I_{LO}	Output Leakage Current		0V ≤V_{OUT} ≤V_{CC}		±10	µA
V_{PP1}	V_{PP} Voltage			3	3.6	V
V_{PPH}	V_{PP} Voltage (Fast Erase)			11.4	12.6	V
V_{LKO}(3)	V_{CC} Lockout Voltage			1.8	2.3	V
I_{CC1}	Supply Current (Standby)	FWH/LPC	FWH4/$\overline{LFRAME}$ = 0.9V_{CC} V_{PP} = V_{CC} All other inputs 0.9V_{CC} to 0.1V_{CC} V_{CC} = 3.6 V, f(CLK) = 33 MHz		100	µA
I_{CC2}	Supply Current (Standby)	FWH/LPC	FWH4/$\overline{LFRAME}$ = 0.1 V_{CC}, V_{PP} = V_{CC} All other inputs 0.9 V_{CC} to 0.1 V_{CC} V_{CC} = 3.6 V, f(CLK) = 33 MHz		10	mA
I_{CC3}	Supply Current (Any internal operation active)	FWH/LPC	V_{CC} = V_{CC} max, V_{PP} = V_{CC} f(CLK) = 33 MHz I_{OUT} = 0 mA		60	mA
I_{CC4}	Supply Current (Read)	A/A Mux	$\overline{G}$ = V_{IH}, f = 6 MHz		20	mA
I_{CC5}(3)	Supply Current (Program/Erase)	A/A Mux	Program/Erase Controller Active		20	mA

Table 24. DC characteristics (continued)

Symbol	Parameter	Interface	Test Condition	Min	Max	Unit
I_{PP}	V_{PP} Supply Current (Read/Standby)		$V_{PP} \geq V_{CC}$		400	µA
I_{PP1}(3)	V_{PP} Supply Current (Program/Erase active)		$V_{PP} = V_{CC}$		40	mA
			V_{PP} = 12 V ± 5%		15	mA

1. Input leakage currents include High-Z output leakage for all bidirectional buffers with three-state outputs.
2. ID3 pin is RFU in LPC mode.
3. Sampled only, not 100% tested.

Figure 13. FWH/LPC interface clock waveform

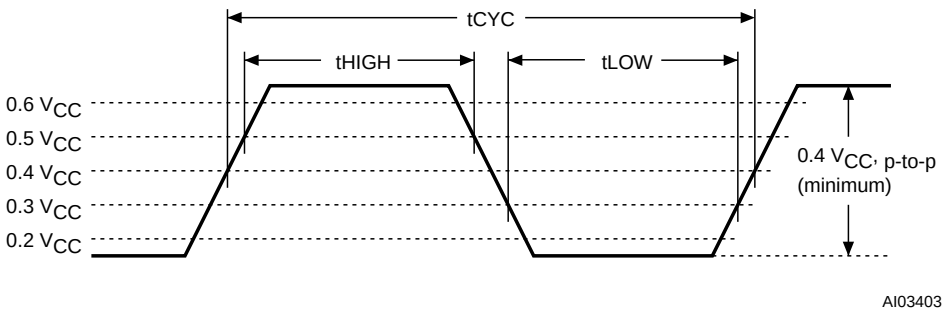


Table 25. FWH/LPC interface clock characteristics

Symbol	Parameter	Test Condition		Value	Unit
t_{CYC}	CLK Cycle Time(1)		Min	30	ns
t_{HIGH}	CLK High Time		Min	11	ns
t_{LOW}	CLK Low Time		Min	11	ns
	CLK Slew Rate	peak to peak	Min	1	V/ns
			Max	4	V/ns

1. Devices on the PCI Bus must work with any clock frequency between DC and 33MHz. Below 16MHz devices may be guaranteed by design rather than tested. Refer to PCI Specification.

Figure 14. FWH/LPC interface AC signal timing waveforms

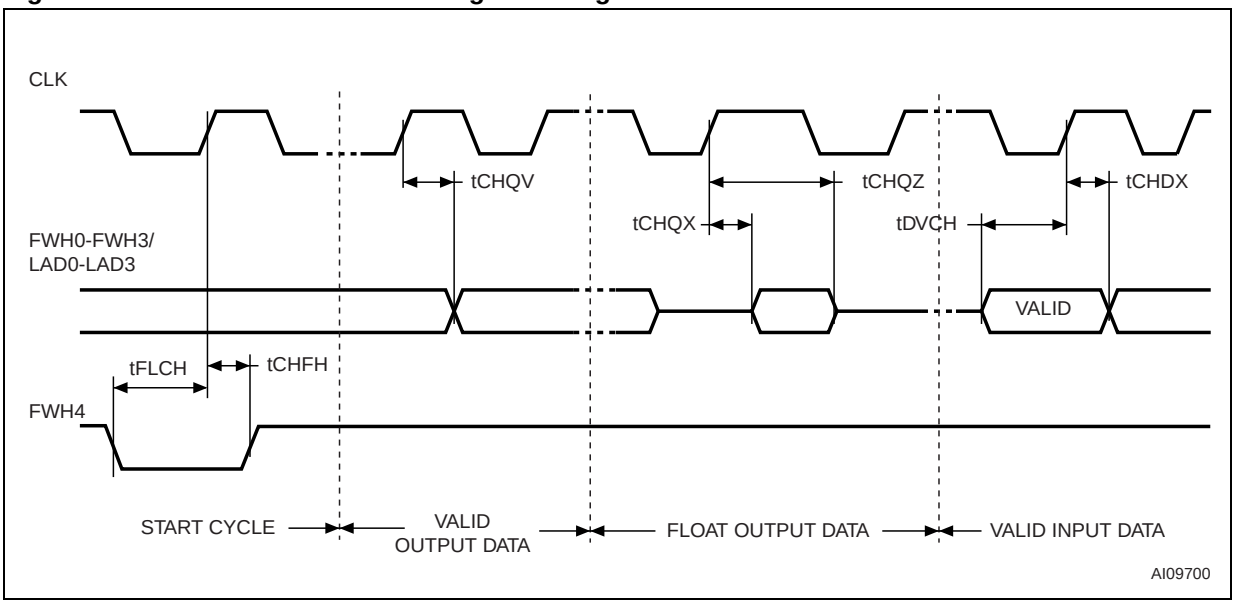


Table 26. FWH/LPC interface AC signal timing characteristics

Symbol	PCI Symbol	Parameter		Value	Unit
t_{CHQV}	t_{val}	CLK to Data Out	Min	2	ns
			Max	11	ns
t_{CHQX}(1)	t_{on}	CLK to Active (Float to Active Delay)	Min	2	ns
t_{CHQZ}	t_{off}	CLK to Inactive (Active to Float Delay)	Max	28	ns
t_{AVCH} t_{DVCH}	t_{su}	Input Set-up Time(2)	Min	7	ns
t_{CHAX} t_{CHDX}	t_h	Input Hold Time(2)	Min	0	ns
t_{FLCH}		Input Set-up time on FWH4	Min	10	ns
t_{CHFH}		Input Hold time on FWH4	Min	5	ns

1. The timing measurements for Active/Float transitions are defined when the current through the pin equals the leakage current specification.
2. Applies to all inputs except CLK and FWH4.

Figure 15. Reset AC waveforms

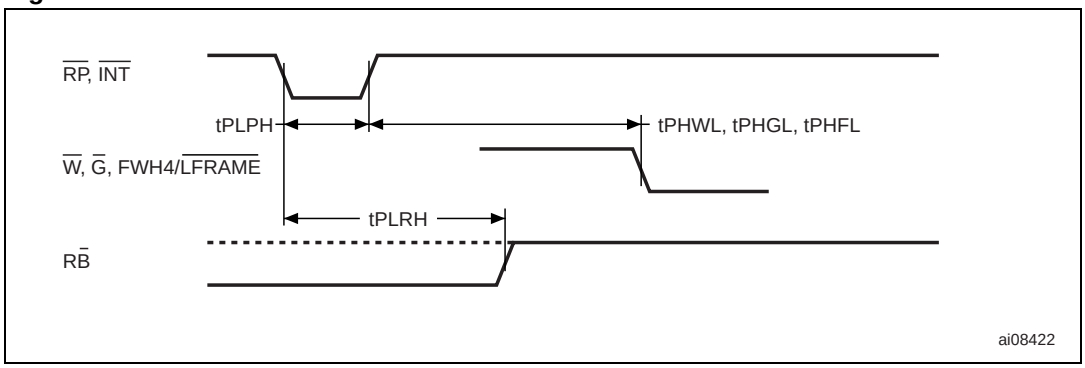


Table 27. Reset AC characteristics

Symbol	Parameter	Test Condition		Value	Unit
t_{PLPH}	RP or INIT Reset Pulse Width		Min	100	ns
t_{PLRH}	RP or INIT Low to Reset	Program/Erase Inactive	Max	100	ns
		Program/Erase Active	Max	30	µs
	RP or INIT Slew Rate(1)	Rising edge only	Min	50	mV/ns
t_{PHFL}	RP or INIT High to FWH4/LFRAME Low	FWH/LPC Interface only	Min	30	µs
t_{PHWL} t_{PHGL}	RP High to Write Enable or Output Enable Low	A/A Mux Interface only	Min	50	µs

1. See Chapter 4 of the PCI Specification.

Figure 16. A/A Mux interface Read AC waveforms

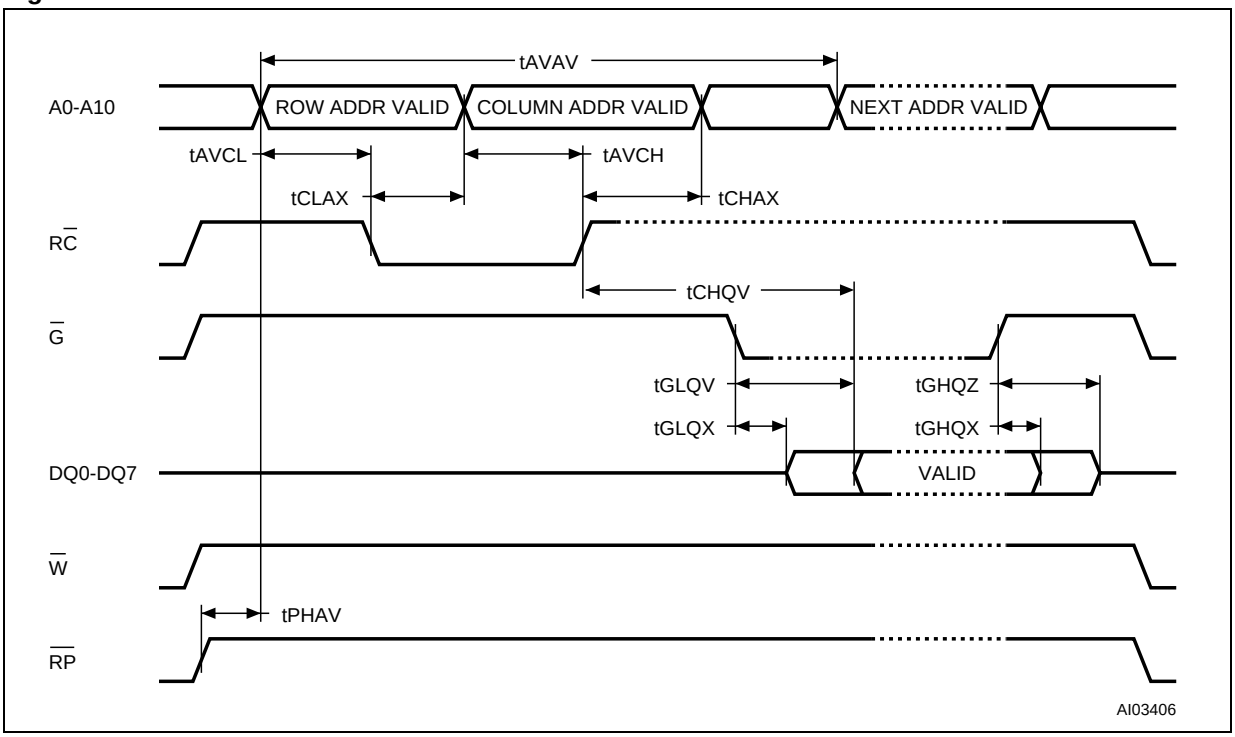


Table 28. A/A Mux interface Read AC characteristics

Symbol	Parameter	Test Condition		Value	Unit
t_{AVAV}	Read Cycle Time		Min	250	ns
t_{AVCL}	Row Address Valid to $\overline{RC}$ Low		Min	50	ns
t_{CLAX}	$\overline{RC}$ Low to Row Address Transition		Min	50	ns
t_{AVCH}	Column Address Valid to $\overline{RC}$ high		Min	50	ns
t_{CHAX}	$\overline{RC}$ High to Column Address Transition		Min	50	ns
t_{CHQV}(1)	$\overline{RC}$ High to Output Valid		Max	150	ns
t_{GLQV}(1)	Output Enable Low to Output Valid		Max	50	ns
t_{PHAV}	$\overline{RP}$ High to Row Address Valid		Min	1	µs
t_{GLQX}	Output Enable Low to Output Transition		Min	0	ns
t_{GHQZ}	Output Enable High to Output Hi-Z		Max	50	ns
t_{GHQX}	Output Hold from Output Enable High		Min	0	ns

1. $\overline{G}$ may be delayed up to $t_{CHQV} - t_{GLQV}$ after the rising edge of $\overline{RC}$ without impact on t_{CHQV}.

Figure 17. A/A Mux interface Write AC waveforms

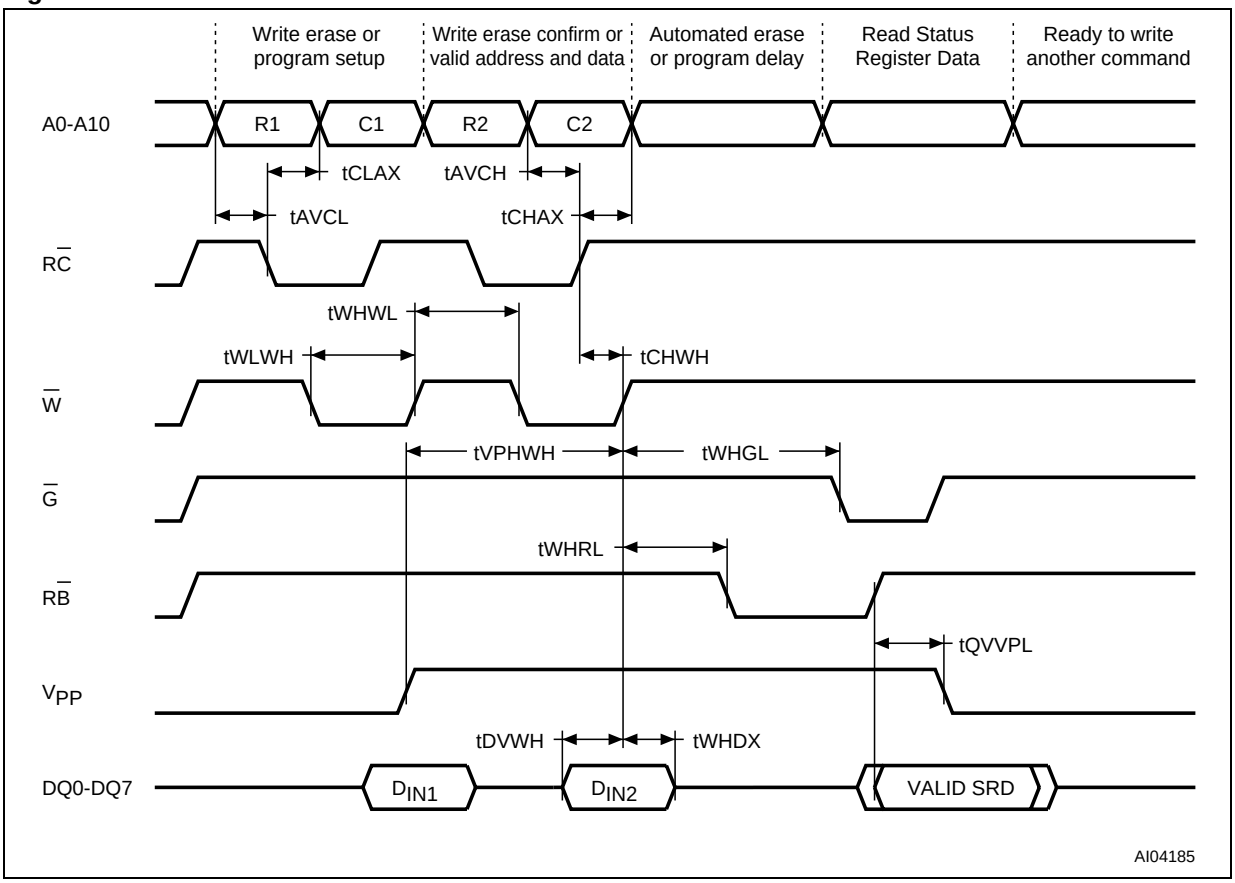


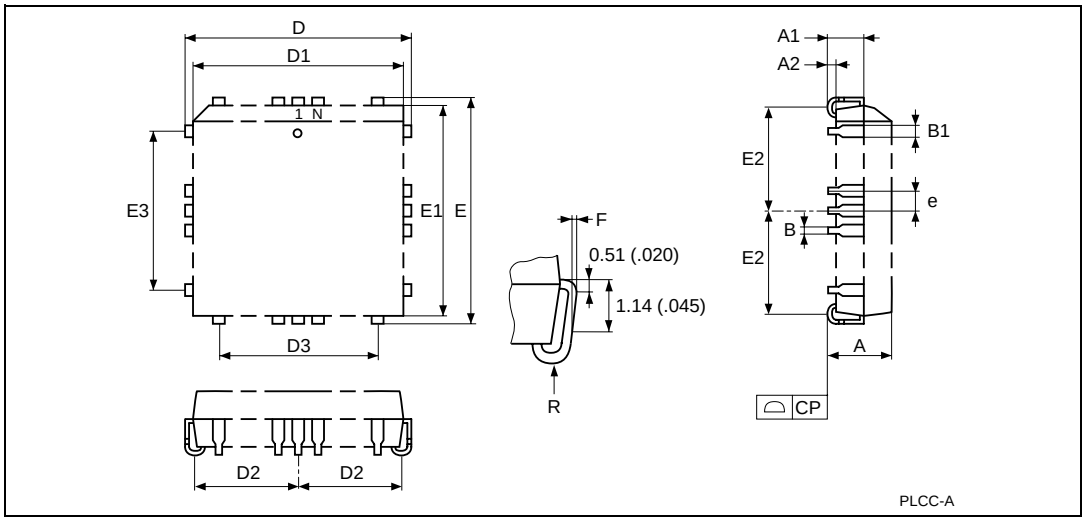
Table 29. A/A Mux interface Write AC characteristics

Symbol	Parameter	Test Condition		Value	Unit
t_{WLWH}	Write Enable Low to Write Enable High		Min	100	ns
t_{DVWH}	Data Valid to Write Enable High		Min	50	ns
t_{WHDX}	Write Enable High to Data Transition		Min	5	ns
t_{AVCL}	Row Address Valid to $\overline{RC}$ Low		Min	50	ns
t_{CLAX}	$\overline{RC}$ Low to Row Address Transition		Min	50	ns
t_{AVCH}	Column Address Valid to $\overline{RC}$ High		Min	50	ns
t_{CHAX}	$\overline{RC}$ High to Column Address Transition		Min	50	ns
t_{WHWL}	Write Enable High to Write Enable Low		Min	100	ns
t_{CHWH}	$\overline{RC}$ High to Write Enable High		Min	50	ns
t_{VPHWH}(1)	V_{PP} High to Write Enable High		Min	100	ns
t_{WHGL}	Write Enable High to Output Enable Low		Min	30	ns
t_{WHRL}	Write Enable High to $\overline{RB}$ Low		Min	0	ns
t_{QVVPL}(1),(2)	Output Valid, $\overline{RB}$ High to V_{PP} Low		Min	0	ns

1. Sampled only, not 100% tested.
2. Applicable if V_{PP} is seen as a logic input (V_{PP} < 3.6V).

10 Package mechanical

Figure 18. PLCC32 – 32 pin Rectangular Plastic Leaded Chip Carrier, package outline

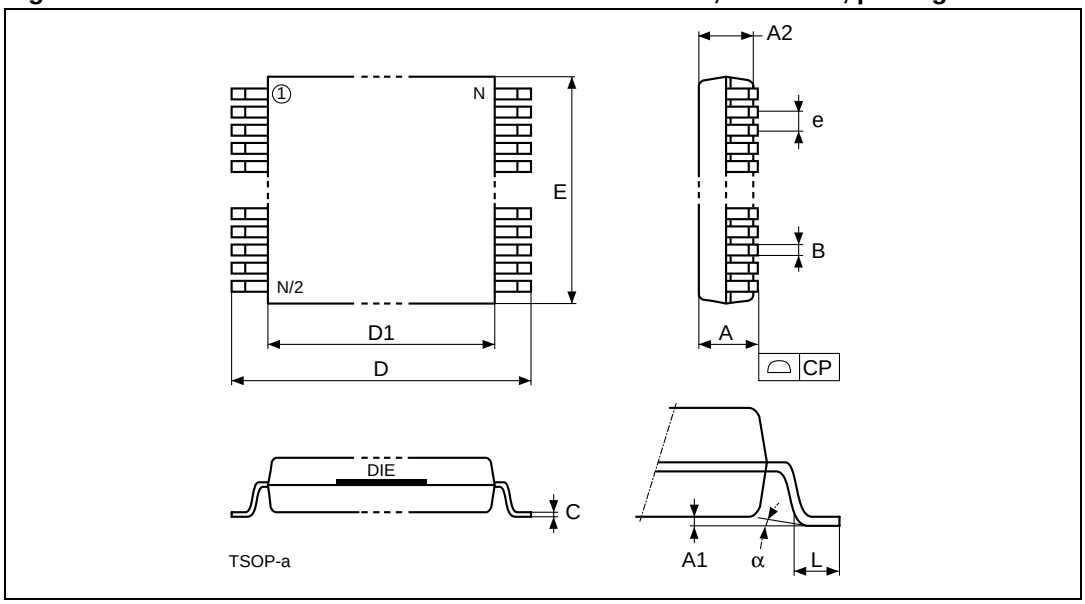


1. Drawing is not to scale.

Table 30. PLCC32 – 32 pin Rectangular Plastic Leaded Chip Carrier, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.18	3.56		0.125	0.140
A1		1.53	2.41		0.060	0.095
A2		0.38	–		0.015	–
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
CP			0.10			0.004
D		12.32	12.57		0.485	0.495
D1		11.35	11.51		0.447	0.453
D2		4.78	5.66		0.188	0.223
D3	7.62	–	–	0.300	–	–
E		14.86	15.11		0.585	0.595
E1		13.89	14.05		0.547	0.553
E2		6.05	6.93		0.238	0.273
E3	10.16	–	–	0.400	–	–
e	1.27	–	–	0.050	–	–
F		0.00	0.13		0.000	0.005
R	0.89	–	–	0.035	–	–
N	32			32		

Figure 19. TSOP32 – 32 lead Plastic Thin Small Outline, 8x14 mm, package outline



1. Drawing is not to scale.

Table 31. TSOP32 – 32 lead Plastic Thin Small Outline, 8x14 mm, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2		0.950	1.050		0.0374	0.0413
α		0°	5°		0°	5°
B		0.170	0.270		0.0067	0.0106
C		0.100	0.210		0.0039	0.0083
CP			0.100			0.0039
D		13.800	14.200		0.5433	0.5591
D1		12.300	12.500		0.4843	0.4921
e	0.500	–	–	0.0197	–	–
E		7.900	8.100		0.3110	0.3189
L		0.500	0.700		0.0197	0.0276
N	32			32		

Figure 20. TSOP40 – 40 lead Plastic Thin Small Outline, 10 x 20mm, package outline

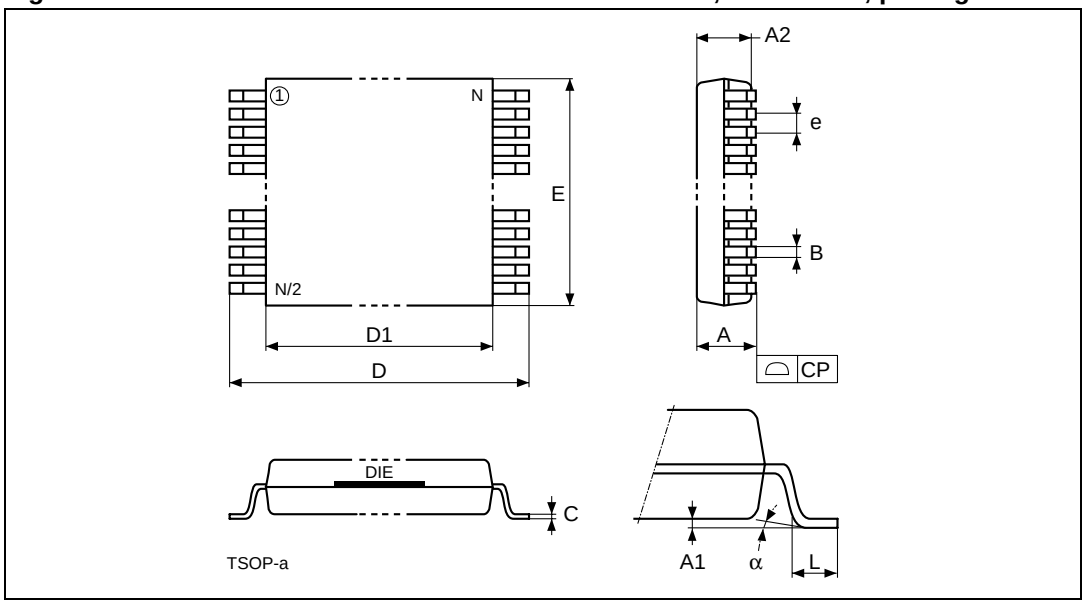


Table 32. TSOP40 – 40 lead Plastic Thin Small Outline, 10 x 20mm, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0
A1		0.050	0.150		0	0
A2		0.950	1.050		0	0
B		0.170	0.270		0	0
C		0.100	0.210		0	0
CP			0.100			0
D		19.800	20.200		1	1
D1		18.300	18.500		1	1
e	0.500	–	–	0	–	–
E		9.900	10.100		0	0
L		0.500	0.700		0	0
α		0°	5°		0°	5°
N	40			40		

11 Part numbering

Table 33. Ordering information scheme

Example: M50FLW040 A K 5 T P

Device Type

M50 = Flash Memory for PC BIOS

Architecture

FL = Firmware Hub/Low Pin Count Interface

Operating Voltage

W = V_{CC} = 3.0 to 3.6V

Device Function

040 = 4 Mbit (x8), Uniform Blocks and Sectors

Array Matrix

A = 2 x 16 x 4KByte top sectors + 1 x 16 x 4KByte bottom sectors

B = 1 x 16 x 4KByte top sectors + 2 x 16 x 4KByte bottom sectors(1)

Package

K = PLCC32

NB = TSOP32: 8 x 14mm(2)

N = TSOP40: 10 x 20 mm(2)

Device Grade

5 = Temperature range –20 to 85 °C.

Device tested with standard test flow

Option

blank = Standard Packing

T = Tape and Reel Packing

Plating Technology

P or G = ECOPACK® (RoHs compliant)

1. Devices with this architecture are Not Recommended for New Design.
2. Devices delivered in this package are Not Recommended for New Design.

Devices are shipped from the factory with the memory content bits erased to ’1’.

For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

The category of second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

Appendix A Block and sector address table

Table 34. M50FLW040A block and sector addresses(1)

Block Size (KByte)	Address Range	Block No and Type	Sector Size (KByte)	Sector No	Register Address
64	7F000h-7FFFFh	7 (Top)	4	47	FBF0002
	7E000h-7EFFFh		4	46	
	7D000h-7DFFFh		4	45	
	7C000h-7CFFFh		4	44	
	7B000h-7BFFFh		4	43	
	7A000h-7AFFFh		4	42	
	79000h-79FFFh		4	41	
	78000h-78FFFh		4	40	
	77000h-77FFFh		4	39	
	76000h-76FFFh		4	38	
	75000h-75FFFh		4	37	
	74000h-74FFFh		4	36	
	73000h-73FFFh		4	35	
	72000h-72FFFh		4	34	
	71000h-71FFFh		4	33	
	70000h-70FFFh		4	32	
64	6F000h-6FFFFh	6 (Main)	4	31	FBE0002
	6E000h-6EFFFh		4	30	
	6D000h-6DFFFh		4	29	
	6C000h-6CFFFh		4	28	
	6B000h-6BFFFh		4	27	
	6A000h-6AFFFh		4	26	
	69000h-69FFFh		4	25	
	68000h-68FFFh		4	24	
	67000h-67FFFh		4	23	
	66000h-66FFFh		4	22	
	65000h-65FFFh		4	21	
	64000h-64FFFh		4	20	
	63000h-63FFFh		4	19	
	62000h-62FFFh		4	18	
	61000h-61FFFh		4	17	
	60000h-60FFFh		4	16	

Table 34. M50FLW040A block and sector addresses(1) (continued)

Block Size (KByte)	Address Range	Block No and Type	Sector Size (KByte)	Sector No	Register Address
64	50000h- 5FFFFh	5 (Main)			FBD0002
64	40000h- 4FFFFh	4 (Main)			FBC0002
64	30000h-3FFFFh	3 (Main)			FBB0002
64	20000h-2FFFFh	2 (Main)			FBA0002
64	10000h-1FFFFh	1 (Main)			FB90002
64	0F000h-0FFFFh	0 (Main)	4	15	FB80002
	0E000h-0EFFFh		4	14	
	0D000h-0DFFFh		4	13	
	0C000h-0CFFFh		4	12	
	0B000h-0BFFFh		4	11	
	0A000h-0AFFFh		4	10	
	09000h-09FFFh		4	9	
	08000h-08FFFh		4	8	
	07000h-07FFFh		4	7	
	06000h-06FFFh		4	6	
	05000h-05FFFh		4	5	
	04000h-04FFFh		4	4	
	03000h-03FFFh		4	3	
	02000h-02FFFh		4	2	
	01000h-01FFFh		4	1	
	00000h-00FFFh		4	0	

1. In LPC mode, a most significant nibble, F, must be added to the memory address. For all registers, A22=0, and the remaining address bits should be set according to the rules shown in the ADDR field of *Table 6* to *Table 9*.

Table 35. M50FLW040B block and sector addresses[1]

Block Size (KByte)	Address Range	Block No and Type	Sector Size (KByte)	Sector No	Register Address
64	7F000h-7FFFFh	7 (Top)	4	47	FBF0002
	7E000h-7EFFFh		4	46	
	7D000h-7DFFFh		4	45	
	7C000h-7CFFFh		4	44	
	7B000h-7BFFFh		4	43	
	7A000h-7AFFFh		4	42	
	79000h-79FFFh		4	41	
	78000h-78FFFh		4	40	
	77000h-77FFFh		4	39	
	76000h-76FFFh		4	38	
	75000h-75FFFh		4	37	
	74000h-74FFFh		4	36	
	73000h-73FFFh		4	35	
	72000h-72FFFh		4	34	
	71000h-71FFFh		4	33	
	70000h-70FFFh		4	32	
64	60000h- 6FFFFh	6 (Main)			FBE0002
64	50000h- 5FFFFh	5 (Main)			FBD0002
64	40000h-4FFFFh	4 (Main)			FBC0002
64	30000h-3FFFFh	3 (Main)			FBB0002
64	20000h-2FFFFh	2 (Main)			FBA0002

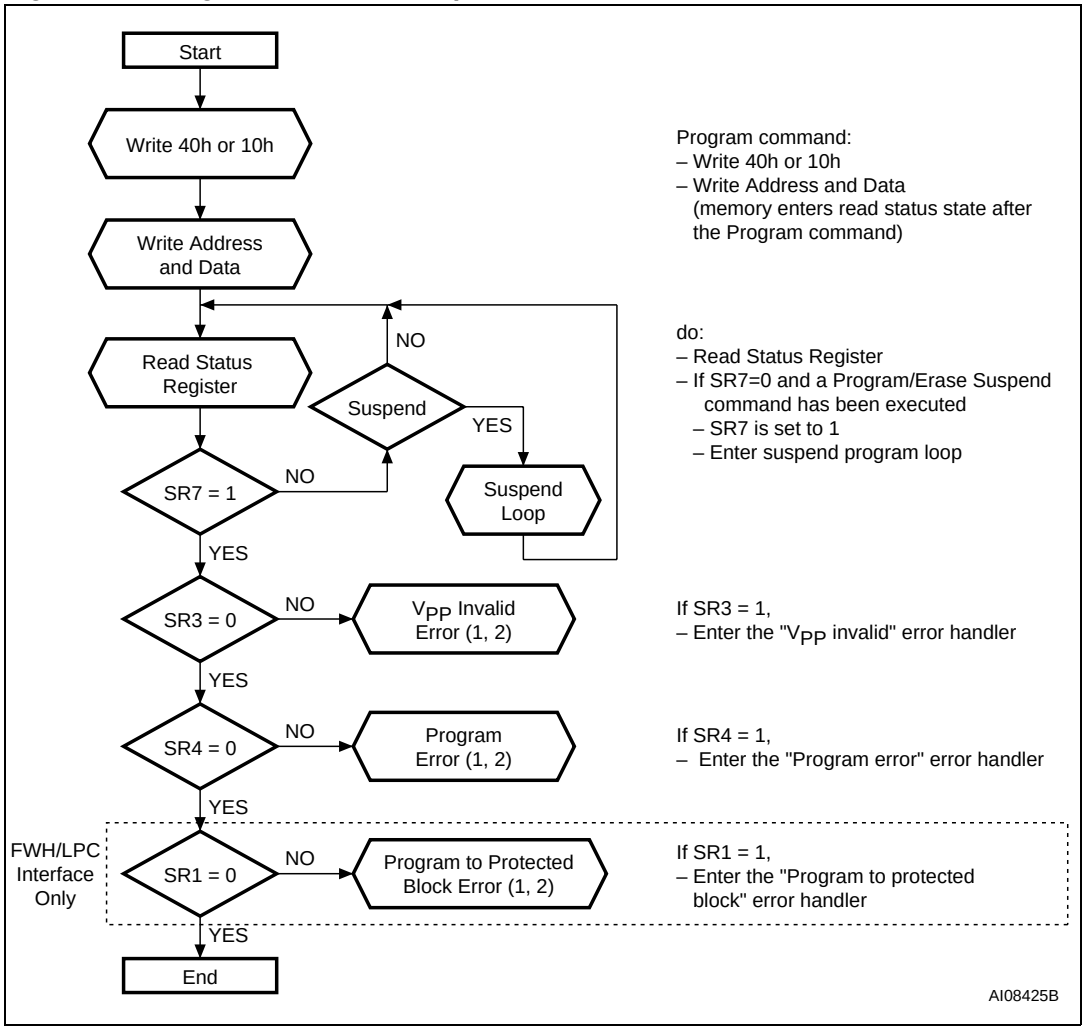
Table 35. M50FLW040B block and sector addresses[1] (continued)

Block Size (KByte)	Address Range	Block No and Type	Sector Size (KByte)	Sector No	Register Address
64	1F000h-1FFFFh	1 (Main)	4	31	FB90002
	1E000h-1EFFFh		4	30	
	1D000h-1DFFFh		4	29	
	1C000h-1CFFFh		4	28	
	1B000h-1BFFFh		4	27	
	1A000h-1AFFFh		4	26	
	19000h-19FFFh		4	25	
	18000h-18FFFh		4	24	
	17000h-17FFFh		4	23	
	16000h-16FFFh		4	22	
	15000h-15FFFh		4	21	
	14000h-14FFFh		4	20	
	13000h-13FFFh		4	19	
	12000h-12FFFh		4	18	
	11000h-11FFFh		4	17	
	10000h-10FFFh		4	16	
64	0F000h-0FFFFh	0 (Main)	4	15	FB80002
	0E000h-0EFFFh		4	14	
	0D000h-0DFFFh		4	13	
	0C000h-0CFFFh		4	12	
	0B000h-0BFFFh		4	11	
	0A000h-0AFFFh		4	10	
	09000h-09FFFh		4	9	
	08000h-08FFFh		4	8	
	07000h-07FFFh		4	7	
	06000h-06FFFh		4	6	
	05000h-05FFFh		4	5	
	04000h-04FFFh		4	4	
	03000h-03FFFh		4	3	
	02000h-02FFFh		4	2	
	01000h-01FFFh		4	1	
	00000h-00FFFh		4	0	

1. In LPC mode, a most significant nibble, F, must be added to the memory address. For all registers, A22=0, and the remaining address bits should be set according to the rules shown in the ADDR field of *Table 6* to *Table 9*.

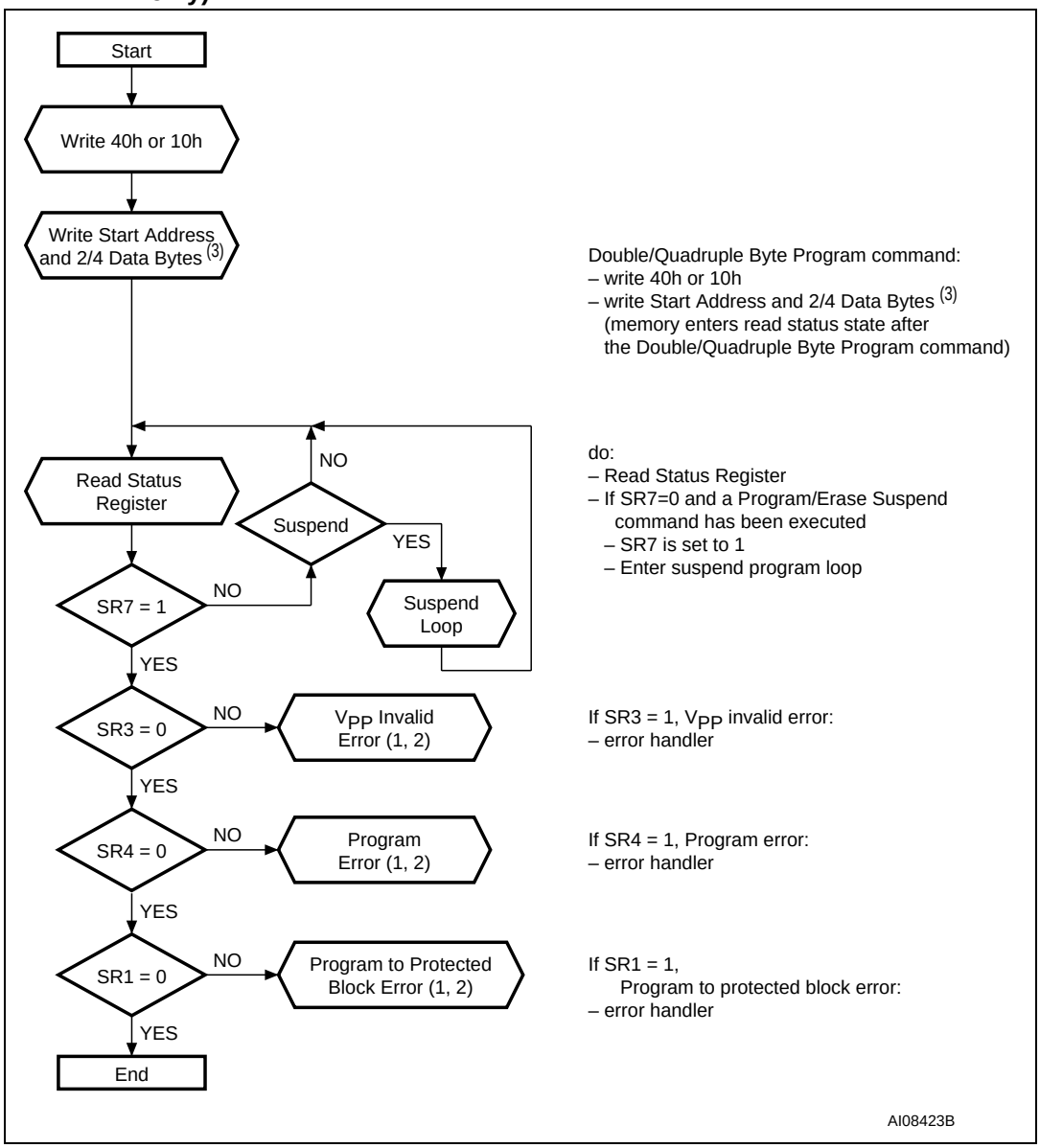
Appendix B Flowcharts and pseudo codes

Figure 21. Program flowchart and pseudo code



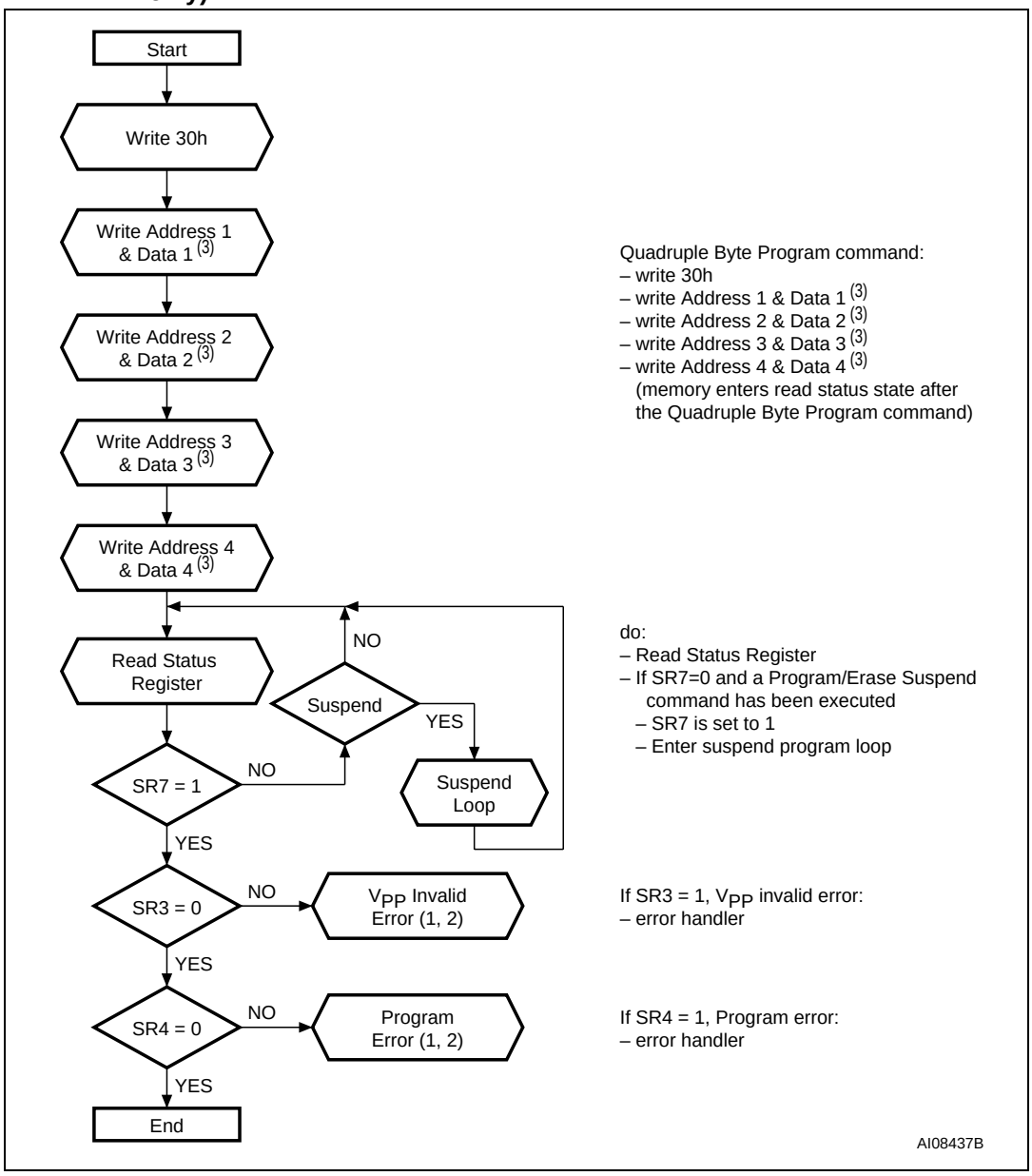
1. A Status check of SR1 (Protected Block), SR3 (V_{PP} invalid) and SR4 (Program Error) can be made after each Program operation by following the correct command sequence.
2. If an error is found, the Status Register must be cleared before further Program/Erase Controller operations.

Figure 22. Double/Quadruple Byte Program flowchart and pseudo code (FWH mode only)



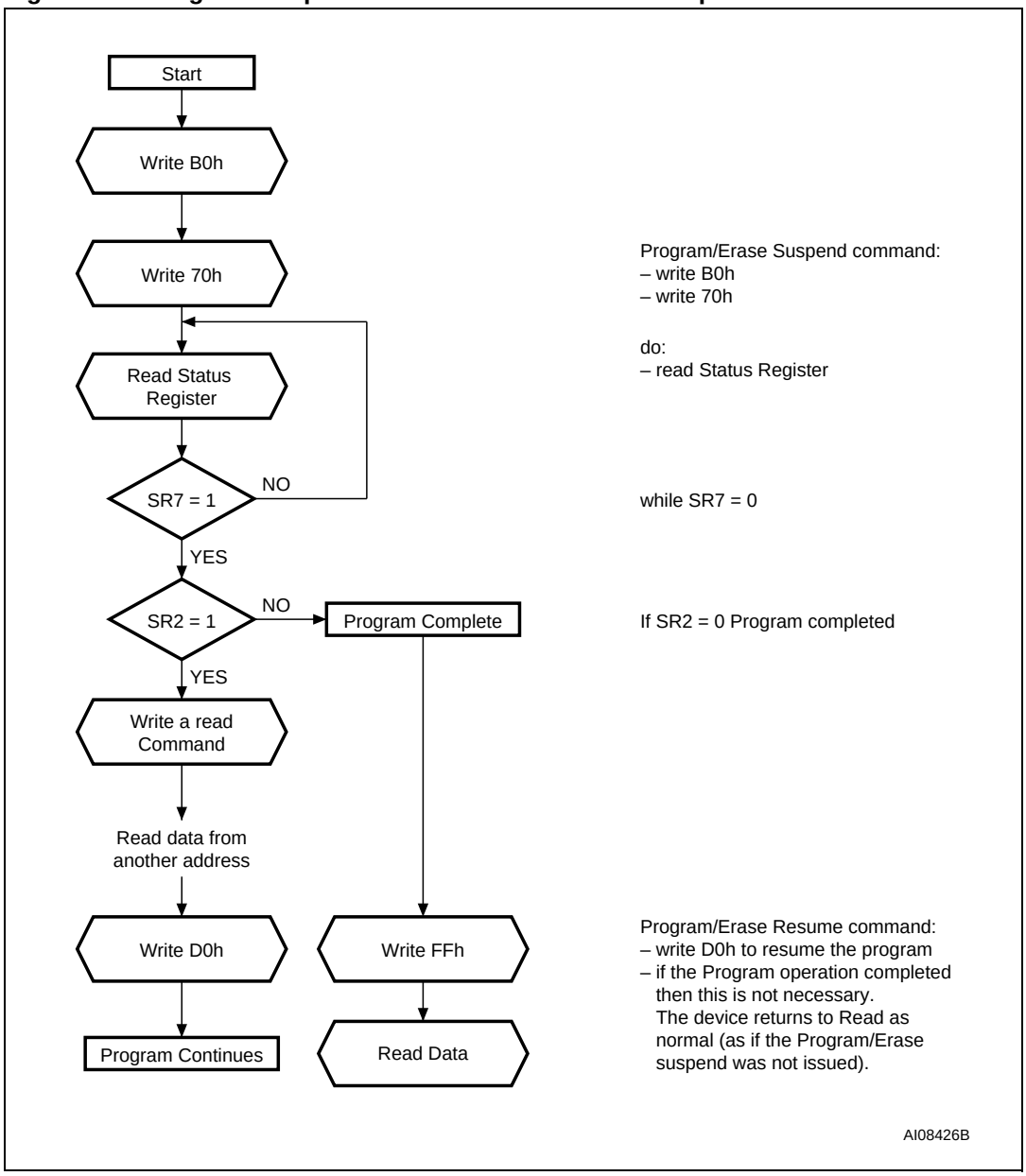
1. A Status check of SR3 (V_{PP} Invalid) and SR4 (Program Error) can be made after each program operation by following the correct command sequence.
2. If an error is found, the Status Register must be cleared before further Program/Erase operations.
3. A0 and/or A1 are treated as Don't Care (A0 for Double Byte Program and A1-A0 for Quadruple Byte Program).
For Double Byte Program: Starting at the Start Address, the first data Byte is programmed at the even address, and the second at the odd address.
For Quadruple Byte Program: Starting at the Start Address, the first data Byte is programmed at the address that has A1-A0 at 00, the second at the address that has A1-A0 at 01, the third at the address that has A1-A0 at 10, and the fourth at the address that has A1-A0 at 11.

Figure 23. Quadruple Byte Program flowchart and pseudo code (A/A Mux interface only)



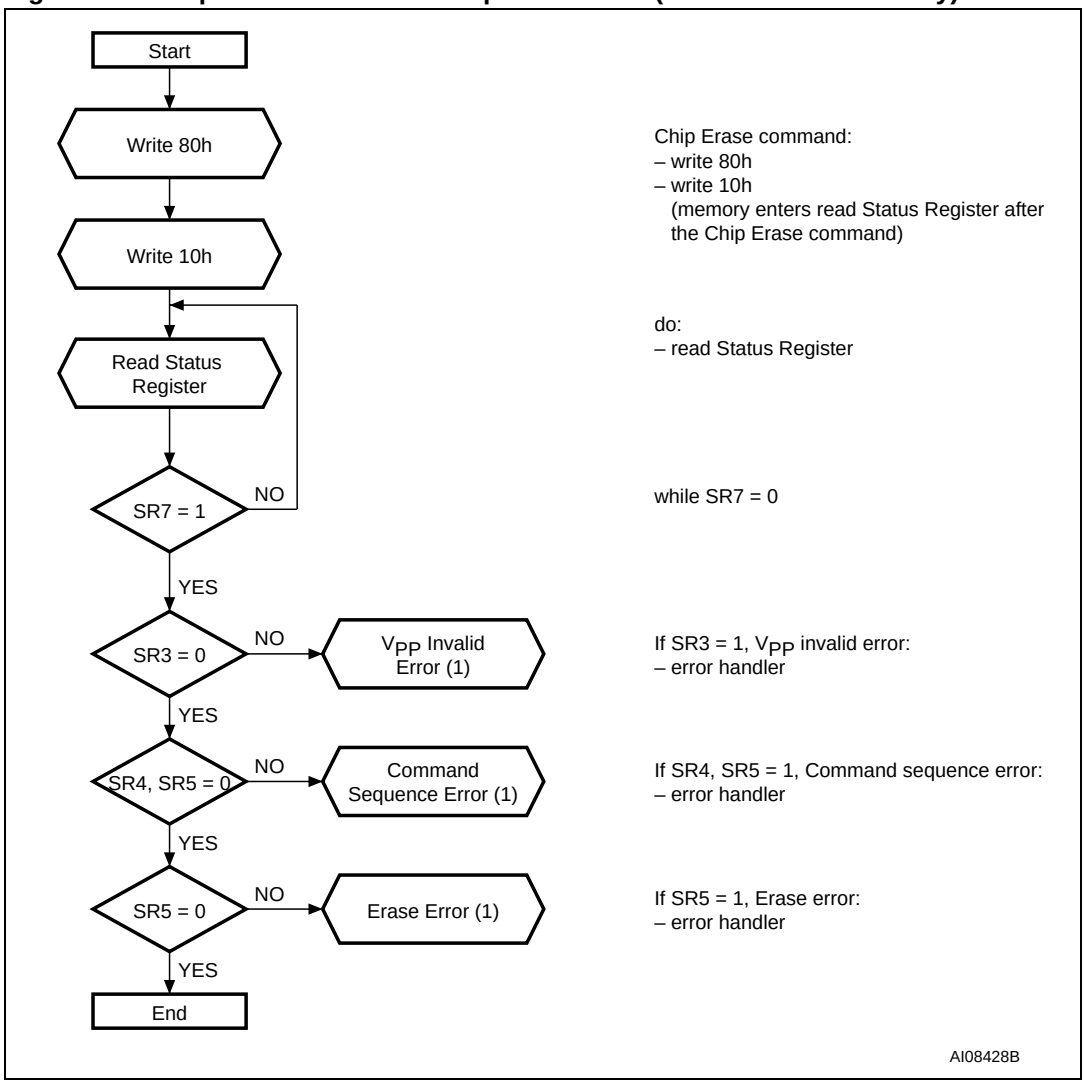
1. A Status check of SR3 (V_{PP} invalid) and SR4 (Program Error) can be made after each Program operation by following the correct command sequence.
2. If an error is found, the Status Register must be cleared before further Program/Erase Controller operations.
3. Address1, Address 2, Address 3 and Address 4 must be consecutive addresses differing only for address bits A0 and A1.

Figure 24. Program Suspend and Resume flowchart and pseudo code



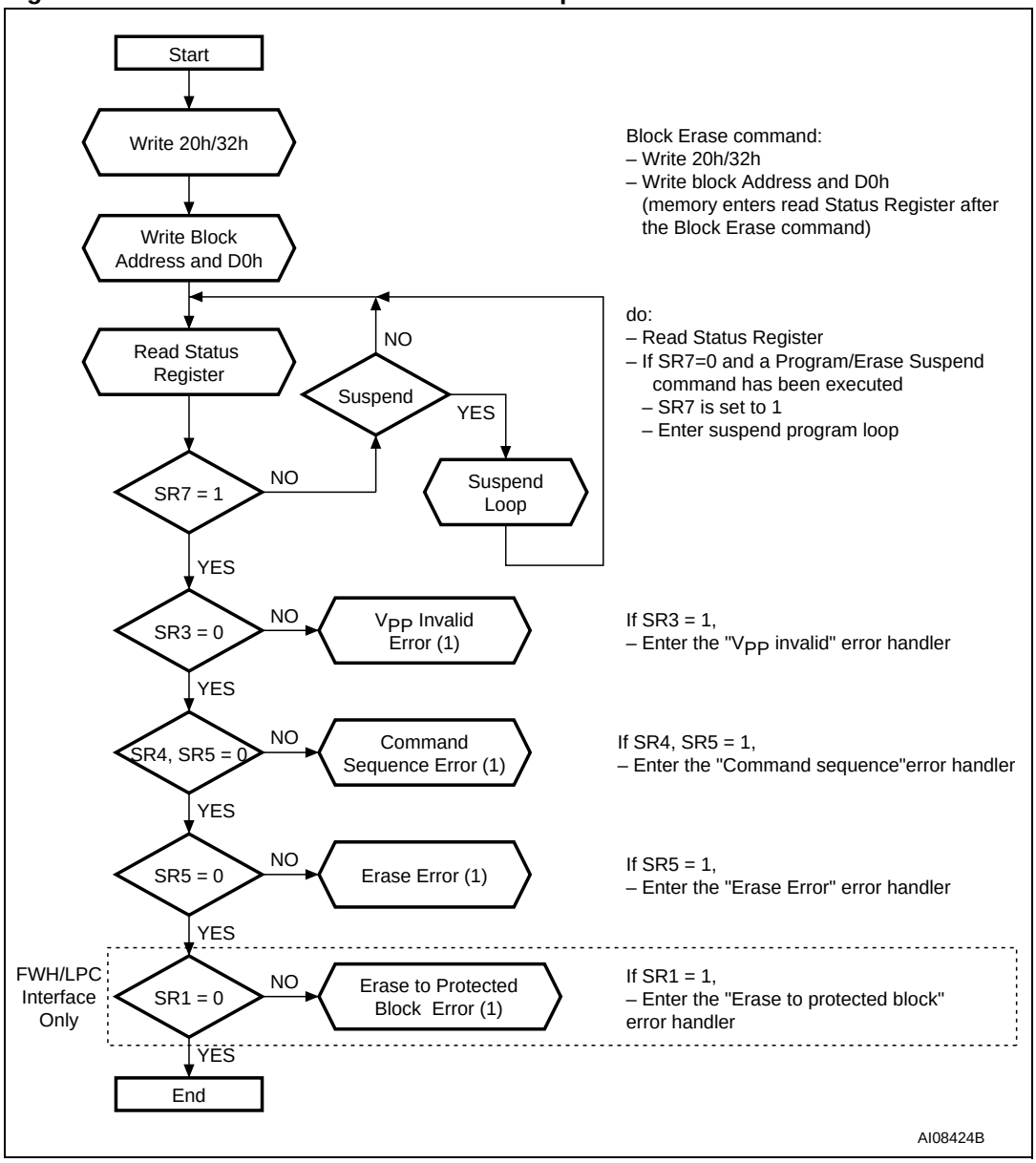
1. If an error is found, the Status Register must be cleared before further Program/Erase operations.
2. Any address within the bank can equally be used.

Figure 25. Chip Erase flowchart and pseudo code (A/A Mux interface only)



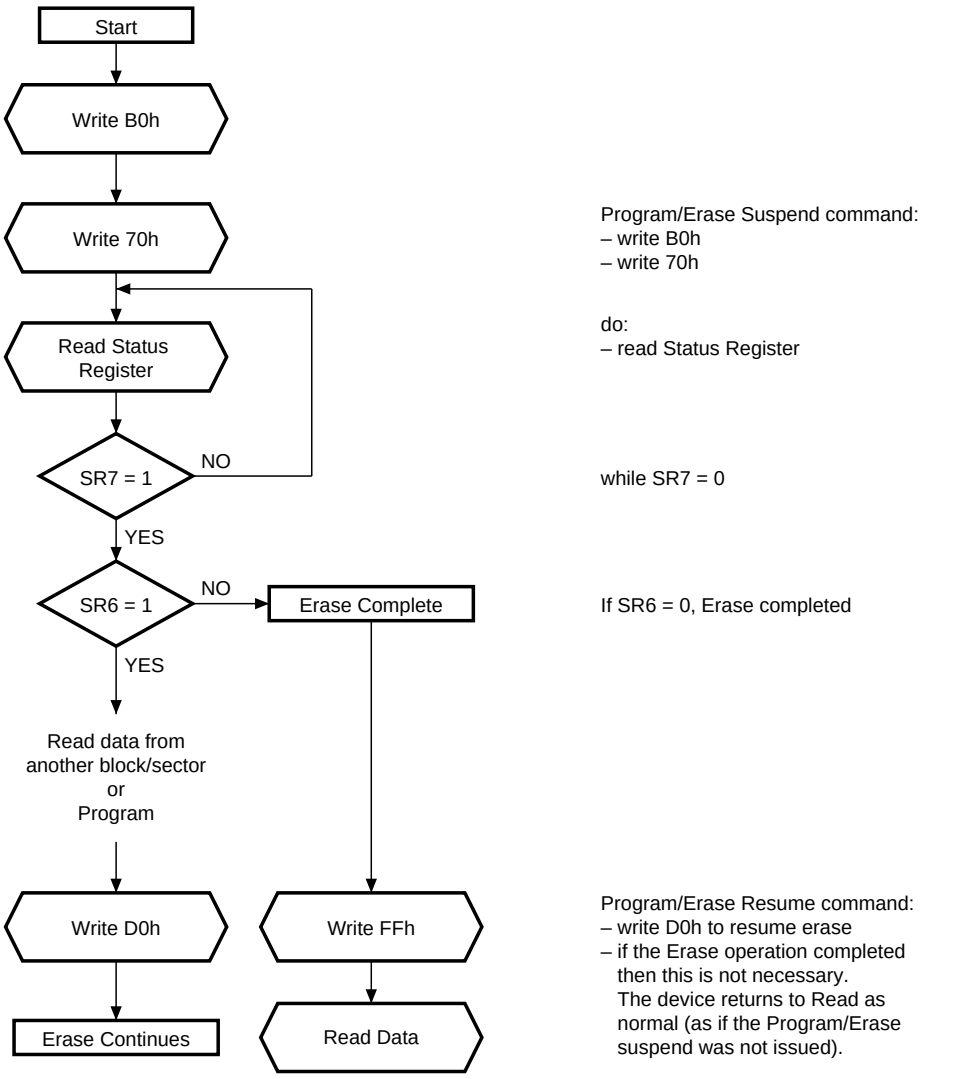
1. If an error is found, the Status Register must be cleared before further Program/Erase Controller operations.

Figure 26. Sector/Block Erase flowchart and pseudo code



1. If an error is found, the Status Register must be cleared before further Program/Erase Controller operations.

Figure 27. Erase Suspend and Resume flowchart and pseudo code



Revision history

Table 36. Document revision history

Date	Version	Changes
23-Jun-2003	1.0	First Issue
04-Jul-2003	2.0	$V_{IH}(\overline{INIT})$ min parameter modified in *Table 24: DC characteristics*. Document status promoted from Target Specification to Product Preview
28-Jul-2003	2.1	Document renamed to M50FLW040A, M50FLW040B
08-Oct-2003	2.2	Block types removed from the Block and Sector Address tables
07-Nov-2003	2.3	Document promoted to Preliminary Data
18-Feb-2004	3.0	Wording in the textual descriptions revised throughout the document.
18-May-2004	4.0	TSOP32 package added. Updates to Tables *8*, *9*, *12*, *13*, *14*, *15*, *19*, *26*, *34* and *35*; and to Figures *14*, and *21* to *27*
18-Aug-2004	5.0	Pins 2 and 5 of the TSOP32 Connections illustration corrected
24-Oct-2006	6	Document converted to new ST template. Packages are ECOPACK® compliant. T_{LEAD} removed from *Table 19: Absolute maximum ratings*. Device grade 1 removed. Blank *Plating Technology* option removed from *Table 33: Ordering information scheme*.

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