DATA SHEET

2.5 V and 3.3 V CMOS PLL Clock Generator and Driver

MPC9315

The MPC9315 is a 2.5 V and 3.3 V compatible, PLL based clock generator designed for low-skew clock distribution in low-voltage mid-range to high-performance telecom, networking and computing applications. The MPC9315 offers 8 low-skew outputs and 2 selectable inputs for clock redundancy. The outputs are configurable and support 1:1, 2:1, 4:1, 1:2 and 1:4 output to input frequency ratios. In addition, a selectable output 180° phase control supports advanced clocking schemes with inverted clock signals. The MPC9315 is specified for the extended temperature range of –40 to +85°C.

LOW VOLTAGE
2.5 V AND 3.3 V PLL
CLOCK GENERATOR

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-04

AC SUFFIX
32-LEAD LQFP PACKAGE
Pb-FREE PACKAGE
CASE 873A-04

Features

- Configurable 8 outputs LVCMOS PLL clock generator
- Compatible to various microprocessors such as PowerQUICC I and II
- Wide range output clock frequency of 18.75 to 160 MHz
- 2.5 V and 3.3 V CMOS compatible
- Designed for mid-range to high-performance telecom, networking and computer applications
- Fully integrated PLL supports spread spectrum clocking
- Supports applications requiring clock redundancy
- Max. output skew of 120 ps (80 ps within one bank)
- Selectable output configurations (1:1, 2:1, 4:1, 1:2, 1:4 frequency ratios)
- Two selectable LVCMOS clock inputs
- External PLL feedback path and selectable feedback configuration
- Tristable outputs
- 32-Lead LQFP package
- Ambient operating temperature range of -40 to +85°C
- 32-Lead Pb-free package available

Functional Description

The MPC9315 utilizes PLL technology to frequency and phase lock its outputs onto an input reference clock. Normal operation requires a connection of one of the device outputs to the selected feedback (FB0 or FB1) input to close the PLL feedback path. The reference clock frequency and the output divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. With available output dividers of divide-by-1, divide-by-2 and divide-by-4, the internal VCO of the MPC9315 is running at either 1x, 2x or 4x of the reference clock frequency. The frequency of the QA, QB, QC output groups is either the equal, one half or one fourth of the selected VCO frequency and can be configured for each output bank using the FSELA, FSELB and FSELC pins, respectively. The available output to input frequency ratios are 4:1, 2:1, 1:1, 1:2 and 1:4. The REF_SEL pin selects one of the two available LVCMOS compatible reference input (CLK0 and CLK1) supporting clock redundant applications. The selectable feedback input pin allows the user to select different feedback configurations and input to output frequency ratios. The MPC9315 also provides a static test mode when the PLL supply pin (V_{CCA}) is pulled to logic low state (GND). In test mode, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The test mode is intended for system diagnostics, test and debug purposes. This test mode is fully static and the minimum clock frequency specification does not apply. The outputs can be disabled by deasserting the $\overline{OE}$ pin (logic high state). In PLL mode, deasserting $\overline{OE}$ causes the PLL to lose lock due to no feedback signal presence at FB0 or FB1. Asserting $\overline{OE}$ will enable the outputs and close the phase locked loop, also enabling the PLL to recover to normal operation. The MPC9315 is fully 2.5 V and 3.3 V compatible and requires no external loop filter components. All inputs accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9315 outputs can drive one or two traces giving the devices an effective fanout of 1:18. The device is packaged in a 7x7 mm^2 32-lead LQFP package.

The fully integrated PLL of the MPC9315 allows the low skew outputs to lock onto a clock input and distribute it with essentially zero propagation delay to multiple components on the board. In zero-delay buffer mode, the PLL minimizes phase offset between the outputs and the reference signal.

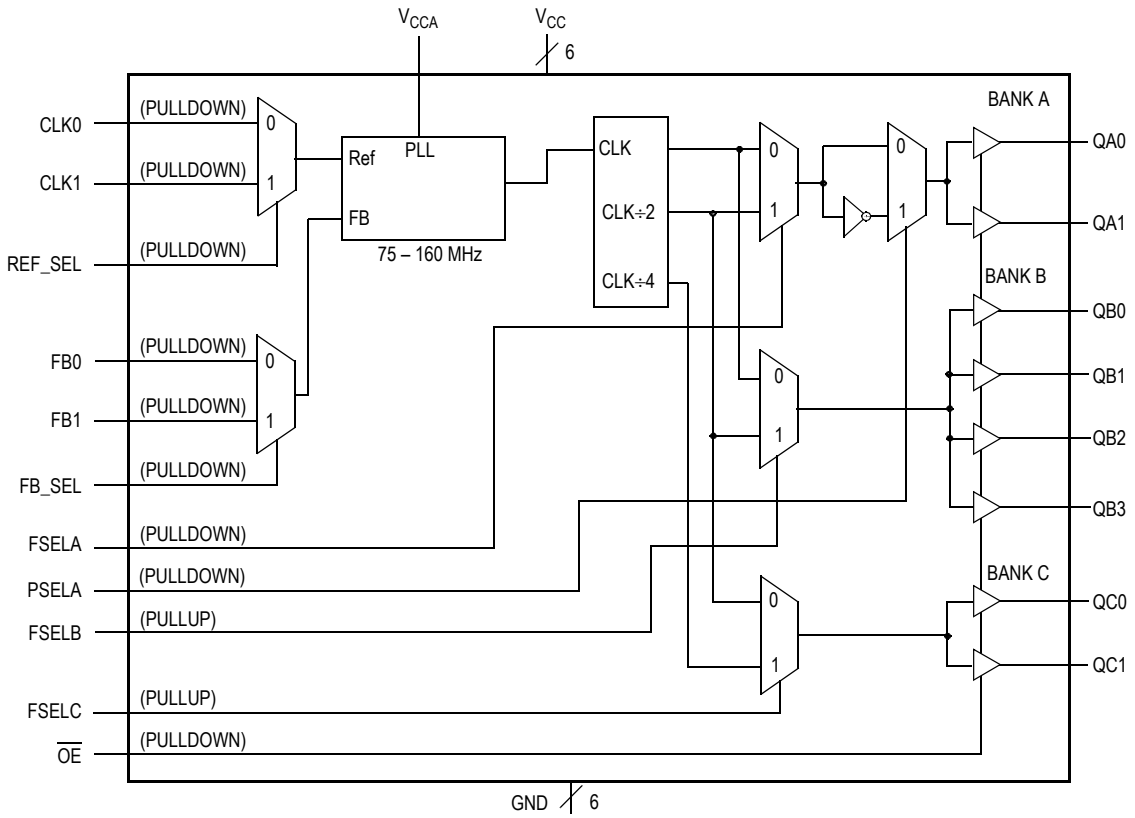


Figure 1. MPC9315 Logic Diagram

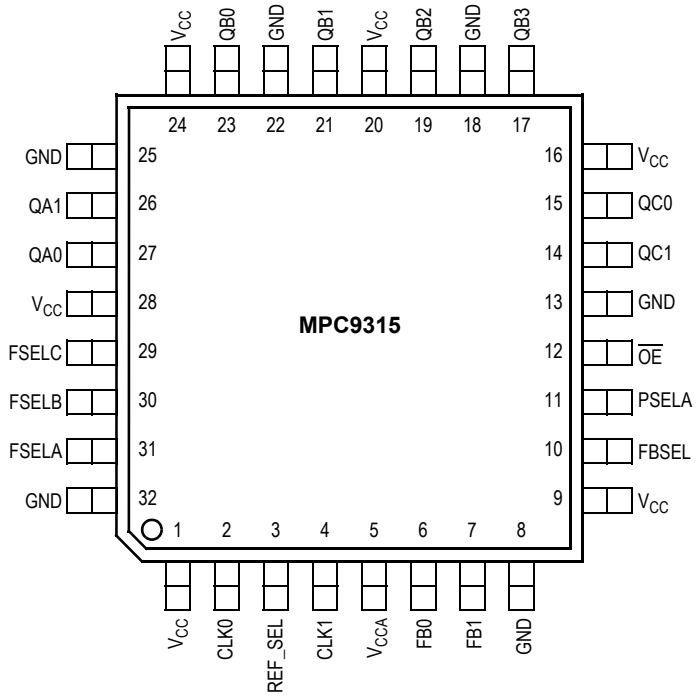


Figure 2. Pinout: 32-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
CLK0	Input	LVCMOS	Reference clock input
CLK1	Input	LVCMOS	Alternative clock input
FB0	Input	LVCMOS	PLL feedback input
FB1	Input	LVCMOS	Alternative feedback input
REF_SEL	Input	LVCMOS	Selects clock input reference clock input, default low (pull-down)
FB_SEL	Input	LVCMOS	Selects PLL feedback clock input, default low (pull-down)
FSELA	Input	LVCMOS	Selects divider ratio of bank A outputs, default low (pull-down)
FSELB	Input	LVCMOS	Selects divider ratio of bank B outputs, default low (pull-up)
FSELC	Input	LVCMOS	Selects divider ratio of bank C outputs, default low (pull-up)
PSELA	Input	LVCMOS	Selects phase of bank A outputs
QA0, QA1	Output	LVCMOS	Bank A outputs
QB0 to QB3	Output	LVCMOS	Bank B outputs
QC0, QC1	Output	LVCMOS	Bank C outputs
$\overline{OE}$	Input	LVCMOS	Output tristate
V_{CCA}		Supply	Analog (PLL) positive supply voltage. Requires external RC filter
V_{CC}		Supply	Digital positive supply voltage
GND		Ground	Digital negative supply voltage (ground)

Table 2. Function Table

Control	Default	0	1
REF_SEL	0	CLK0	CLK1
FB_SEL	0	FB0	FB1
FSELA	0	QAx = VCO clock frequency	QA0, QA1 = VCO clock frequency ÷ 2
FSELB	1	QBx = VCO clock frequency	QB0 - QB3 = VCO clock frequency ÷ 2
FSELC	1	QCx = VCO clock frequency ÷ 2	QC0, QC1 = VCO clock frequency ÷ 4
PSELA	0	0° (QA0, QA1 non-inverted)	180° (QA0, QA1 inverted)
V_{CCA}	none	V_{CCA} = GND, PLL off and bypassed for static test and diagnosis	V_{CCA} = 3.3 or 2.5 V, PLL enabled
MR	0	Normal operation	Reset (VCO clamped to min. range)
$\overline{OE}$	0	Outputs enabled	Outputs disabled (tristate), open PLL loop

Table 3. Absolute Maximum Ratings(1)

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	4.6	V	
V_{IN}	DC Input Voltage	-0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	-0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage temperature	-55	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD (Machine Model)	200			V	
HBM	ESD (Human Body Model)	2000			V	
LU	Latch-Up	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 5. DC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = -40° to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –24 mA(1)
V_{OL}	Output Low Voltage			0.55 0.30	V V	I_{OL}= 24 mA(1) I_{OL}= 12 mA
Z_{OUT}	Output Impedance		14 - 17		Ω	
I_{IN}	Input Current(2)			±200	μA	V_{IN} = V_{CC} or GND
I_{CCA}	Maximum PLL Supply Current		3.5	7.0	mA	V_{CCA} Pin
I_{CCQ}	Maximum Quiescent Supply Current			1.0	mA	All V_{CC} Pins

1. The MPC9315 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines.
2. Inputs have pull-up or pull-down resistors affecting the input current.

Table 6. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = -40° to 85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency	÷1 feedback ÷2 feedback ÷4 feedback PLL bypass mode	100[2] 37.50 18.75 0		160 80 40 TBD	MHz MHz MHz MHz	PLL locked PLL locked PLL locked V_{CCA} = GND
f_{VCO}	VCO Lock Range		75[2]		160	MHz	
f_{MAX}	Maximum Output Frequency	÷1 output ÷2 output ÷4 output	75 37.50 18.75		160 80 40	MHz MHz MHz	
f_{refDC}	Reference Input Duty Cycle		25		75	%	
t_r, t_f	CLK0, CLK1 Input Rise/Fall Time				1.0	ns	0.8 to 2.0 V
$t_{(\varnothing)}$	Propagation Delay (Static Phase Offset)	CLK0 or CLK1 to FB	-150		+150	ps	PLL locked
$t_{SK(\varnothing)}$	Output-to-Output Skew	Within one bank Any output			80 120	ps ps	
DC	Output Duty Cycle		45	50	55	%	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4 V
$t_{PLZ, HZ}$	Output Disable Time				10	ns	
$t_{PZL, LZ}$	Output Enable Time				10	ns	
BW	PLL closed loop bandwidth	÷1 feedback ÷2 feedback ÷4 feedback		TBD 2.0 - 20 0.6 - 6.0		MHz MHz MHz	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	(1σ)		10	22	ps	RMS value
$t_{JIT(PER)}$	Period Jitter	(1σ)		8.0	15	ps	RMS value
$t_{JIT(\varnothing)}$	I/O Phase Jitter	(1σ)		8.0 - 25[3]	TBD	ps	RMS value
t_{LOCK}	Maximum PLL Lock Time				1.0	ms	

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. The VCO range in ÷1 feedback configuration (e.g. QAx connected to FBx and FSELA = 0) is limited to $100 \le f_{VCO} \le 160$ MHz. Please see next revision of the MPC9315 for improved VCO frequency range.
3. I/O jitter depends on VCO frequency. Please see application section for I/O jitter versus VCO frequency characteristics.

Table 7. DC Characteristics (V_{CC} = 2.5 V ± 5%, T_A = -40° to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	1.7		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.7	V	LVCMOS
V_{OH}	Output High Voltage	1.8			V	I_{OH} = –15 mA[1]
V_{OL}	Output Low Voltage			0.6	V	I_{OL}= 15 mA
Z_{OUT}	Output Impedance		17 - 20		Ω	
I_{IN}	Input Current[2]			±200	μA	V_{IN} = V_{CC} or GND
I_{CCA}	Maximum PLL Supply Current		2.0	5.0	mA	V_{CCA} Pin
I_{CCQ}	Maximum Quiescent Supply Current			1.0	mA	All V_{CC} Pins

1. The MPC9315 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines.
2. Inputs have pull-up or pull-down resistors affecting the input current.

Table 8. AC Characteristics (V_{CC} = 2.5 V ± 5%, T_A = -40° to 85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency	÷2 feedback ÷4 feedback PLL bypass mode	37.50 18.75 0		80 40 TBD	MHz MHz MHz	PLL locked PLL locked VCCA = GND
f_{VCO}	VCO Lock Range		75[2]		160[2]	MHz	
f_{MAX}	Maximum Output Frequency	÷1 output ÷2 output ÷4 output	75 37.50 18.75		160 80 40	MHz MHz MHz	
f_{refDC}	Reference Input Duty Cycle		25		75	%	
t_r, t_f	CLK0, CLK1 Input Rise/Fall Time				1.0	ns	0.7 to 1.7 V
$t_{(\varnothing)}$	Propagation Delay (Static Phase Offset)	CLK0 or CLK1 to FB	-150		+150	ps	PLL locked
$t_{SK(\varnothing)}$	Output-to-Output Skew	Within one bank Any output			80 120	ps ps	
DC	Output Duty Cycle		45	50	55	%	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4 V
$t_{PLZ, HZ}$	Output Disable Time				12	ns	
$t_{PZL, LZ}$	Output Enable Time				12	ns	
BW	PLL closed loop bandwidth	÷2 feedback ÷4 feedback		1.0 - 10 0.4 - 3.0		MHz MHz	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	(1σ)		10	22	ps	RMS value
$t_{JIT(PER)}$	Period Jitter	(1σ)		8.0	15	ps	RMS value
$t_{JIT(\varnothing)}$	I/O Phase Jitter	(1σ)		10 - 25[3]	TBD	ps	RMS value
t_{LOCK}	Maximum PLL Lock Time				1.0	ms	

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. ÷1 feedback is responsible for V_{CC} = 2.5 V operation. Please see application section for I/O jitter versus VCO frequency characteristics.
3. I/O jitter depends on VCO frequency. Please see application section for I/O jitter versus VCO frequency characteristics.

APPLICATIONS INFORMATION

Programming the MPC9315

The PLL of the MPC9315 supports output clock frequencies from 18.75 to 160 MHz. Different feedback and output divider configurations can be used to achieve the desired input to output frequency relationship. The feedback frequency and divider should be used to situate the VCO in the frequency range between 75 and 160 MHz for stable and optimal operation. The FSELA, FSELB, FSELC pins select the desired output clock frequencies. Possible frequency ratios of the reference clock input to the outputs are 1:1, 1:2, 1:4 as well as 2:1 and 4:1, Table 9, Table 10, and Table 11 illustrate the various output configurations and frequency ratios supported by the MPC9315. PSELA controls the output phase of the QA0 and QA1 outputs, allowing the user to generate inverted clock signals synchronous to non-inverted clock signals. See also Example Configurations for the MPC9315 for further reference.

Table 9. Output Frequency Relationship for QA0 connected to FB0(1)

Inputs			Outputs		
FSELA	FSELB	FSELC	QA0, QA1	QB0–QB3	QC0, QC1
0	0	0	CLK	CLK	CLK ÷ 2
0	0	1	CLK	CLK	CLK ÷ 4
0	1	0	CLK	CLK ÷ 2	CLK ÷ 2
0	1	1	CLK	CLK ÷ 2	CLK ÷ 4
1	0	0	CLK	2 * CLK	CLK
1	0	1	CLK	2 * CLK	CLK ÷ 2
1	1	0	CLK	CLK	CLK
1	1	1	CLK	CLK	CLK ÷ 2

1. Output frequency relationship with respect to input reference frequency CLK.

Table 10. Output Frequency Relationship for QB0 connected to FB0(1)

Inputs			Outputs		
FSELA	FSELB	FSELC	QA0, QA1	QB0–QB3	QC0, QC1
0	0	0	CLK	CLK	CLK ÷ 2
0	0	1	CLK	CLK	CLK ÷ 4
0	1	0	2 * CLK	CLK	CLK
0	1	1	2 * CLK	CLK	CLK ÷ 2
1	0	0	CLK ÷ 2	CLK	CLK ÷ 2
1	0	1	CLK ÷ 2	CLK	CLK ÷ 4
1	1	0	CLK	CLK	CLK
1	1	1	CLK	CLK	CLK ÷ 2

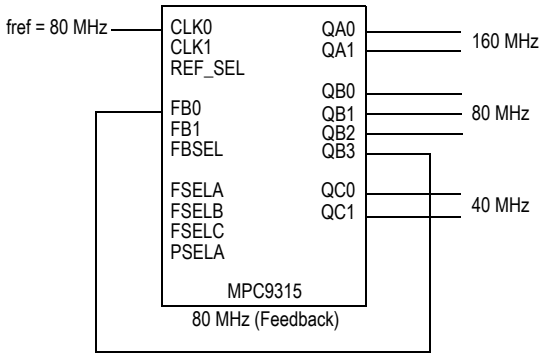
1. Output frequency relationship with respect to input reference frequency CLK.

Table 11. Output Frequency Relationship for QC0 connected to FB0(1)

Inputs			Outputs		
FSELA	FSELB	FSELC	QA0, QA1	QB0–QB3	QC0, QC1
0	0	0	2 * CLK	2 * CLK	CLK
0	0	1	4 * CLK	4 * CLK	CLK
0	1	0	2 * CLK	CLK	CLK
0	1	1	4 * CLK	2 * CLK	CLK
1	0	0	CLK	2 * CLK	CLK
1	0	1	2 * CLK	4 * CLK	CLK
1	1	0	CLK	CLK	CLK
1	1	1	2 * CLK	2 * CLK	CLK

1. Output frequency relationship with respect to input reference frequency CLK.

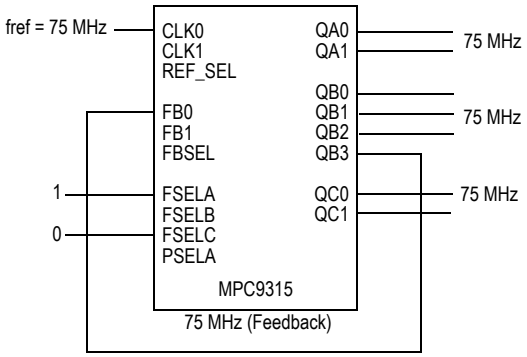
Example Configurations for the MPC9315



MPC9315 default configuration (feedback of QB3 = 100 MHz). All control pins are left open.

Frequency range	Min	Max
Input	37.50 MHz	80 MHz
QA outputs	75.00 MHz	160 MHz
QB outputs	37.50 MHz	80 MHz
QC outputs	18.75 MHz	40 MHz

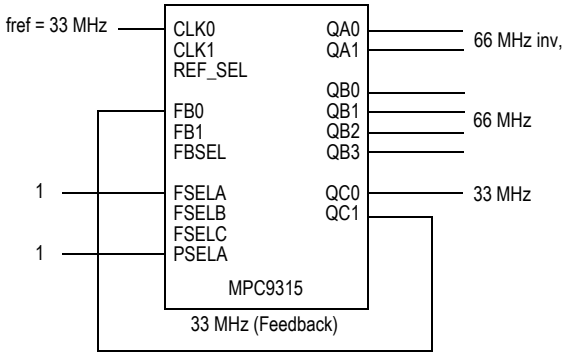
Figure 3. MPC9315 Default Configuration



MPC9315 1:1 frequency configuration (feedback of QB3 = 75 MHz). FSELA = H, FSELC = L. All other control pins are left open.

Frequency range	Min	Max
Input	37.50 MHz	80 MHz
QA outputs	37.50 MHz	80 MHz
QB outputs	37.50 MHz	80 MHz
QC outputs	37.50 MHz	80 MHz

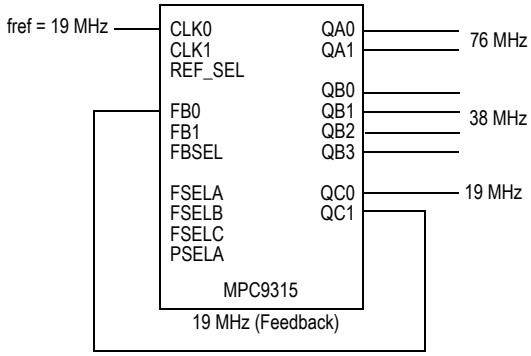
Figure 4. MPC9315 Zero Delay Buffer Configuration



MPC9315 1:1 frequency configuration (feedback of QC1 = 33 MHz). FSELA = PSELA = H. All other control pins are left open.

Frequency range	Min	Max
Input	18.75 MHz	40 MHz
QA outputs	37.50 MHz	80 MHz
QB outputs	37.50 MHz	80 MHz
QC outputs	18.75 MHz	40 MHz

Figure 5. MPC9315 180° Phase Inversion Configuration



MPC9315 4x, 2x, 1x frequency configuration (feedback of QC1 = 19 MHz). All control pins are left open.

Frequency range	Min	Max
Input	18.75 MHz	40 MHz
QA outputs	75.00 MHz	160 MHz
QB outputs	37.50 MHz	80 MHz
QC outputs	18.75 MHz	40 MHz

Figure 6. MPC9315 x4 Multiplier Configuration

Using the MPC9315 in Zero-Delay Applications

The external feedback option of the MPC9315 PLL allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge and virtually eliminates the propagation delay through the device.

The remaining insertion delay (skew error) of the MPC9315 in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset (SPO or $t_{(\varnothing)}$), I/O jitter ($t_{JIT(\varnothing)}$, phase or long-term jitter), feedback path delay and the output-to-output skew ($t_{SK(O)}$ relative to the feedback output.

Calculation of Part-to-Part Skew

The MPC9315 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs (TCLK or PCLK) of two or more MPC9315 are connected together, the maximum overall timing uncertainty from the common TCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \bullet CF$$

This maximum timing uncertainty consists of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

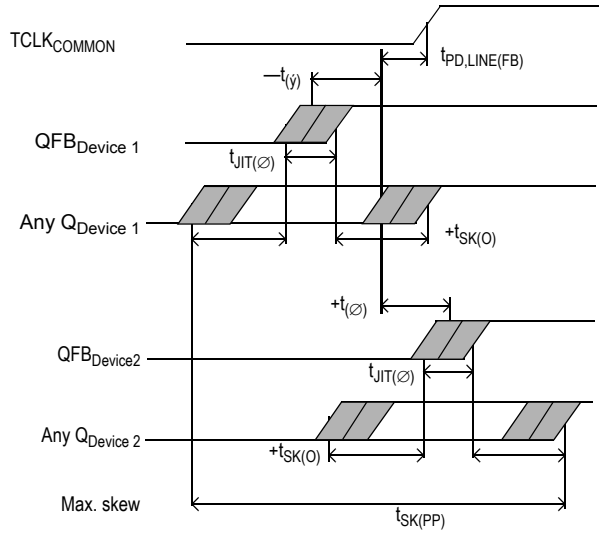


Figure 7. MPC9315 max. Device-to-Device Skew

Due to the statistical nature of I/O jitter, an RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 12.

Table 12. Confidence Factor CF

CF	Probability of Clock Edge within the Distribution
± 1σ	0.68268948
± 2σ	0.95449988
± 3σ	0.99730007
± 4σ	0.99993663
± 5σ	0.99999943
± 6σ	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation, an I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of –300 ps to +300 ps relative to TCLK (V_{CC} = 3.3 V and f_{VCO} = 160 MHz):

$$t_{SK(PP)} = [–150ps...150ps] + [–150ps...150ps] + [(10ps\ @\ –3)...(10ps\ @\ 3)] + t_{PD,\ LINE(FB)}$$

$$t_{SK(PP)} = [–300ps...300ps] + t_{PD,\ LINE(FB)}$$

Above equation uses the maximum I/O jitter number shown in the AC characteristic table for V_{CC} = 3.3 V (10 ps RMS). I/O jitter is frequency-dependant with a maximum at the lowest VCO frequency (160 MHz for the MPC9315). Applications using a higher VCO frequency exhibit less I/O jitter than the AC characteristic limit. The I/O jitter characteristics in Figure 8 and Figure 9 can be used to derive a smaller I/O jitter number at the specific VCO frequency, resulting in tighter timing limits in zero-delay mode and for part-to-part skew $t_{SK(PP)}$.

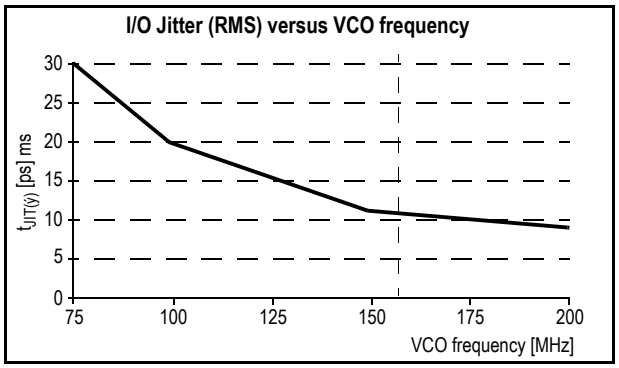


Figure 8. Max. I/O Jitter (RMS) versus frequency for V_{CC} = 2.5 V

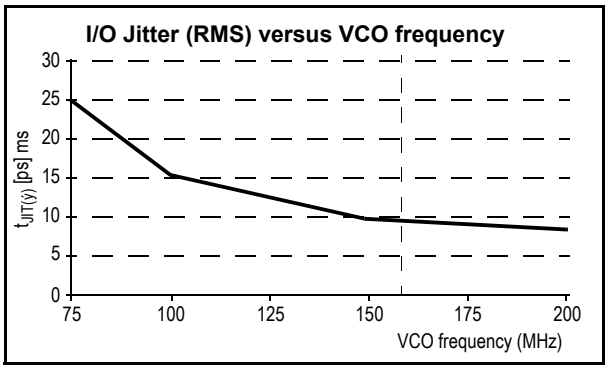


Figure 9. Max. I/O Jitter (RMS) versus frequency for V_{CC} = 3.3 V

Power Supply Filtering

The MPC9315 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Noise on the V_{CCA} (PLL) power supply impacts the device characteristics, for instance I/O jitter. The MPC9315 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies, a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CCA} pin for the MPC9315. Figure 10 illustrates a typical power supply filter scheme. The MPC9315 frequency and phase stability is most susceptible to noise with spectral content in the 100 kHz to 20 MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet, the I_{CCA} current (the current sourced through the V_{CCA} pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.325 V (V_{CC} = 3.3 V or V_{CC} = 2.5 V) must be maintained on the V_{CCA} pin. The resistor R_F shown in Figure 10 must have a resistance of 270 Ω (V_{CC} = 3.3 V) or 9-10 Ω (V_{CC} = 2.5 V) to meet the voltage drop criteria.

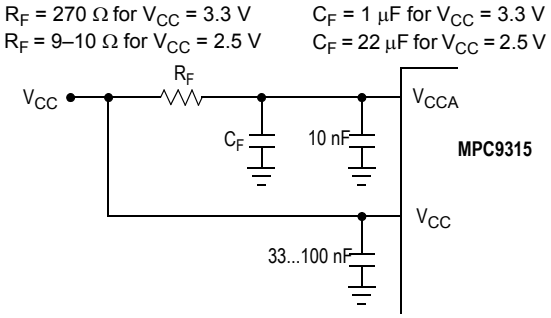


Figure 10. V_{CCA} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 10, the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9315 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise-related problems in most designs.

Driving Transmission Lines

The MPC9315 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user, the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω, the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines, the reader is referred to Freescale application note AN1091. In most high performance clock networks, point-to-point distribution of signals is the method of choice. In a point-to-point scheme, either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to V_{CC}÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9315 clock driver. For the series terminated case, however, there is no DC current draw; thus, the outputs can drive multiple series terminated lines. Figure 11 illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme, the fanout of the MPC9315 clock driver is effectively doubled due to its capability to drive multiple lines.

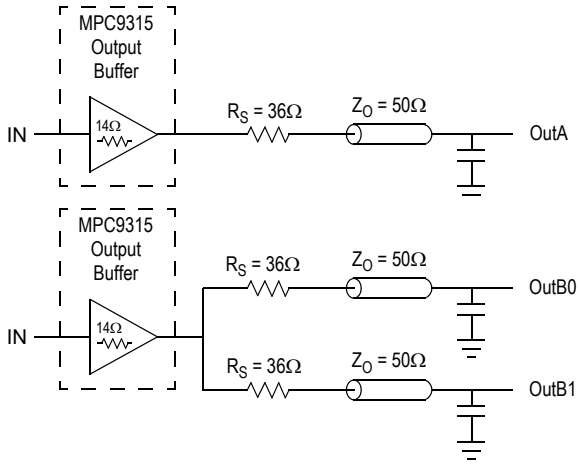


Figure 11. Single versus Dual Transmission Lines

The waveform plots in Figure 11 show the simulation results of an output driving a single line versus two lines. In

both cases, the drive capability of the MPC9315 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations, a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9315. The output waveform in Figure 12 shows a step in the waveform; this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\ \Omega \parallel 50\ \Omega$$
$$R_S = 36\ \Omega \parallel 36\ \Omega$$
$$R_0 = 14\ \Omega$$
$$V_L = 3.0\ (25 \div (18+17+25)$$
$$= 1.31\ V$$

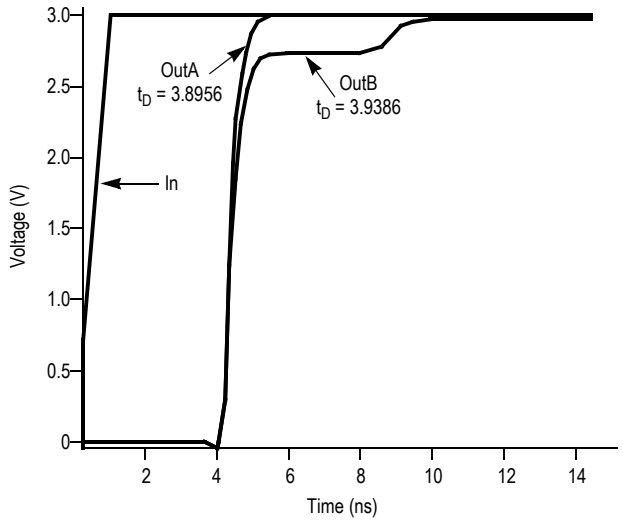


Figure 12. Single versus Dual Line Termination Waveforms

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

Since this step is well above the threshold region, it will not cause any false clock triggering; however, designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines, the situation in Figure 13 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance, the line impedance is perfectly matched.

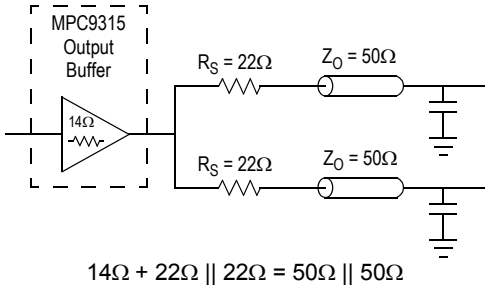


Figure 13. Optimized Dual Line Termination

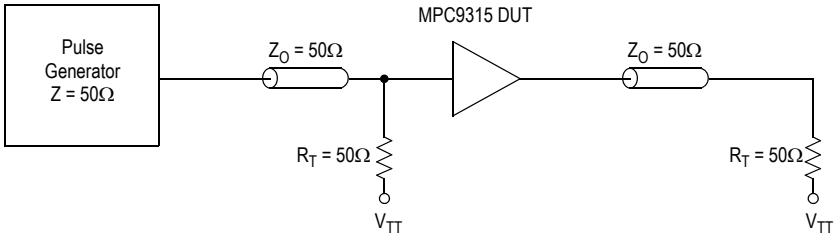


Figure 14. CLK0, CLK1 MPC9315 AC Test Reference

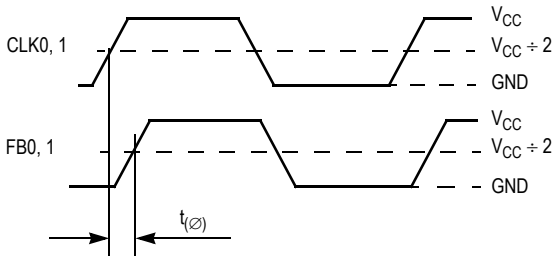
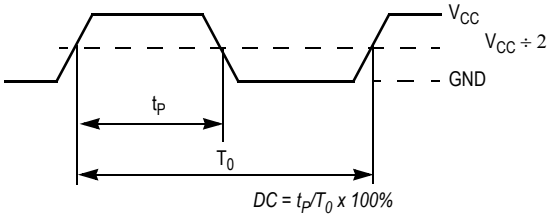
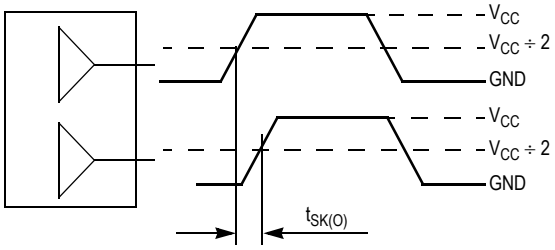


Figure 15. Propagation delay ($t_{(\varnothing)}$, SPO) Test Reference



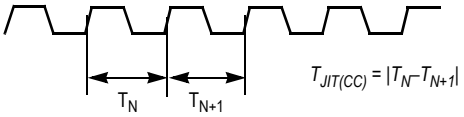
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 16. Output Duty Cycle (DC)



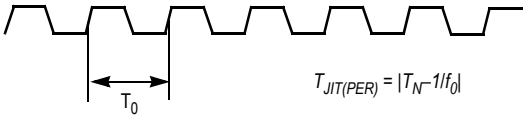
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 17. Output-to-Output Skew $t_{SK(O)}$



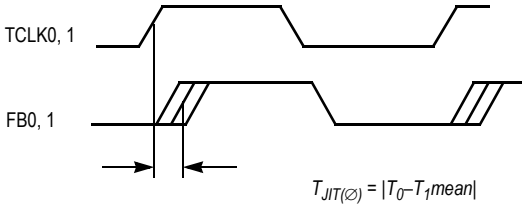
The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 18. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 19. Period Jitter



The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 20. I/O Jitter

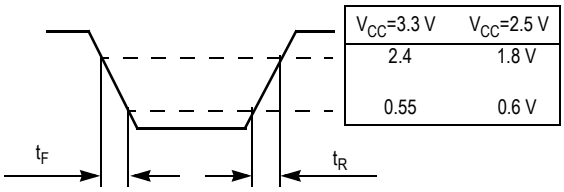
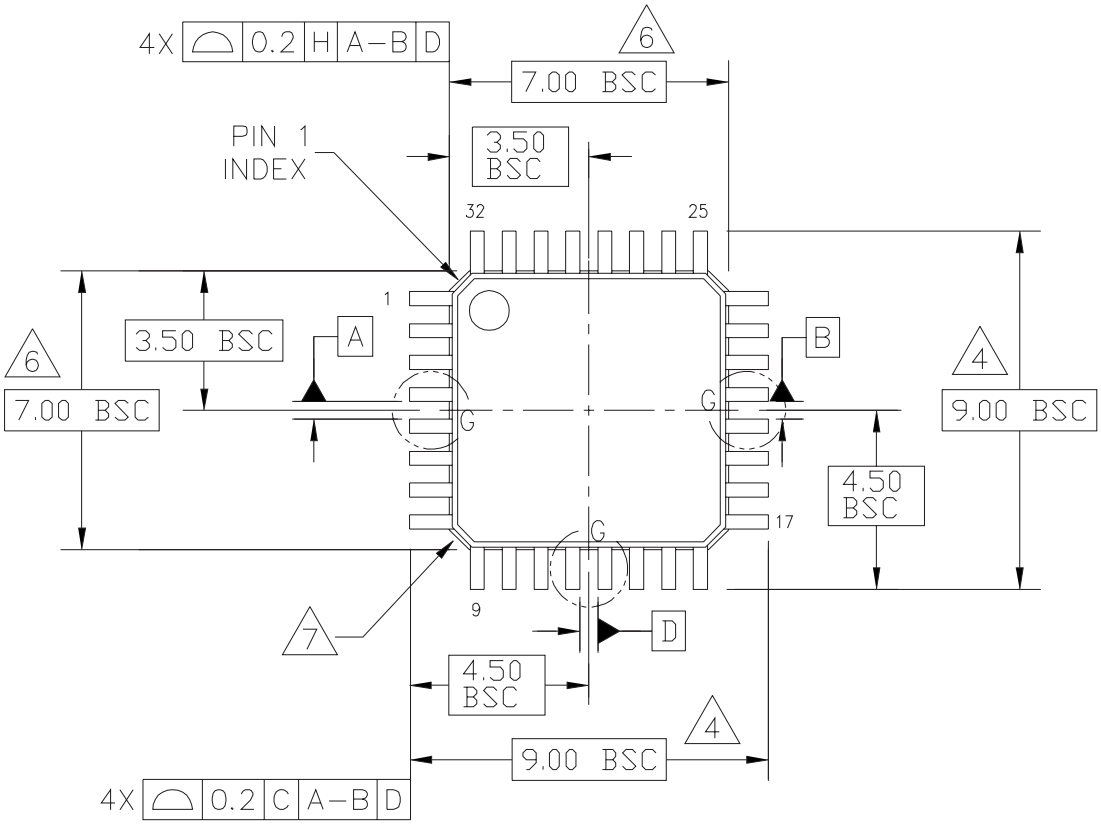
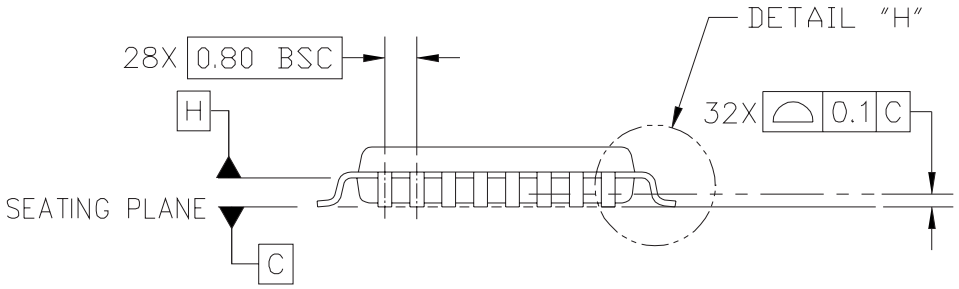


Figure 21. Output Transition Time Test Reference

PACKAGE DIMENSIONS





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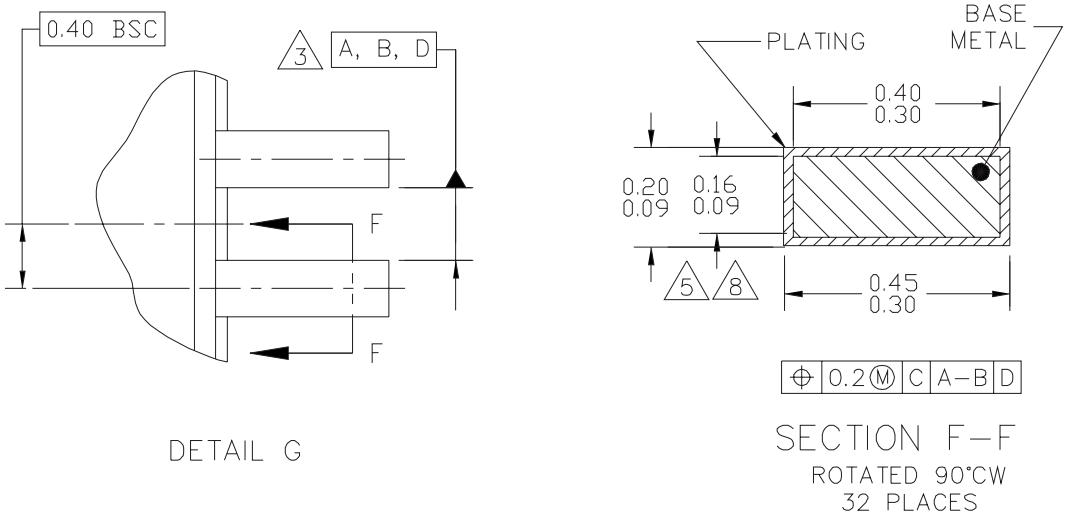

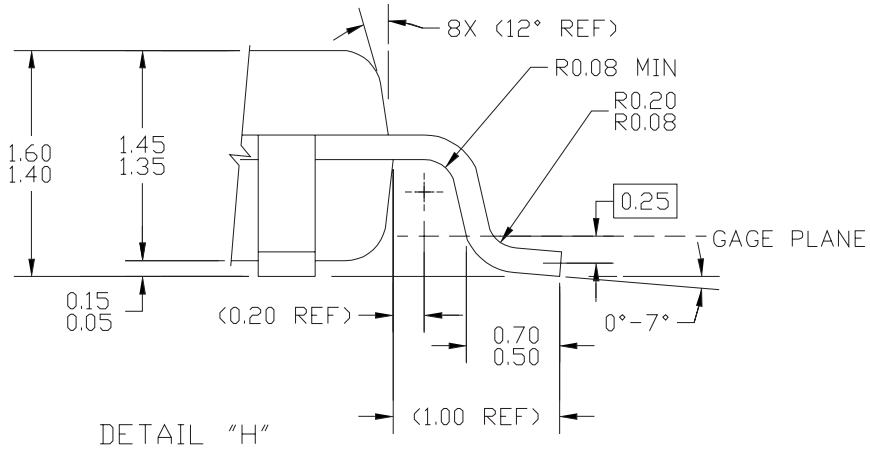

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NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5–1994.
3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE DATUM C.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07 MM.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

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