

NUP4301MR6T1

Low Capacitance Diode Array for ESD Protection in Four Data Lines

NUP4301MR6T1 is a MicroIntegration™ device designed to provide protection for sensitive components from possible harmful electrical transients; for example, ESD (electrostatic discharge).

Features

- Low Capacitance (1.5 pf Maximum Between I/O Lines)
- Single Package Integration Design
- Provides ESD Protection for JEDEC Standards JESD22 Machine Model = Class C Human Body Model = Class 3B
- Protection for IEC61000-4-2 (Level 4) 8.0 kV (Contact) 15 kV (Air)
- Ensures Data Line Speed and Integrity
- Fewer Components and Less Board Space
- Direct the Transient to Either Positive Side or to the Ground
- Pb-Free Package is Available

Applications

- USB 1.1 and 2.0 Data Line Protection
- T1/E1 Secondary IC Protection
- T3/E3 Secondary IC Protection
- HDSL, IDSL Secondary IC Protection
- Video Line Protection
- Microcontroller Input Protection
- Base Stations
- I²C Bus Protection

MAXIMUM RATINGS (Each Diode) (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Reverse Voltage	V _R	70	Vdc
Forward Current	I _F	200	mAdc
Peak Forward Surge Current	I _{FM(surge)}	500	mAdc
Repetitive Peak Reverse Voltage	V _{RPM}	70	V
Average Rectified Forward Current (Note 1) (averaged over any 20 ms period)	I _{F(AV)}	715	mA
Repetitive Peak Forward Current	I _{FRM}	450	mA
Non-Repetitive Peak Forward Current	I _{FSM}	2.0 1.0 0.5	A
		t = 1.0 μs	
		t = 1.0 ms	
		t = 1.0 S	

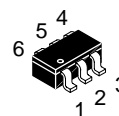
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. FR-5 = 1.0 × 0.75 × 0.062 in.



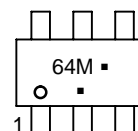
ON Semiconductor®

<http://onsemi.com>



TSOP-6
CASE 318F
PLASTIC

MARKING DIAGRAM

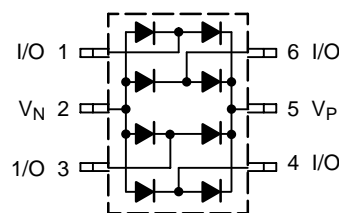


64 = Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location.)

*Date Code orientation may vary depending upon manufacturing location.

PIN CONFIGURATION AND SCHEMATIC



ORDERING INFORMATION

Device	Package	Shipping†
NUP4301MR6T1	TSOP-6	3000/Tape & Reel
NUP4301MR6T1G	TSOP-6 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NUP4301MR6T1

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	556	°C/W
Lead Solder Temperature, Maximum 10 Seconds Duration	T_L	260	°C
Junction Temperature	T_J	-40 to +85	°C
Storage Temperature	T_{stg}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (Each Diode)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Reverse Breakdown Voltage ($I_{(BR)} = 100 \mu\text{A}$)	$V_{(BR)}$	70	-	-	Vdc
Reverse Voltage Leakage Current ($V_R = 70 \text{ Vdc}$) ($V_R = 25 \text{ Vdc}, T_J = 150^\circ\text{C}$) ($V_R = 70 \text{ Vdc}, T_J = 150^\circ\text{C}$)	I_R	-	-	2.5 30 50	μA_{dc}
Capacitance (between I/O pins) ($V_R = 0 \text{ V}, f = 1.0 \text{ MHz}$)	C_D	-	0.8	1.5	pF
Capacitance (between I/O pin and ground) ($V_R = 0 \text{ V}, f = 1.0 \text{ MHz}$)	C_D	-	1.6	3	pF
Forward Voltage ($I_F = 1.0 \text{ mA}_{dc}$) ($I_F = 10 \text{ mA}_{dc}$) ($I_F = 50 \text{ mA}_{dc}$) ($I_F = 150 \text{ mA}_{dc}$)	V_F	-	-	715 855 1000 1250	mV_{dc}

2. Alumina = $0.4 \times 0.3 \times 0.024$ in. 99.5% alumina.

Curves Applicable to Each Cathode

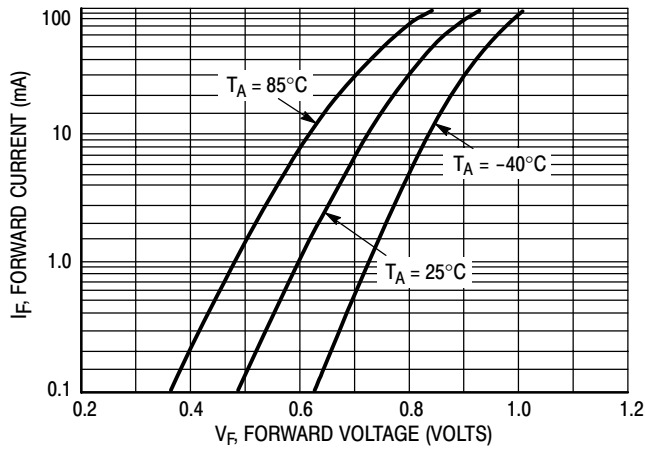


Figure 1. Forward Voltage

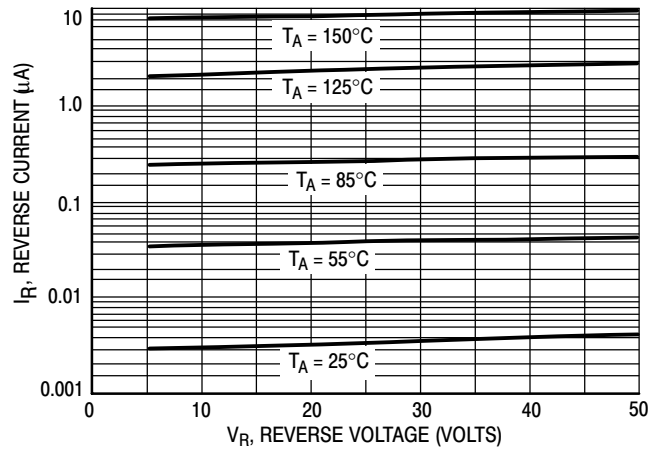


Figure 2. Leakage Current

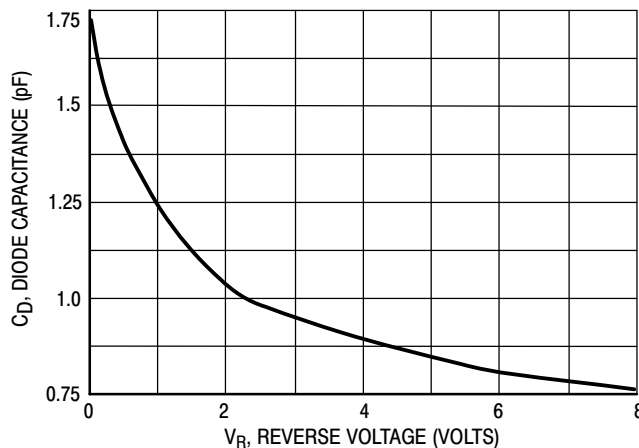
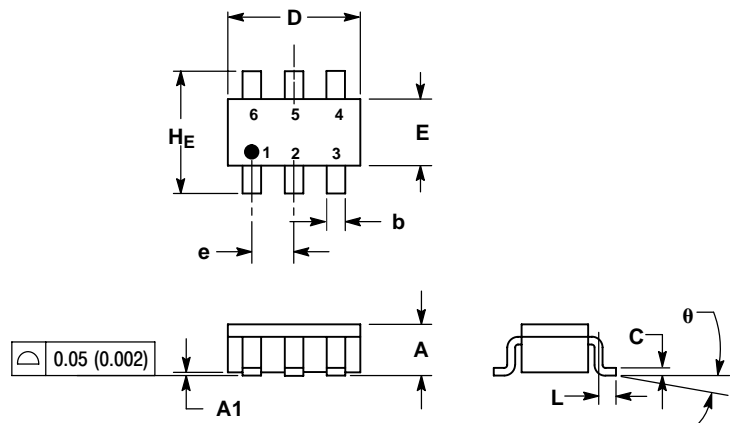


Figure 3. Capacitance

NUP4301MR6T1

PACKAGE DIMENSIONS

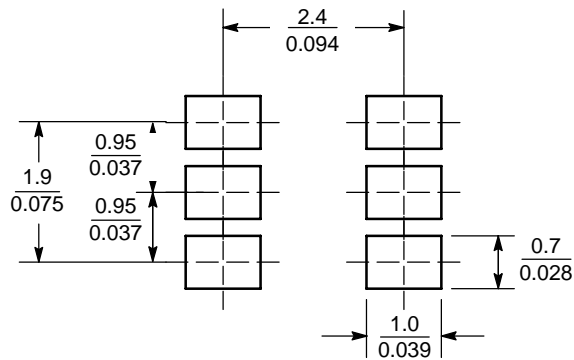
TSOP-6
CASE 318F-05
ISSUE L



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
 4. 318F-01, -02, -03 OBSOLETE. NEW STANDARD 318F-04.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.37	0.50	0.010	0.015	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
HE	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	-	10°	0°	-	10°

SOLDERING FOOTPRINT*



SCALE 10:1 (mm/inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NUP4301MR6T1

MicroIntegration is a trademarks of Semiconductor Components Industries, LLC (SCILLC).

ON Semiconductor and **ON** are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA
Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada
Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your
local Sales Representative.

NUP4301MR6T1/D