

# SN74CB3Q3244

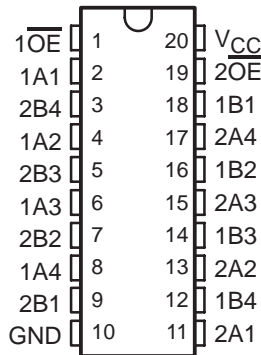
## 8-BIT FET BUS SWITCH

### 2.5-V/3.3-V LOW-VOLTAGE HIGH-BANDWIDTH BUS SWITCH

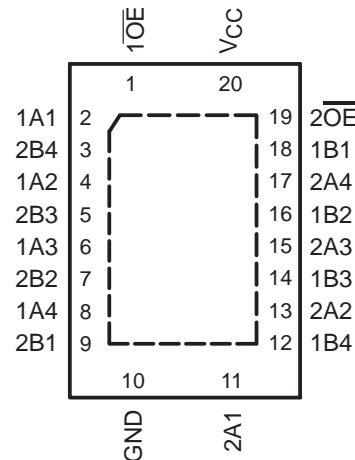
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- High-Bandwidth Data Path (Up To 500 MHz†)
  - 5-V-Tolerant I/Os with Device Powered Up or Powered Down
  - Low and Flat ON-State Resistance ( $r_{ON}$ ) Characteristics Over Operating Range ( $r_{ON} = 4 \Omega$  Typical)
  - Rail-to-Rail Switching on Data I/O Ports
    - 0- to 5-V Switching With 3.3-V  $V_{CC}$
    - 0- to 3.3-V Switching With 2.5-V  $V_{CC}$
  - Bidirectional Data Flow, With Near-Zero Propagation Delay
  - Low Input/Output Capacitance Minimizes Loading and Signal Distortion ( $C_{IO(OFF)} = 3.5 \text{ pF}$  Typical)
  - Fast Switching Frequency ( $f_{OE} = 20 \text{ MHz}$  Max)
- † For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C*, *CB3T*, and *CB3Q Signal-Switch Families*, literature number SCDA008.
- Data and Control Inputs Provide Undershoot Clamp Diodes
  - Low Power Consumption ( $I_{CC} = 0.7 \text{ mA}$  Typical)
  - $V_{CC}$  Operating Range From 2.3 V to 3.6 V
  - Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
  - Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
  - $I_{off}$  Supports Partial-Power-Down Mode Operation
  - Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
  - ESD Performance Tested Per JESD 22
    - 2000-V Human-Body Model (A114-B, Class II)
    - 1000-V Charged-Device Model (C101)
  - Supports Both Digital and Analog Applications: Differential Signal Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating

DB, DBQ, DGV, DW, OR PW PACKAGE  
(TOP VIEW)



RGY PACKAGE  
(TOP VIEW)



#### description/ordering information

The SN74CB3Q3244 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance ( $r_{ON}$ ). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3244 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.



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**description/ordering information (continued)**

The SN74CB3Q3244 is organized as two 4-bit bus switches with separate output-enable ( $\overline{1OE}$ ,  $\overline{2OE}$ ) inputs. It can be used as two 4-bit bus switches or as one 8-bit bus switch. When  $\overline{OE}$  is low, the associated 4-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When  $\overline{OE}$  is high, the associated 4-bit bus switch is OFF, and the high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

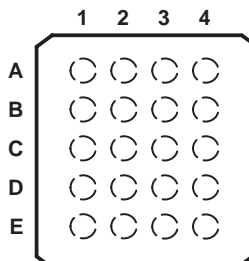
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**ORDERING INFORMATION**

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RGY	Tape and reel	SN74CB3Q3244RGYR	BU244
	SOIC – DW	Tube	SN74CB3Q3244DW	CB3Q3244
		Tape and reel	SN74CB3Q3244DWR	
	SSOP – DB	Tape and reel	SN74CB3Q3244DBR	BU244
	SSOP (QSOP) – DBQ	Tape and reel	SN74CB3Q3244DBQR	CB3Q3244
	TSSOP – PW	Tube	SN74CB3Q3244PW	BU244
		Tape and reel	SN74CB3Q3244PWR	
TVSOP – DGV	Tape and reel	SN74CB3Q3244DGV	BU244	
VFBGA – GQN	Tape and reel	SN74CB3Q3244GQNR	BU244	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

**GQN PACKAGE (TOP VIEW)**



**terminal assignments**

	1	2	3	4
A	1A1	$\overline{1OE}$	$V_{CC}$	$\overline{2OE}$
B	1A2	2A4	2B4	1B1
C	1A3	2B3	2A3	1B2
D	1A4	2A2	2B2	1B3
E	GND	2B1	2A1	1B4

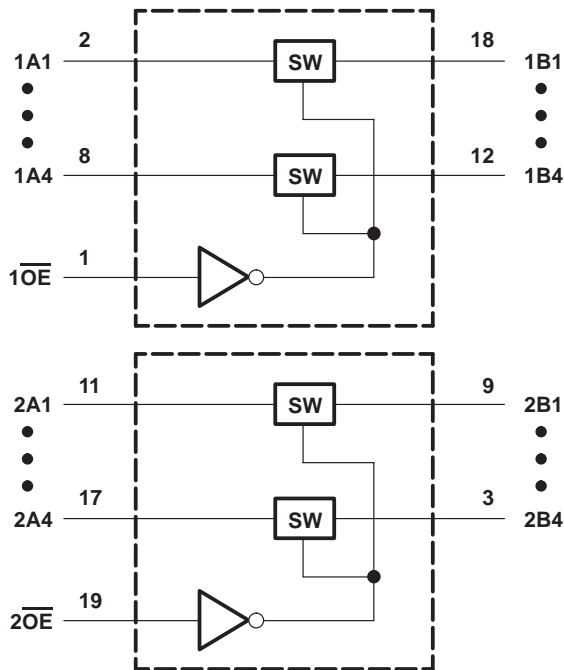
**FUNCTION TABLE (each 4-bit bus switch)**

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

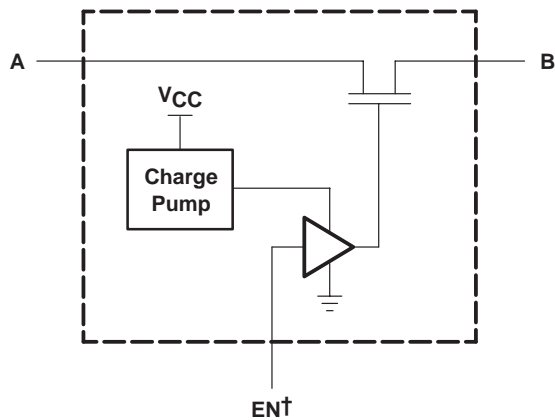
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logic diagram (positive logic)



simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Control input voltage range, $V_{IN}$ (see Notes 1 and 2)	–0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	–0.5 V to 7 V
Control input clamp current, $I_{IK}$ ( $V_{IN} < 0$ )	–50 mA
I/O port clamp current, $I_{I/OK}$ ( $V_{I/O} < 0$ )	–50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	±64 mA
Continuous current through $V_{CC}$ or GND terminals	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 5): DB package	70°C/W
(see Note 5): DBQ package	68°C/W
(see Note 5): DGV package	92°C/W
(see Note 5): DW package	58°C/W
(see Note 5): GQN package	78°C/W
(see Note 5): PW package	83°C/W
(see Note 6): RGY package	37°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
- All voltages are with respect to ground unless otherwise specified.
  - The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  - $V_I$  and  $V_O$  are used to denote specific conditions for  $V_{I/O}$ .
  - $I_I$  and  $I_O$  are used to denote specific conditions for  $I_{I/O}$ .
  - The package thermal impedance is calculated in accordance with JESD 51-7.
  - The package thermal impedance is calculated in accordance with JESD 51-5.

#### recommended operating conditions (see Note 7)

		MIN	MAX	UNIT	
$V_{CC}$	Supply voltage	2.3	3.6	V	
$V_{IH}$	High-level control input voltage	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	5.5	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2	5.5	
$V_{IL}$	Low-level control input voltage	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0	0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	0	0.8	
$V_{I/O}$	Data input/output voltage	0	5.5	V	
$T_A$	Operating free-air temperature	–40	85	°C	

NOTE 7: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V <sub>IK</sub>		V <sub>CC</sub> = 3.6 V,	I <sub>I</sub> = -18 mA			-1.8	V
I <sub>IN</sub>	Control inputs	V <sub>CC</sub> = 3.6 V,	V <sub>IN</sub> = 0 to 5.5 V			±1	μA
I <sub>OZ</sub> ‡		V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0 to 5.5 V, V <sub>I</sub> = 0, Switch OFF, V <sub>IN</sub> = V <sub>CC</sub> or GND			±1	μA
I <sub>off</sub>		V <sub>CC</sub> = 0,	V <sub>O</sub> = 0 to 5.5 V, V <sub>I</sub> = 0			1	μA
I <sub>CC</sub>		V <sub>CC</sub> = 3.6 V,	I <sub>I/O</sub> = 0, Switch ON or OFF, V <sub>IN</sub> = V <sub>CC</sub> or GND		0.7	2	mA
ΔI <sub>CC</sub> §	Control inputs	V <sub>CC</sub> = 3.6 V,	One input at 3 V, Other inputs at V <sub>CC</sub> or GND			30	μA
I <sub>CCD</sub> ¶		V <sub>CC</sub> = 3.6 V,	A and B ports open, Control input switching at 50% duty cycle		0.14	0.15	mA/ MHz
C <sub>in</sub>		V <sub>CC</sub> = 3.3 V,	V <sub>IN</sub> = 5.5 V, 3.3 V, or 0		2.5	3.5	pF
C <sub>io</sub> (OFF)		V <sub>CC</sub> = 3.3 V,	Switch OFF, V <sub>IN</sub> = V <sub>CC</sub> or GND, V <sub>I/O</sub> = 5.5 V, 3.3 V, or 0		3.5	5	pF
C <sub>io</sub> (ON)		V <sub>CC</sub> = 3.3 V,	Switch ON, V <sub>IN</sub> = V <sub>CC</sub> or GND, V <sub>I/O</sub> = 5.5 V, 3.3 V, or 0		9	11	pF
r <sub>on</sub> #	V <sub>CC</sub> = 2.3 V, TYP at V <sub>CC</sub> = 2.5 V	V <sub>I</sub> = 0,	I <sub>O</sub> = 30 mA		4	8	Ω
		V <sub>I</sub> = 1.7 V,	I <sub>O</sub> = -15 mA		5	9	
	V <sub>CC</sub> = 3 V	V <sub>I</sub> = 0,	I <sub>O</sub> = 30 mA		4	6	
		V <sub>I</sub> = 2.4 V,	I <sub>O</sub> = -15 mA		5	8	

V<sub>IN</sub> and I<sub>IN</sub> refer to control inputs. V<sub>I</sub>, V<sub>O</sub>, I<sub>I</sub>, and I<sub>O</sub> refer to data pins.

† All typical values are at V<sub>CC</sub> = 3.3 V (unless otherwise noted), T<sub>A</sub> = 25°C.

‡ For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V<sub>CC</sub> or GND.

¶ This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).

# Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
f <sub>OE</sub>	$\overline{OE}$	A or B		10		20	MHz
t <sub>pd</sub> *	A or B	B or A		0.12		0.2	ns
t <sub>en</sub>	$\overline{OE}$	A or B	2.8	7.1	2.5	5.9	ns
t <sub>dis</sub>	$\overline{OE}$	A or B	1	5.8	1.5	5.8	ns

|| Maximum switching frequency for control input (V<sub>O</sub> > V<sub>CC</sub>, V<sub>I</sub> = 5 V, R<sub>L</sub> ≥ 1 MΩ, C<sub>L</sub> = 0)

\* The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



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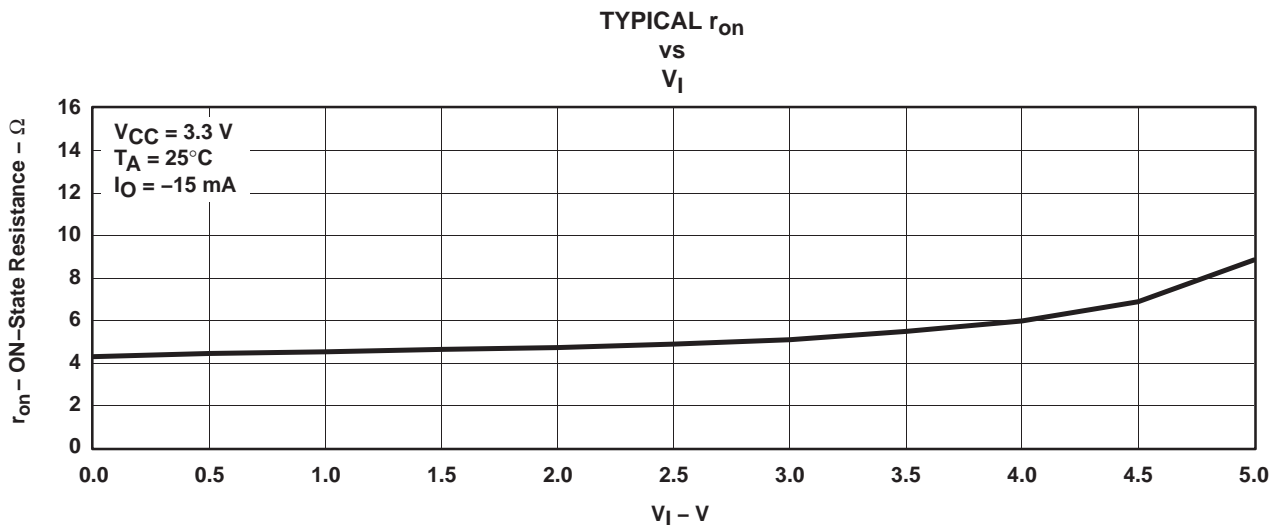


Figure 1. Typical  $r_{on}$  vs  $V_I$ ,  $V_{CC} = 3.3$  V and  $I_O = -15$  mA

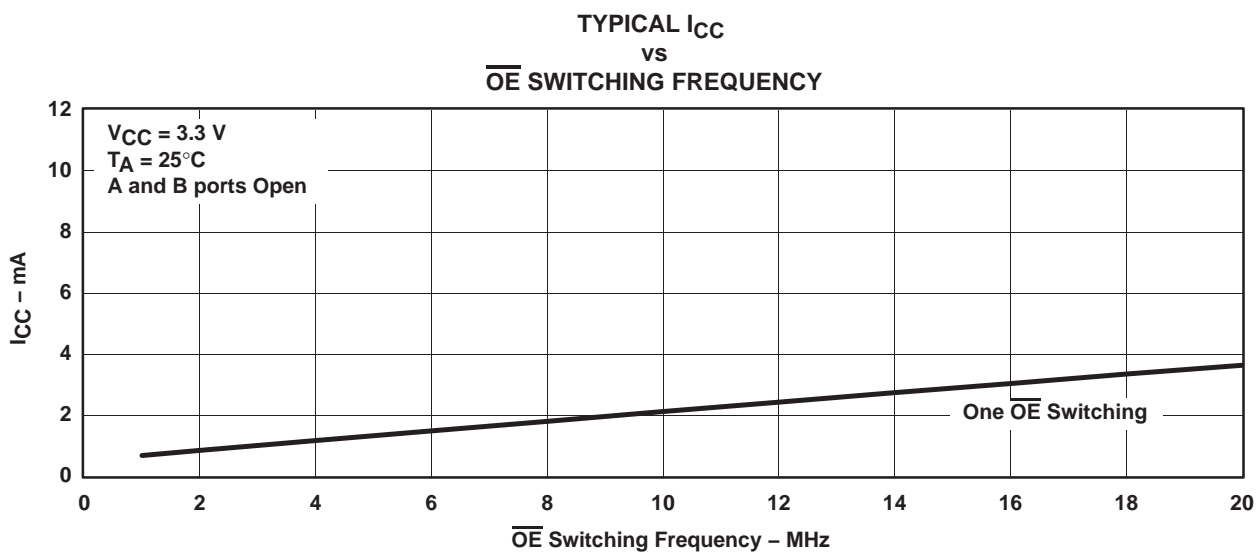
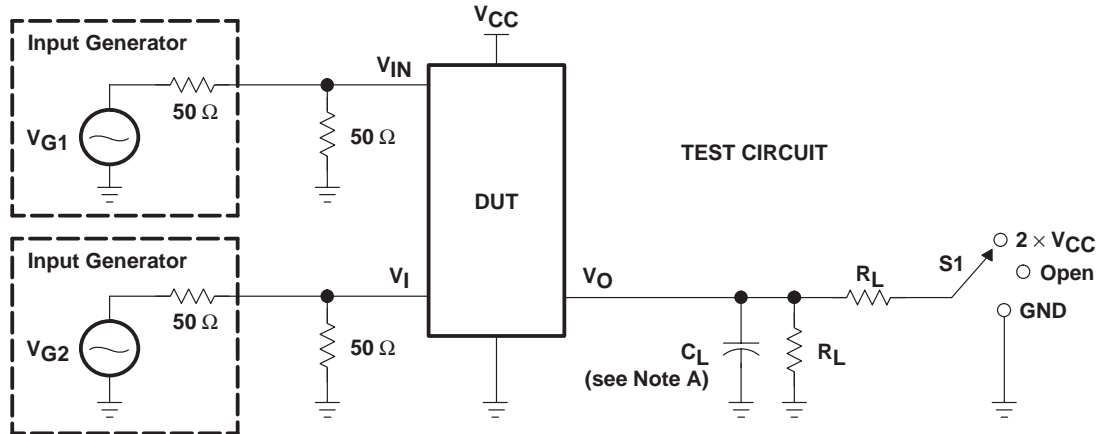
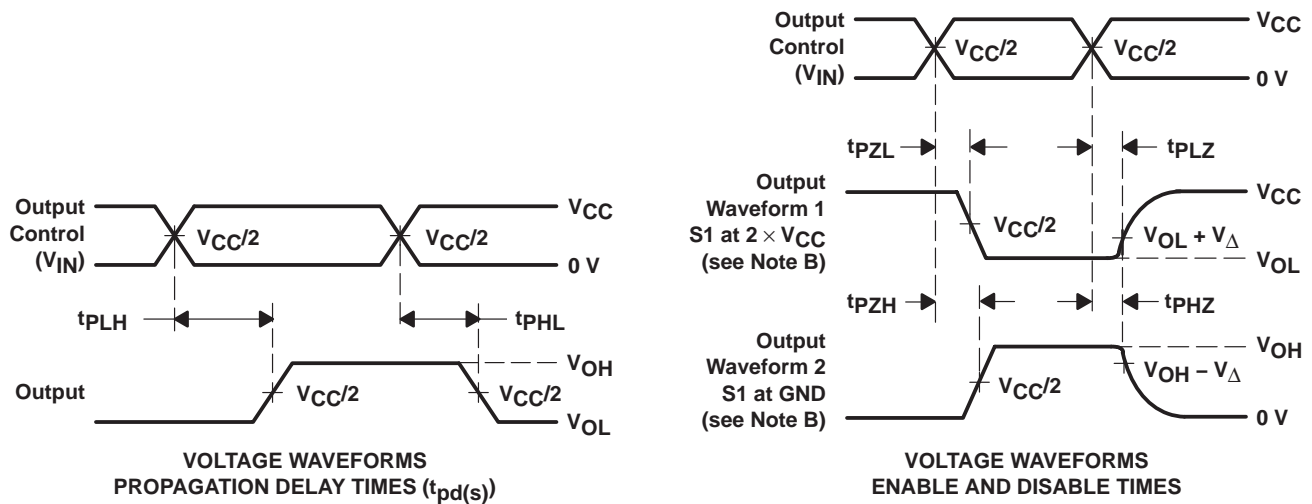


Figure 2. Typical  $I_{CC}$  vs  $\overline{OE}$  Switching Frequency,  $V_{CC} = 3.3$  V

**PARAMETER MEASUREMENT INFORMATION**



TEST	V <sub>CC</sub>	S1	R <sub>L</sub>	V <sub>I</sub>	C <sub>L</sub>	V <sub>Δ</sub>
t <sub>pd</sub> (s)	2.5 V ± 0.2 V	Open	500 Ω	V <sub>CC</sub> or GND	30 pF	
	3.3 V ± 0.3 V	Open	500 Ω	V <sub>CC</sub> or GND	50 pF	
t <sub>PLZ</sub> /t <sub>PZL</sub>	2.5 V ± 0.2 V	2 × V <sub>CC</sub>	500 Ω	GND	30 pF	0.15 V
	3.3 V ± 0.3 V	2 × V <sub>CC</sub>	500 Ω	GND	50 pF	0.3 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	2.5 V ± 0.2 V	GND	500 Ω	V <sub>CC</sub>	30 pF	0.15 V
	3.3 V ± 0.3 V	GND	500 Ω	V <sub>CC</sub>	50 pF	0.3 V



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.  
 F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.  
 G. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>(s). The t<sub>pd</sub> propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).  
 H. All parameters and waveforms are not applicable to all devices.

**Figure 3. Test Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74CB3Q3244DBQRE4	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
74CB3Q3244DBQRG4	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
74CB3Q3244DGVRE4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CB3Q3244DGVRG4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CB3Q3244RGYRG4	ACTIVE	QFN	RGY	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN74CB3Q3244DBQR	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN74CB3Q3244DBR	PREVIEW	SSOP	DB	16	2000	TBD	Call TI	Call TI
SN74CB3Q3244DGV	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3Q3244DW	PREVIEW	SOIC	DW	16	40	TBD	Call TI	Call TI
SN74CB3Q3244DWR	PREVIEW	SOIC	DW	16	2000	TBD	Call TI	Call TI
SN74CB3Q3244GQNR	NRND	BGA MICROSTAR JUNIOR	GQN	20	1000	TBD	SNPB	Level-1-240C-UNLIM
SN74CB3Q3244PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3Q3244PWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3Q3244PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3Q3244PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3Q3244PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3Q3244PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3Q3244RGYR	ACTIVE	QFN	RGY	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN74CB3Q3244ZQNR	ACTIVE	BGA MICROSTAR JUNIOR	ZQN	20	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements



for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

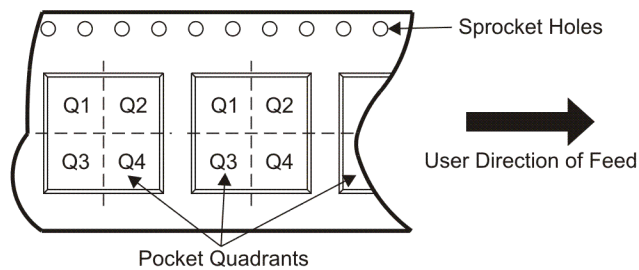
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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3Q3244DBQR	SSOP/ QSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CB3Q3244DGVR	TVSOP	DGV	20	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
SN74CB3Q3244GQNR	BGA MICROSTAR JUNIOR	GQN	20	1000	330.0	12.4	3.3	4.3	1.5	8.0	12.0	Q1
SN74CB3Q3244PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74CB3Q3244RGYR	QFN	RGY	20	1000	180.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
SN74CB3Q3244ZQNR	BGA MICROSTAR JUNIOR	ZQN	20	1000	330.0	12.4	3.3	4.3	1.5	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3Q3244DBQR	SSOP/QSOP	DBQ	20	2500	346.0	346.0	33.0
SN74CB3Q3244DGVR	TVSOP	DGV	20	2000	346.0	346.0	29.0
SN74CB3Q3244GQNR	BGA MICROSTAR JUNIOR	GQN	20	1000	346.0	346.0	29.0
SN74CB3Q3244PWR	TSSOP	PW	20	2000	346.0	346.0	33.0
SN74CB3Q3244RGYR	QFN	RGY	20	1000	190.5	212.7	31.8
SN74CB3Q3244ZQNR	BGA MICROSTAR JUNIOR	ZQN	20	1000	346.0	346.0	29.0

ZQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-285 variation BC-2.
  - D. This package is lead-free. Refer to the 20 GQN package (drawing 4200704) for tin-lead (SnPb).

GQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-285 variation BC-2.
  - D. This package is tin-lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead-free.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



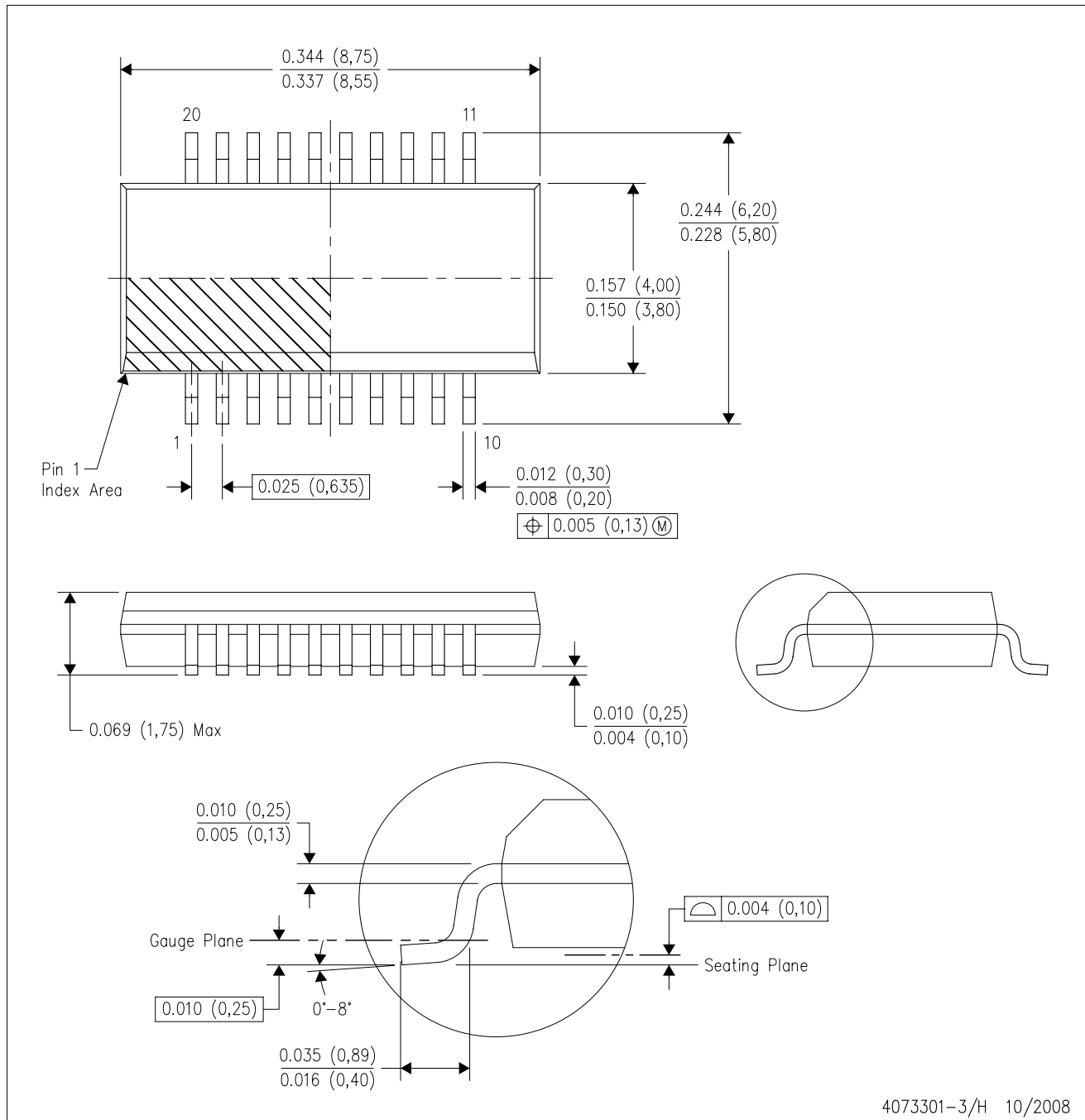
4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194



DBQ (R-PDSO-G20)

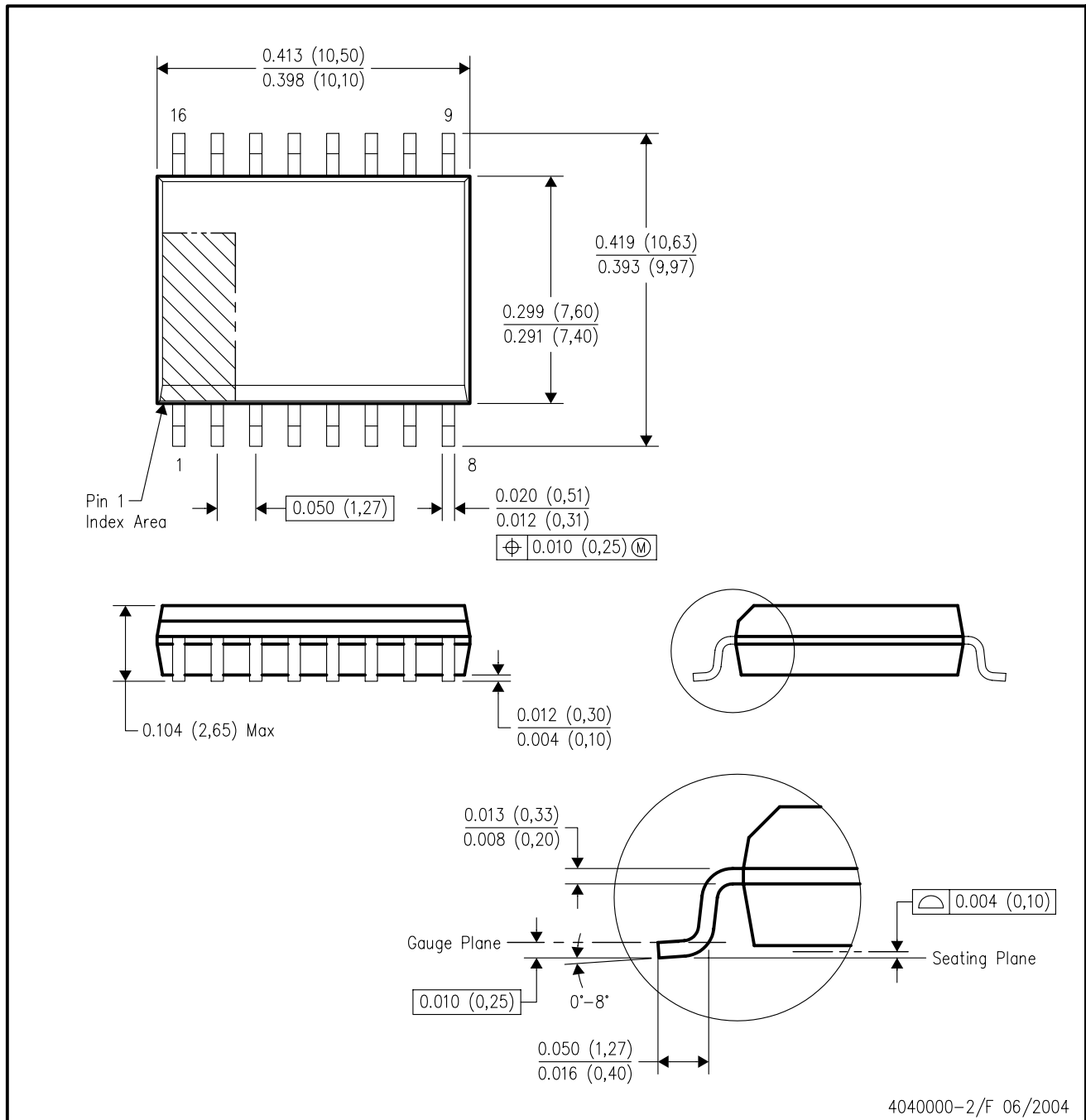
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - D. Falls within JEDEC MO-137 variation AD.

DW (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE

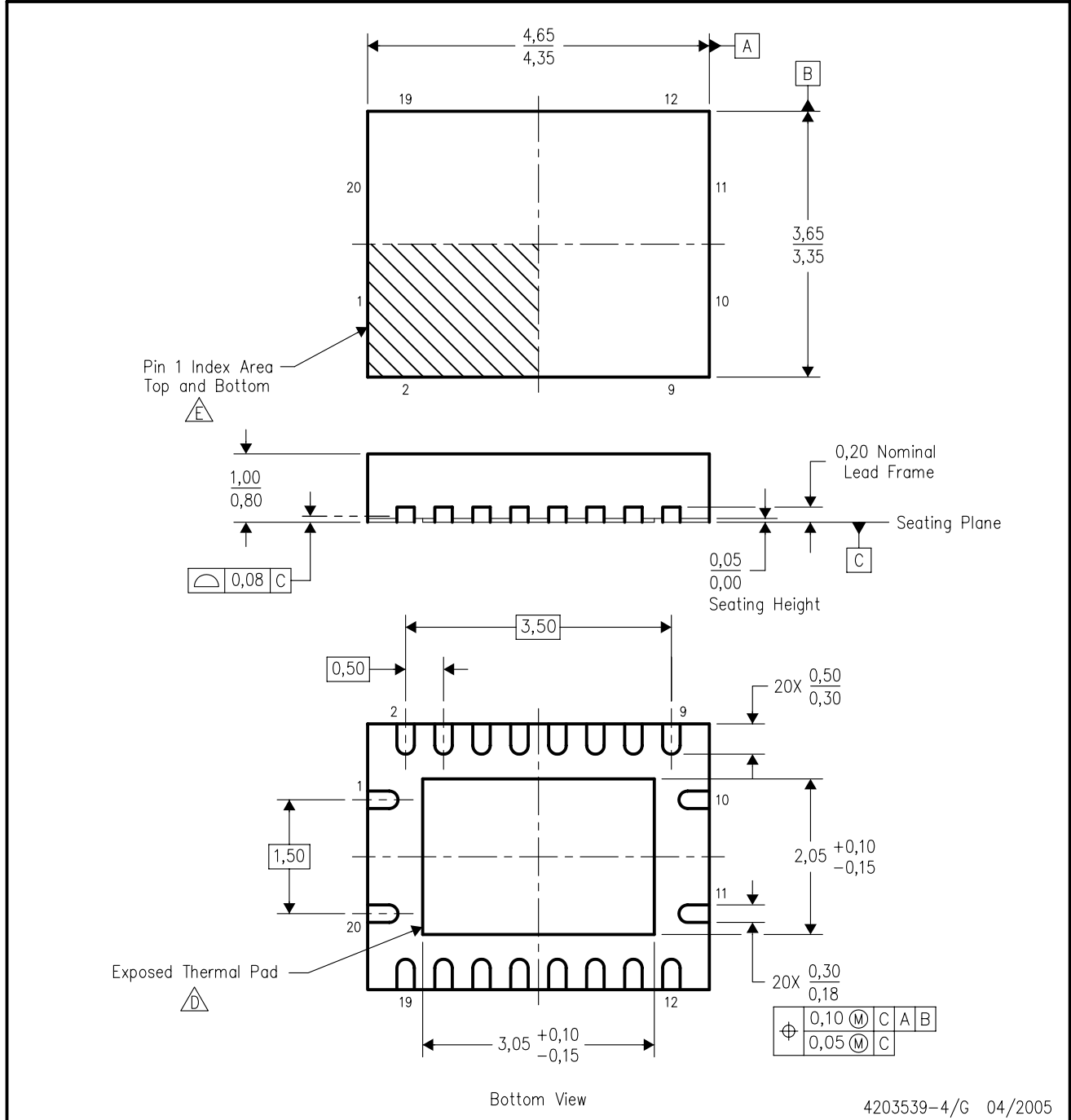




4040000-2/F 06/2004

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AA.

RGY (R-PQFP-N20)

PLASTIC QUAD FLATPACK



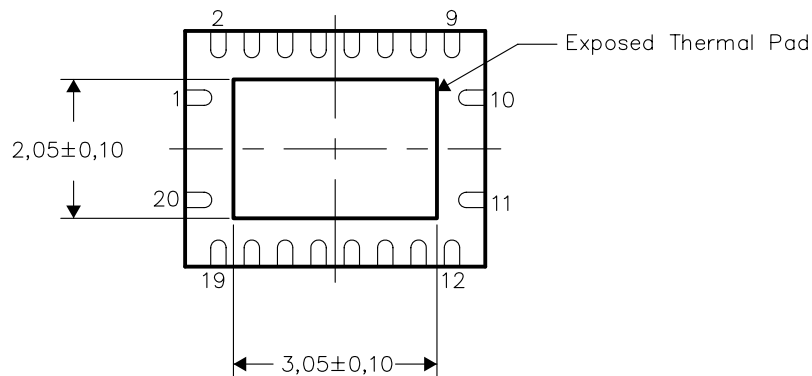
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  -  The package thermal pad must be soldered to the board for thermal and mechanical performance.
  -  Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - F. Package complies to JEDEC MO-241 variation BC.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

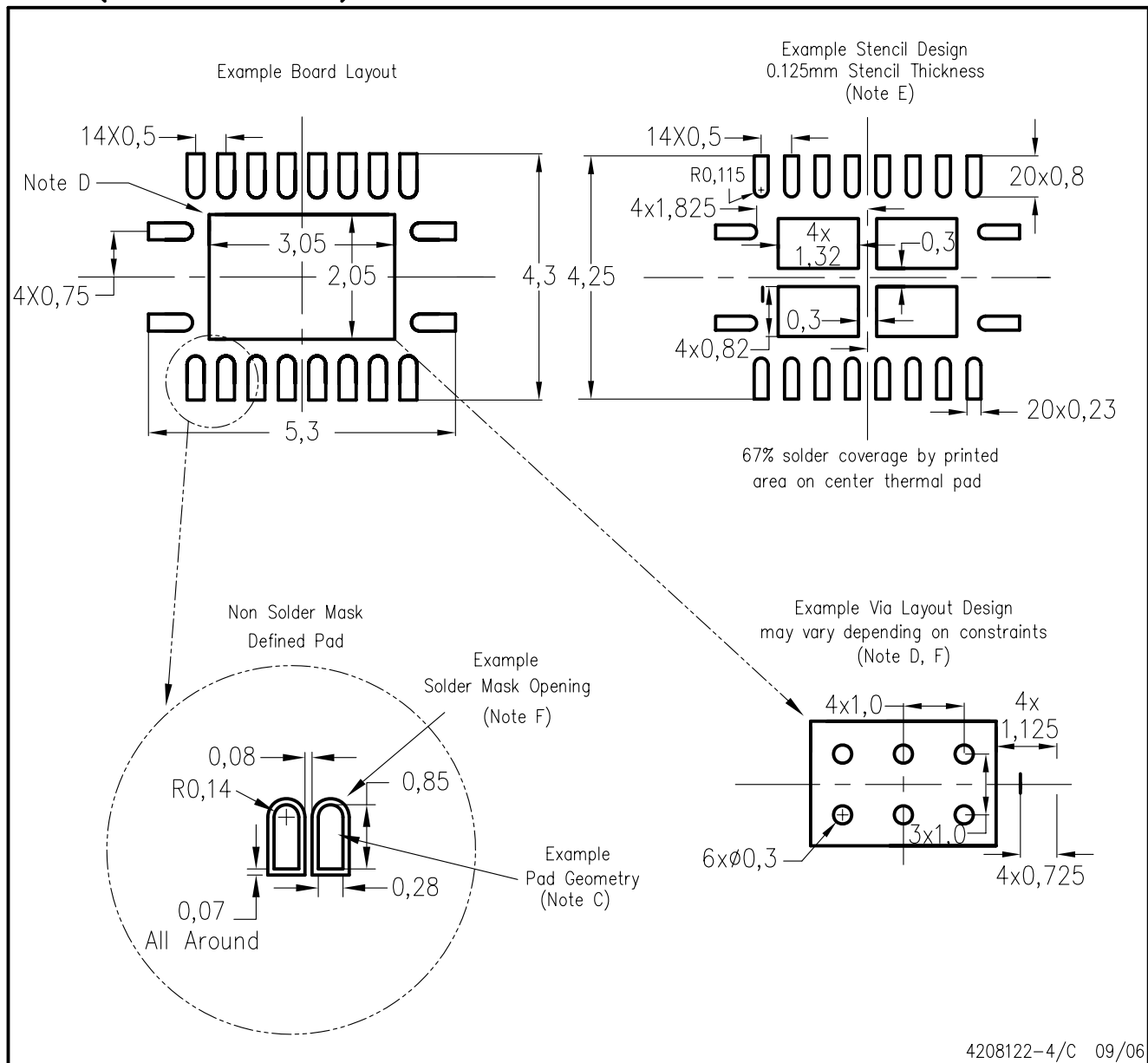


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGY (R-PQFP-N20)



4208122-4/C 09/06

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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