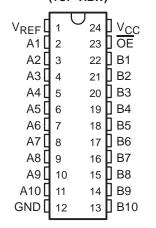
- Enable Signal Is SSTL_2 Compatible
- Flow-Through Architecture Optimizes PCB Layout
- Designed for Use With 200 Mbit/s Double Data-Rate (DDR) SDRAM Applications
- Switch On-State Resistance Is Designed to Eliminate Series Resistor to DDR SDRAM
- Internal 10-kΩ Pulldown Resistors to Ground on B Port
- Internal 50-kΩ Pullup Resistor on Output-Enable Input
- Rail-to-Rail Switching on Data I/O Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

DBQ, DGV, DW, OR PW PACKAGE (TOP VIEW)



description/ordering information

This 10-bit FET bus switch is designed for 3-V to 3.6-V V_{CC} operation and SSTL_2 output-enable (OE) input levels.

When \overline{OE} is low, the 10-bit bus switch is on, and port A is connected to port B. When \overline{OE} is high, the switch is open, and the high-impedance state exists between the two ports. There are 10-k Ω pulldown resistors to ground on the B port.

The FET switch on-state resistance is designed to replace the series terminating resistor in the SSTL_2 data path.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

ORDERING INFORMATION

TA	PACK	AGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	QSOP – DBQ	Tape and reel	SN74CBTLV3857DBQR	CL857
	0010 014	Tube	SN74CBTLV3857DW	CDTI VOOEZ
-40°C to 85°C	SOIC - DW	Tape and reel	SN74CBTLV3857DWR	CBTLV3857
	TSSOP – PW Tape and reel		SN74CBTLV3857PWR	CL857
	TVSOP - DGV	Tape and reel	SN74CBTLV3857DGVR	CL857

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

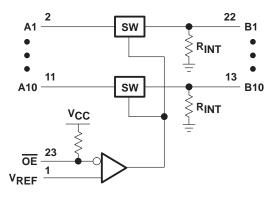
INPUT OE	FUNCTION
L	A port = B port
Н	Disconnect



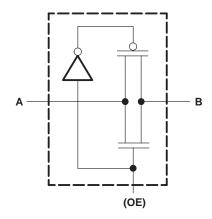
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logic diagram (positive logic)



simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		0.5 V to 4.6 V
Input voltage range (OE only), V _I (see Note 1)		
Input voltage range (except OE), V _I (see Note	1)	–0.5 V to 4.6 V
Continuous channel current	• • • • • • • • • • • • • • • • • • • •	48 mA
Input clamp current, I _{IK} (V _{I/O} < 0)		–50 mA
Package thermal impedance, θ _{JA} (see Note 2):	: DBQ package	61°C/W
	DGV package	86°C/W
	DW package	46°C/W
	PW package	88°C/W
Storage temperature range, T _{stq}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.



recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	3	3.3	3.6	V
V _{REF}	Reference voltage (0.38 × V _{CC})	1.15	1.25	1.35	V
V _{IH}	AC high-level control input voltage	V _{REF} + 350 mV			V
VIL	AC low-level control input voltage			V _{REF} - 350 mV	V
VIH	DC high-level control input voltage	V _{REF} + 180 mV			V
V _{IL}	DC low-level control input voltage			V _{REF} – 180 mV	V
TA	Operating free-air temperature	-40		85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CONDITIO	MIN	TYP [†]	MAX	UNIT		
VIK		V _{CC} = 3 V,	$I_{I} = -18 \text{ mA}$				-1.2	V	
	ŌE						±1	mA	
١.	A port		ON	D			±5	μΑ	
ij	B port	V _{CC} = 3.6 V,	$V_I = V_{CC}$ or GN	U			±1	mA	
	VREF					±5	μΑ		
Icc		$V_{CC} = 3.6 \text{ V},$	$I_{O} = 0$,	$V_I = V_{CC}$ or GND			25	mA	
Ci	Control inputs	V _I = 3 V or 0				3.5		pF	
C _{io(C}	OFF)	$V_{O} = 3 \text{ V or } 0,$	OE = VCC			5		pF	
			V _I = 0,	I _I = 24 mA		5	8		
. +		.,	$V_{I} = 0.9 V$,	I _I = 24 mA		6	11		
r _{on} ‡		ACC = 3 A	V _I = 1.25 V,	I _I = 24 mA		7	13	Ω	
			$V_{I} = 1.6 \text{ V}, \qquad I_{I} = 24 \text{ mA}$			9	40		
r _{off} ‡		VCC = 0	V _{CC} = 0					МО	
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V},$	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}, \qquad V_I = 1.65 \text{ V}, \qquad \overline{OE} = V_{CC}$					MΩ	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

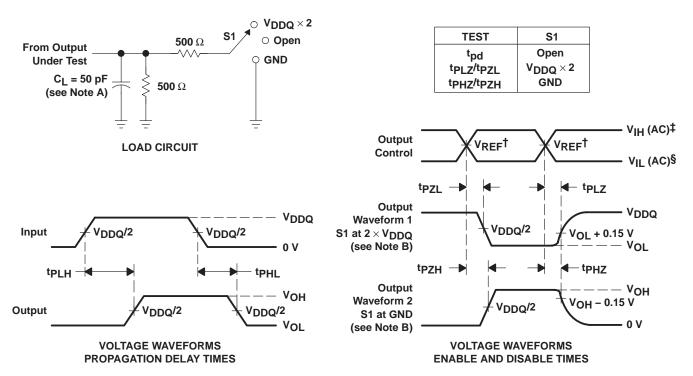
PARAMETER	FROM	TO (OUTPUT)	V _{CC} =	UNIT	
	(INPUT)	(OUTPUT)	MIN	MAX	
t _{pd} §	A or B	B or A		0.25	ns
^t en	ŌĒ	A or B	1.4	4.2	ns
^t dis	ŌĒ	A or B	1.4	4.8	ns

[§] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



[‡] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. Resistance is determined by the lower of the voltages of the two (A or B) terminals.

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ AND $V_{DDQ} = 2.5 \pm 0.2 \text{ V}$



 $^{^{\}dagger}$ V_{REF} = $0.38 \times$ V_{CC}

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_r \leq 2$ ns, $t_f \leq 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



 $V_{IH}(AC) = V_{REF} + 350 \text{ mV}$

[§] V_{IL}(AC) = V_{REF} - 350 mV







PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74CBTLV3857DBQRE4	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
74CBTLV3857DBQRG4	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
74CBTLV3857DGVRE4	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBTLV3857DGVRG4	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBTLV3857DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBTLV3857DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBTLV3857PWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBTLV3857PWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTLV3857DBQR	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN74CBTLV3857DGVR	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTLV3857DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTLV3857DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTLV3857DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTLV3857DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTLV3857PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



PACKAGE OPTION ADDENDUM

24-May-2007

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBTLV3857DBQR	SSOP/ QSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CBTLV3857DGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBTLV3857DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74CBTLV3857PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBTLV3857DBQR	SSOP/QSOP	DBQ	24	2500	346.0	346.0	33.0
SN74CBTLV3857DGVR	TVSOP	DGV	24	2000	346.0	346.0	29.0
SN74CBTLV3857DWR	SOIC	DW	24	2000	346.0	346.0	41.0
SN74CBTLV3857PWR	TSSOP	PW	24	2000	346.0	346.0	33.0

DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194

DW (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AD.



DBQ (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



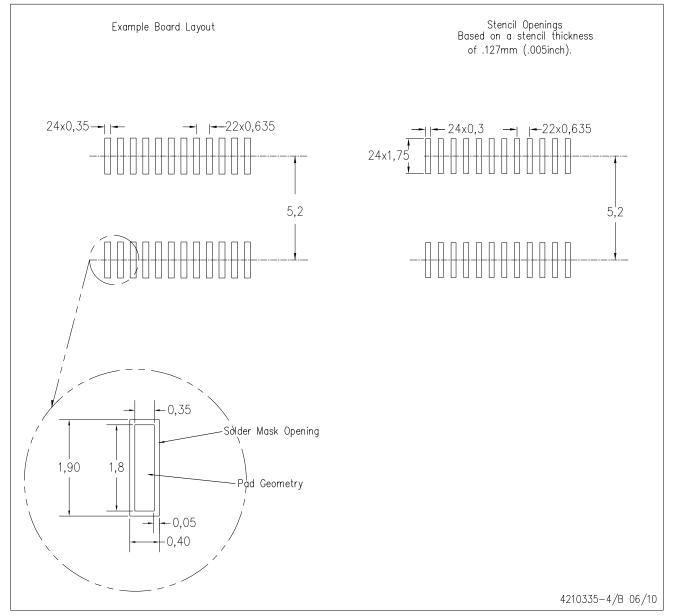
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
- D. Falls within JEDEC MO-137 variation AE.



DBQ (R-PDSO-G24)

PLASTIC SMALL OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



PW (R-PDSO-G**)

14 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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