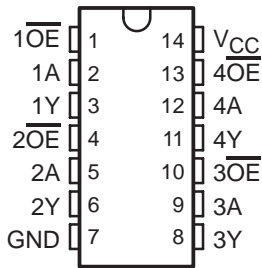


# SN54LV125A, SN74LV125A QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

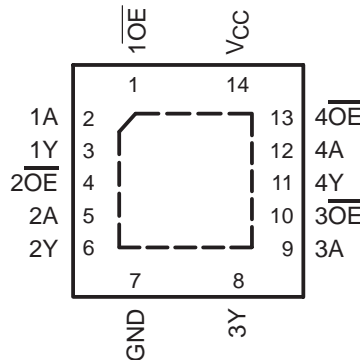
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- 2-V to 5.5-V  $V_{CC}$  Operation
- Max  $t_{pd}$  of 6 ns at 5 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $>2.3$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

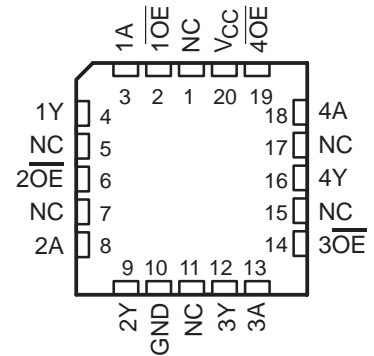
SN54LV125A ... J OR W PACKAGE  
SN74LV125A ... D, DB, DGV, N, NS,  
OR PW PACKAGE  
(TOP VIEW)



SN74LV125A ... RGY PACKAGE  
(TOP VIEW)



SN54LV125A ... FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The 'LV125A quadruple bus buffer gates are designed for 2-V to 5.5-V  $V_{CC}$  operation.

These devices feature independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ( $\overline{OE}$ ) input is high.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 25	SN74LV125AN	SN74LV125AN
	QFN – RGY	Reel of 1000	SN74LV125ARGYR	LV125A
	SOIC – D	Tube of 50	SN74LV125AD	LV125A
		Reel of 2500	SN74LV125ADR	
	SOP – NS	Reel of 2000	SN74LV125ANSR	74LV125A
	SSOP – DB	Reel of 2000	SN74LV125ADBR	LV125A
	TSSOP – PW	Tube of 90	SN74LV125APW	LV125A
Reel of 2000		SN74LV125APWR		
Reel of 250		SN74LV125APWT		
TVSOP – DGV	Reel of 2000	SN74LV125ADGVR	LV125A	
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54LV125AJ	SNJ54LV125AJ
	CFP – W	Tube of 150	SNJ54LV125AW	SNJ54LV125AW
	LCCC – FK	Tube of 55	SNJ54LV125AFK	SNJ54LV125AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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# SN54LV125A, SN74LV125A QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

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## description/ordering information (continued)

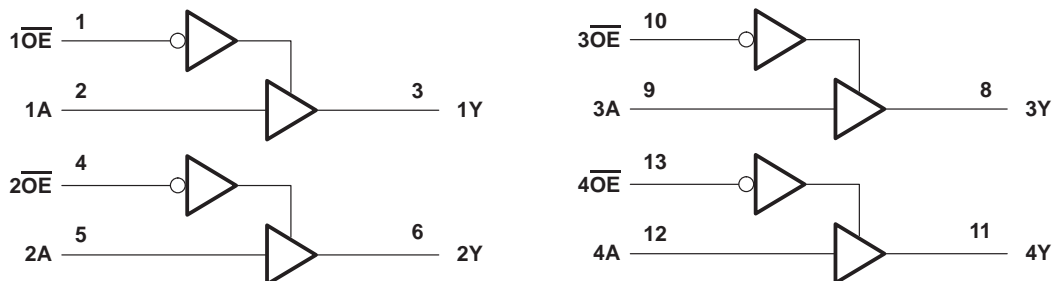
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

FUNCTION TABLE  
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

## logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, RGY, and W packages.

**SN54LV125A, SN74LV125A**  
**QUADRUPLE BUS BUFFER GATES**  
**WITH 3-STATE OUTPUTS**

SCES124L – DECEMBER 1997 – REVISED APRIL 2005

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) .....	-0.5 V to 7 V
Output voltage range, $V_O$ (see Notes 1 and 2) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 35$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 70$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): D package .....	86°C/W
(see Note 3): DB package .....	96°C/W
(see Note 3): DGV package .....	127°C/W
(see Note 3): N package .....	80°C/W
(see Note 3): NS package .....	76°C/W
(see Note 3): PW package .....	113°C/W
(see Note 4): RGY package .....	47°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.  
2. This value is limited to 5.5 V maximum.  
3. The package thermal impedance is calculated in accordance with JESD 51-7.  
4. The package thermal impedance is calculated in accordance with JESD 51-5.



# SN54LV125A, SN74LV125A QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCES124L – DECEMBER 1997 – REVISED APRIL 2005

## recommended operating conditions (see Note 5)

		SN54LV125A		SN74LV125A		UNIT	
		MIN	MAX	MIN	MAX		
$V_{CC}$	Supply voltage	2	5.5	2	5.5	V	
$V_{IH}$	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5	1.5		V	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$			
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$			
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$			
$V_{IL}$	Low-level input voltage	$V_{CC} = 2\text{ V}$	0.5	0.5		V	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$			
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$			
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$			
$V_I$	Input voltage	0	5.5	0	5.5	V	
$V_O$	Output voltage	High or low state	0	$V_{CC}$	0	$V_{CC}$	V
		3-state	0	5.5	0	5.5	
$I_{OH}$	High-level output current	$V_{CC} = 2\text{ V}$		-50	-50	$\mu\text{A}$	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		-2	-2	mA	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		-8	-8		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		-16	-16		
$I_{OL}$	Low-level output current	$V_{CC} = 2\text{ V}$		50	50	$\mu\text{A}$	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		2	2	mA	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		8	8		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		16	16		
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		200	200	ns/V	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		100	100		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		20	20		
$T_A$	Operating free-air temperature	-55	125	-40	85	$^{\circ}\text{C}$	

NOTE 5: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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# SN54LV125A, SN74LV125A QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCES124L – DECEMBER 1997 – REVISED APRIL 2005

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LV125A			SN74LV125A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	2 V to 5.5 V	V <sub>CC</sub> -0.1			V <sub>CC</sub> -0.1			V
	I <sub>OH</sub> = -2 mA	2.3 V	2			2			
	I <sub>OH</sub> = -8 mA	3 V	2.48			2.48			
	I <sub>OH</sub> = -16 mA	4.5 V	3.8			3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V to 5.5 V				0.1			V
	I <sub>OL</sub> = 2 mA	2.3 V				0.4			
	I <sub>OL</sub> = 8 mA	3 V				0.44			
	I <sub>OL</sub> = 16 mA	4.5 V				0.55			
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V				±1			μA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V				±5			μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V				20			μA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0				5			μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V				1.6			pF
		5 V				1.6			

**switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			SN54LV125A		SN74LV125A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 15 pF	6.8*	13*		1*	15.5*	1	15.5	ns
t <sub>en</sub>	$\overline{\text{OE}}$	Y		7*	13*		1*	15.5*	1	15.5	
t <sub>dis</sub>	$\overline{\text{OE}}$	Y		5.1*	14.7*		1*	17*	1	17	
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 50 pF	8.7	16.5		1	18.5	1	18.5	ns
t <sub>en</sub>	$\overline{\text{OE}}$	Y		8.8	16.5		1	18.5	1	18.5	
t <sub>dis</sub>	$\overline{\text{OE}}$	Y		7.3	18.2		1	20.5	1	20.5	
t <sub>sk(o)</sub>						2				2	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			SN54LV125A		SN74LV125A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 15 pF	4.8*	8*		1*	9.5*	1	9.5	ns
t <sub>en</sub>	$\overline{\text{OE}}$	Y		4.8*	8*		1*	9.5*	1	9.5	
t <sub>dis</sub>	$\overline{\text{OE}}$	Y		4.1*	9.7*		1*	11.5*	1	11.5	
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 50 pF	6.1	11.5		1	13	1	13	ns
t <sub>en</sub>	$\overline{\text{OE}}$	Y		6.2	11.5		1	13	1	13	
t <sub>dis</sub>	$\overline{\text{OE}}$	Y		5.5	13.2		1	15	1	15	
t <sub>sk(o)</sub>						1.5				1.5	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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# SN54LV125A, SN74LV125A QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCES124L – DECEMBER 1997 – REVISED APRIL 2005

switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV125A		SN74LV125A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	Y	$C_L = 15\text{ pF}$	3.4*	5.5*	1*	6.5*	1	6.5	ns	
$t_{en}$	$\overline{OE}$	Y		3.4*	5.1*	1*	6*	1	6		
$t_{dis}$	$\overline{OE}$	Y		3.2*	6.8*	1*	8*	1	8		
$t_{pd}$	A	Y	$C_L = 50\text{ pF}$	4.3	7.5	1	8.5	1	8.5	ns	
$t_{en}$	$\overline{OE}$	Y		4.4	7.1	1	8	1	8		
$t_{dis}$	$\overline{OE}$	Y		4	8.8	1	10	1	10		
$t_{sk(o)}$						1			1		

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics,  $V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 6)

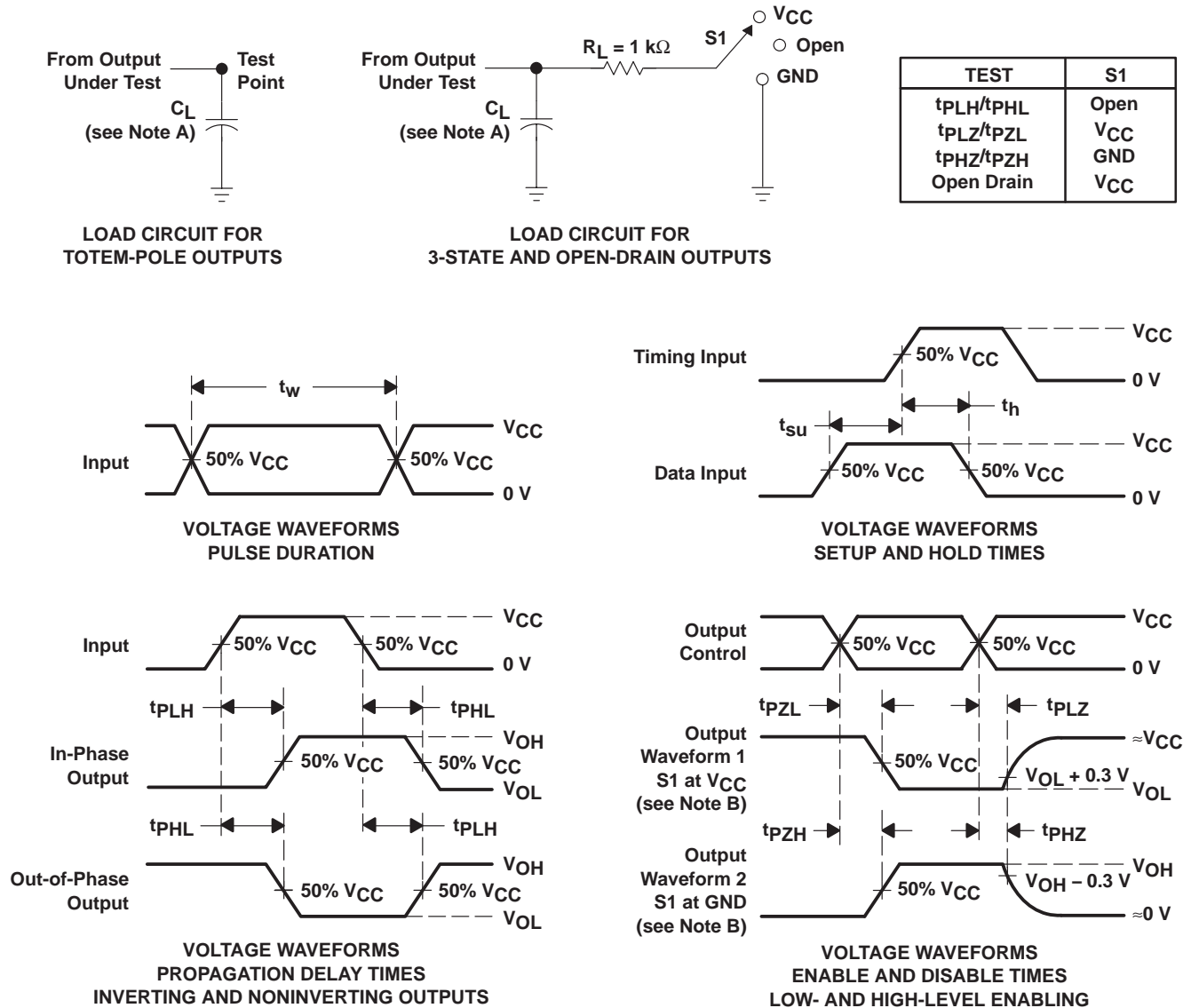
PARAMETER	SN74LV125A			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic $V_{OL}$		0.4	0.8	V
$V_{OL(V)}$ Quiet output, minimum dynamic $V_{OL}$		-0.3	-0.8	V
$V_{OH(V)}$ Quiet output, minimum dynamic $V_{OH}$		3		V
$V_{IH(D)}$ High-level dynamic input voltage	2.31			V
$V_{IL(D)}$ Low-level dynamic input voltage		0.99		V

NOTE 6: Characteristics are for surface-mount packages only.

operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$	3.3 V	15.5	pF
			5 V	17.6	

PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .  
 D. The outputs are measured one at a time, with one input transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .  
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LV125AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV125ADBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI
SN74LV125ADBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV125ADBRE4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV125ADBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV125ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV125ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV125ADGVR	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV125ADGVRE4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV125ADGVRG4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV125ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV125ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV125ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV125AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LV125ANE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LV125ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV125ANSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV125APW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV125APWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV125APWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV125APWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI
SN74LV125APWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV125APWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV125APWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV125APWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV125APWTE4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM



Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
						no Sb/Br)		
SN74LV125APWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV125ARGYR	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN74LV125ARGYRG4	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV125ADBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LV125ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV125ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV125ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV125APWR	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
SN74LV125ARGYR	QFN	RGY	14	1000	180.0	12.4	3.85	3.85	1.35	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



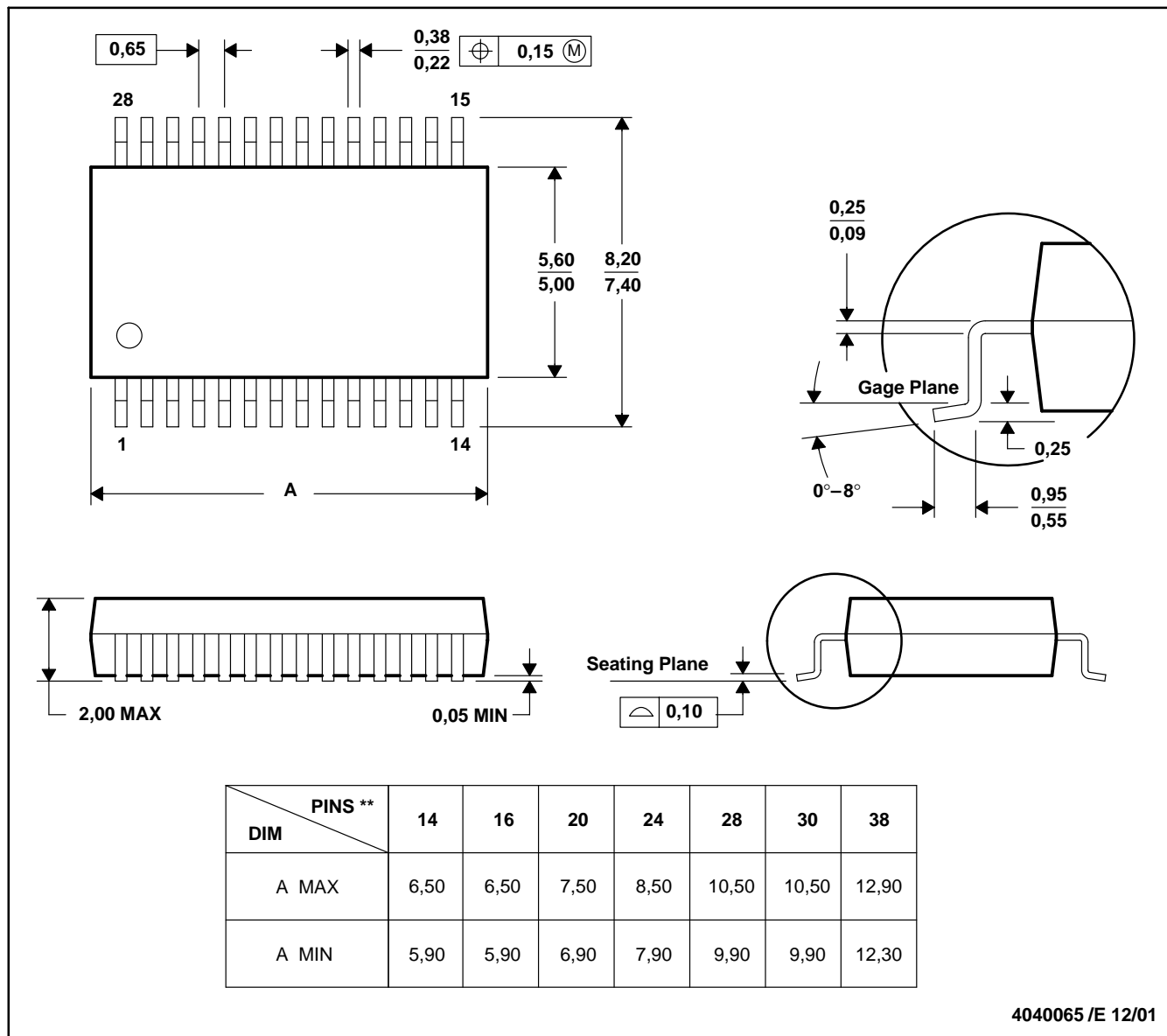
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV125ADBR	SSOP	DB	14	2000	346.0	346.0	33.0
SN74LV125ADGVR	TVSOP	DGV	14	2000	346.0	346.0	29.0
SN74LV125ADR	SOIC	D	14	2500	346.0	346.0	33.0
SN74LV125ANSR	SO	NS	14	2000	346.0	346.0	33.0
SN74LV125APWR	TSSOP	PW	14	2000	346.0	346.0	29.0
SN74LV125ARGYR	QFN	RGY	14	1000	190.5	212.7	31.8

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

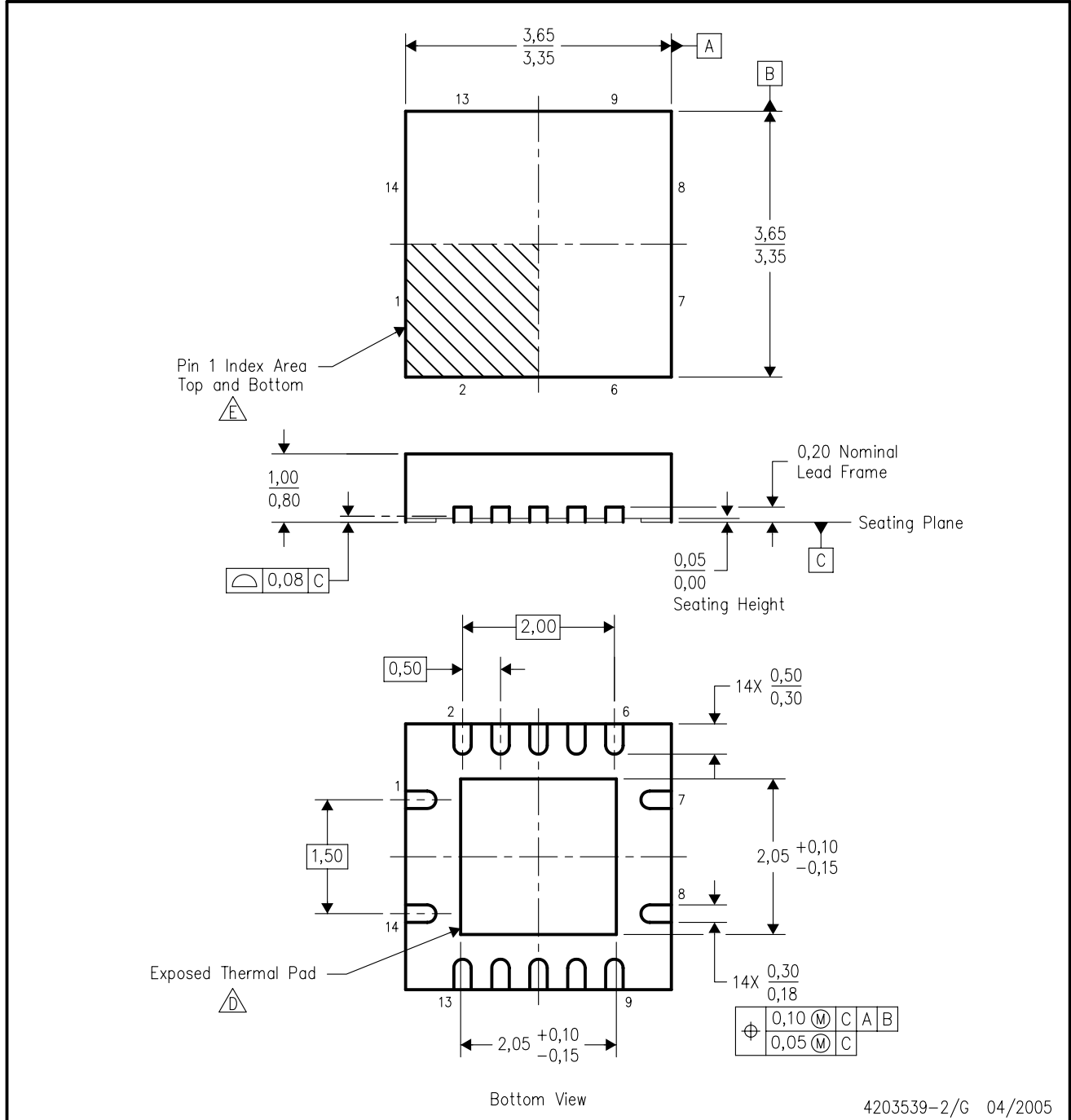
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

RGY (S-PQFP-N14)

PLASTIC QUAD FLATPACK



4203539-2/G 04/2005

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - F. Package complies to JEDEC MO-241 variation BA.

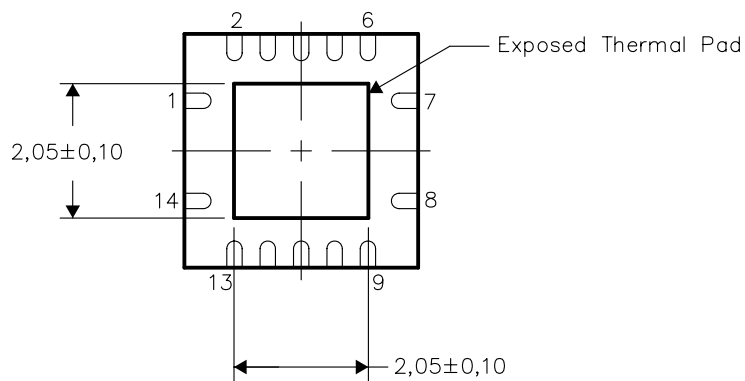


THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

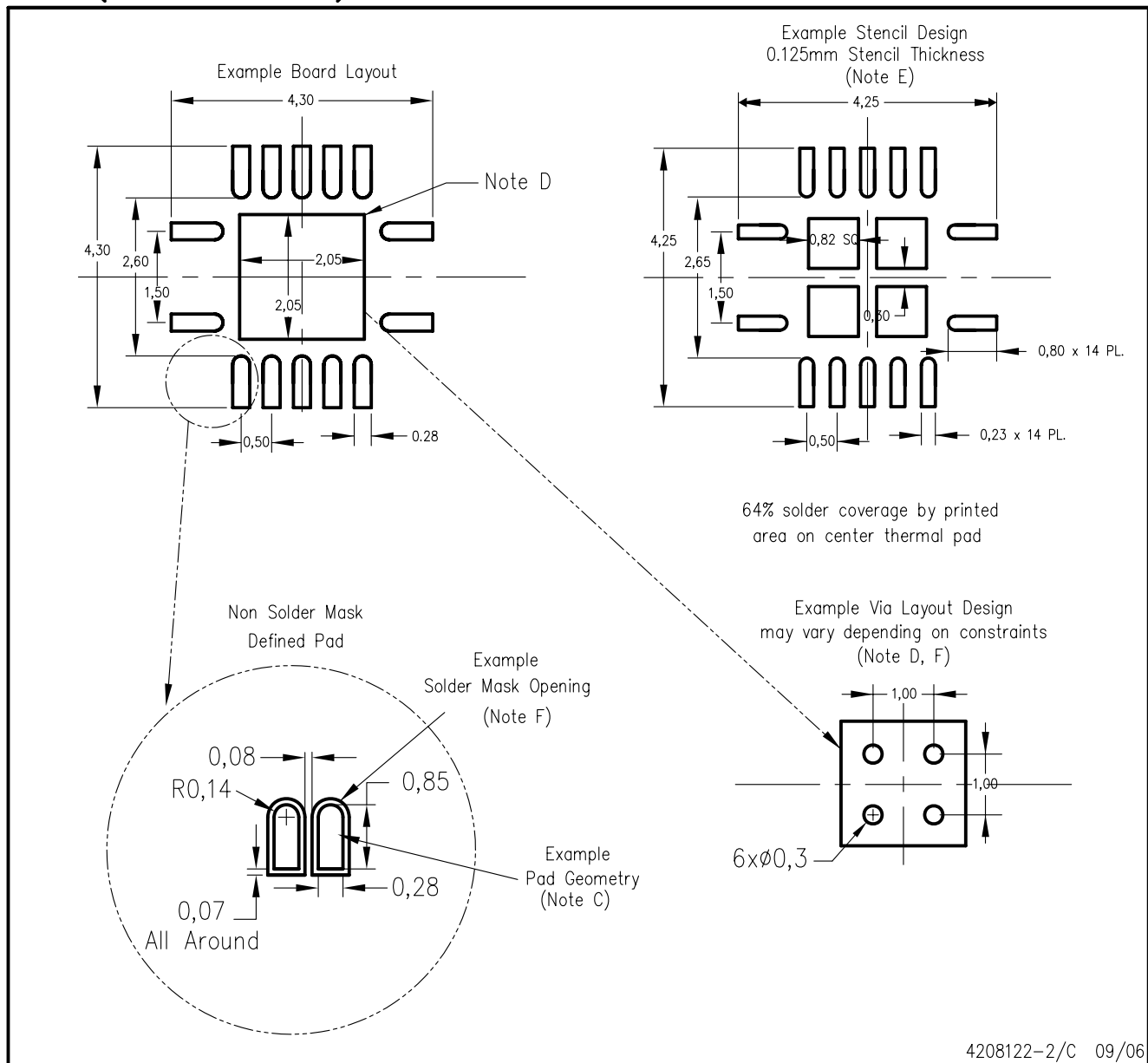


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

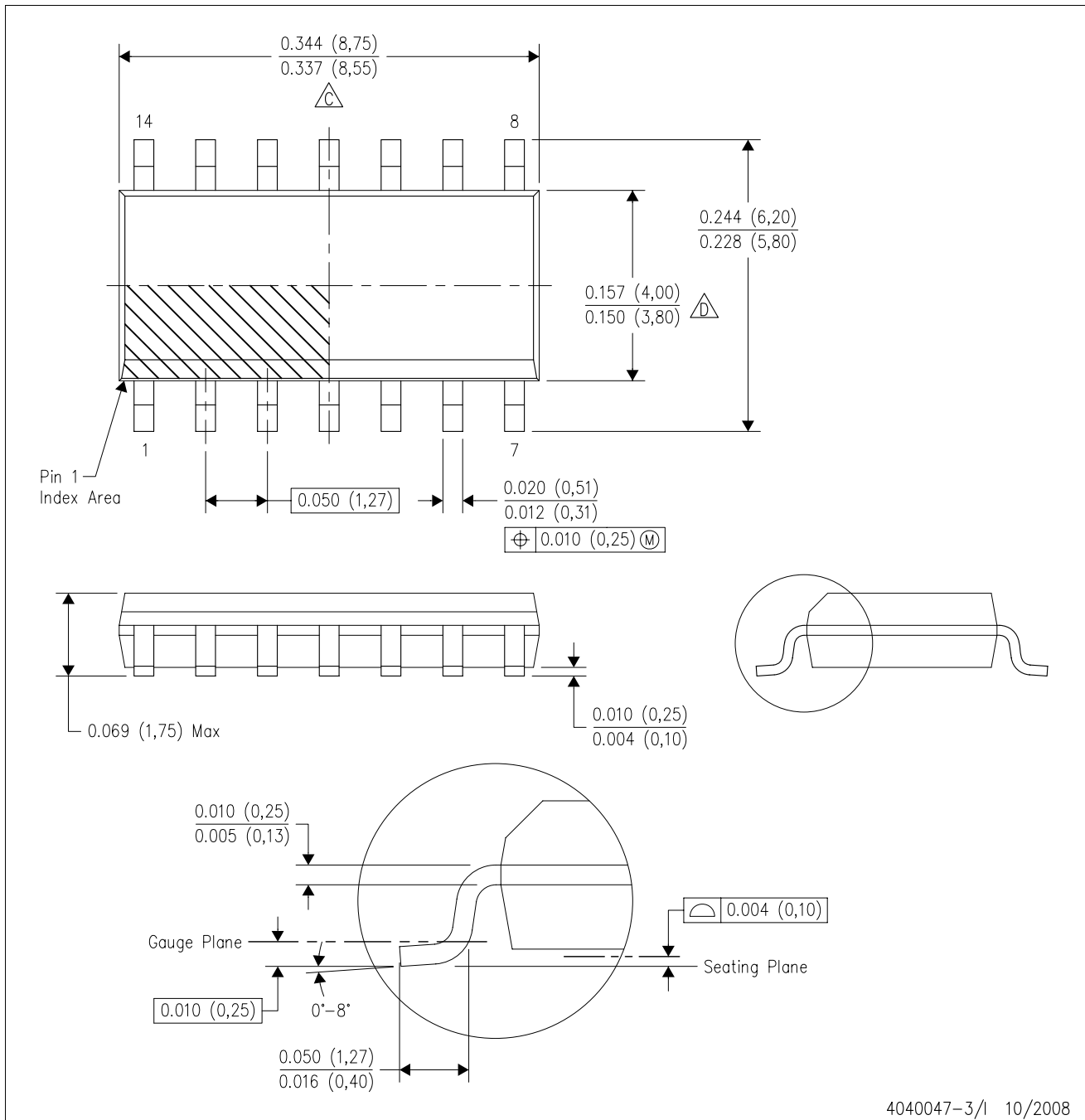
RGY (R-PQFP-N14)





- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  -  Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AB.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

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