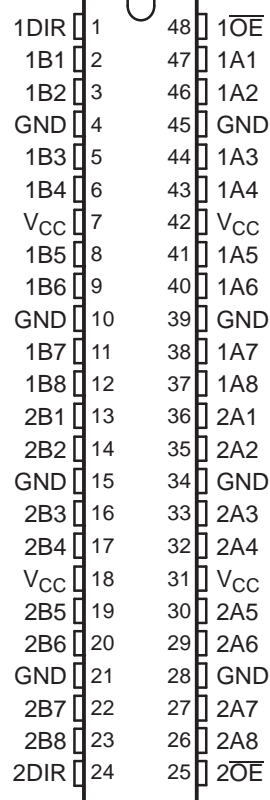


## FEATURES

- Members of the Texas Instruments Widebus™ Family
- A-Port Outputs Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Support Unregulated Battery Operation Down to 2.7 V
- Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- Distributed  $V_{CC}$  and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

SN54LVT162245A... WD PACKAGE  
SN74LVT162245A... DGG OR DL PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

The 'LVT162245A devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices are designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input and the output-enable ( $\overline{OE}$ ) input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports is always active and must have a logic HIGH or LOW level applied to prevent excess  $I_{CC}$  and  $I_{CCZ}$ .

The A-port outputs, which are designed to source or sink up to 12 mA, include equivalent 22-Ω series resistors to reduce overshoot and undershoot.

When  $V_{CC}$  is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

# SN54LVT162245A, SN74LVT162245A 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS714D—FEBRUARY 2000—REVISED NOVEMBER 2006

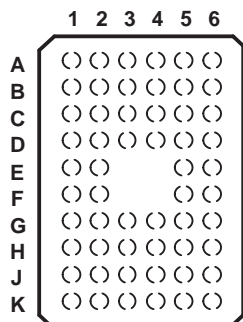
## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	FBGA – GRD	Reel of 1000	SN74LVT162245AGRDR	LZ245A
	FBGA – ZRD (Pb-free)		SN74LVT162245AZRDR	
	SSOP – DL	Tube of 25	SN74LVT162245ADL	LVT162245A
			SN74LVT162245ADLG4	
		Reel of 1000	SN74LVT162245ADLR	
			74LVT162245ADLRG4	
	TSSOP – DGG	Reel of 2000	SN74LVT162245ADGGR 74LVT162245ADGGRE4	LVT162245A
–55°C to 125°C	VFBGA – GQL	Reel of 1000	SN74LVT162245AGQLR	LZ245A
	VFBGA – ZQL (Pb-free)		SN74LVT162245AZQLR	
	CFP – WD	Tube	SNJ54LVT162245AWD <sup>(2)</sup>	SNJ54LVT162245AWD

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

(2) Product preview

**GQL OR ZQL PACKAGE  
(TOP VIEW)**

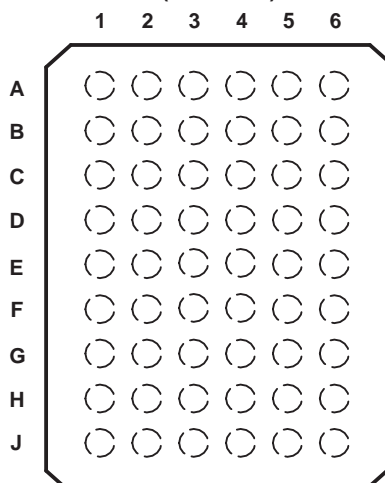


**TERMINAL ASSIGNMENTS<sup>(1)</sup>  
(56-Ball GQL/ZQL Package)**

	1	2	3	4	5	6
<b>A</b>	1DIR	NC	NC	NC	NC	1OE
<b>B</b>	1B2	1B1	GND	GND	1A1	1A2
<b>C</b>	1B4	1B3	V <sub>CC</sub>	V <sub>CC</sub>	1A3	1A4
<b>D</b>	1B6	1B5	GND	GND	1A5	1A6
<b>E</b>	1B8	1B7			1A7	1A8
<b>F</b>	2B1	2B2			2A2	2A1
<b>G</b>	2B3	2B4	GND	GND	2A4	2A3
<b>H</b>	2B5	2B6	V <sub>CC</sub>	V <sub>CC</sub>	2A6	2A5
<b>J</b>	2B7	2B8	GND	GND	2A8	2A7
<b>K</b>	2DIR	NC	NC	NC	NC	2OE

(1) NC – No internal connection

**GRD OR ZRD PACKAGE  
(TOP VIEW)**



**TERMINAL ASSIGNMENTS<sup>(1)</sup>  
(54-Ball GRD/ZRD Package)**

	1	2	3	4	5	6
<b>A</b>	1B1	NC	1DIR	1OE	NC	1A1
<b>B</b>	1B3	1B2	NC	NC	1A2	1A3
<b>C</b>	1B5	1B4	V <sub>CC</sub>	V <sub>CC</sub>	1A4	1A5
<b>D</b>	1B7	1B6	GND	GND	1A6	1A7
<b>E</b>	2B1	1B8	GND	GND	1A8	2A1
<b>F</b>	2B3	2B2	GND	GND	2A2	2A3
<b>G</b>	2B5	2B4	V <sub>CC</sub>	V <sub>CC</sub>	2A4	2A5
<b>H</b>	2B7	2B6	NC	NC	2A6	2A7
<b>J</b>	2B8	NC	2DIR	2OE	NC	2A8

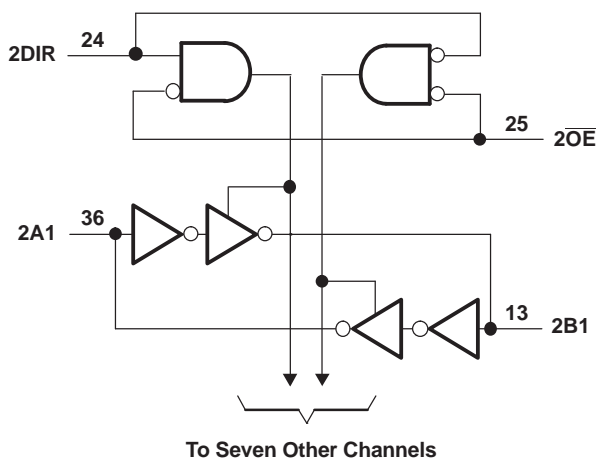
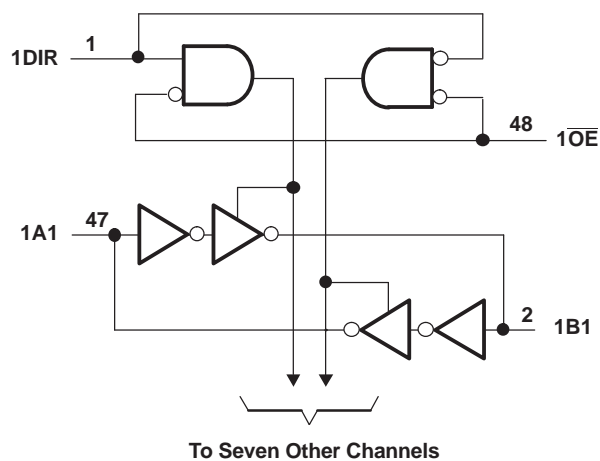
(1) NC – No internal connection

**FUNCTION TABLE<sup>(1)</sup>**  
**(EACH 8-BIT SECTION)**

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{\text{OE}}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os always are active.

### LOGIC DIAGRAM (POSITIVE LOGIC)



# SN54LVT162245A, SN74LVT162245A 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS714D—FEBRUARY 2000—REVISED NOVEMBER 2006

## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	−0.5	4.6	V
$V_I$	Input voltage range <sup>(2)</sup>	−0.5	7	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	−0.5	7	V
$V_O$	Voltage range applied to any output in the high state <sup>(2)</sup>	−0.5	$V_{CC} + 0.5$	V
$I_O$	Current into any output in the low state	SN54LVT162245A (B port)		96
		SN74LVT162245A (B port)		128
		A port		30
$I_O$	Current into any output in the high state <sup>(3)</sup>	SN54LVT162245A (B port)		48
		SN74LVT162245A (B port)		64
		A port		30
$I_{IK}$	Input clamp current	$V_I < 0$		−50
$I_{OK}$	Output clamp current	$V_O < 0$		−50
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DGG package		70
		DL package		63
		GQL/ZQL package		42
		GRD/ZRD package		36
$T_{stg}$	Storage temperature range	−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(3) This current flows only when the output is in the high state and  $V_O > V_{CC}$ .

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions<sup>(1)</sup>

			SN54LVT162245A <sup>(2)</sup>		SN74LVT162245A		UNIT
			MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage		2.7	3.6	2.7	3.6	V
V <sub>IH</sub>	High-level input voltage		2		2		V
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	V
V <sub>I</sub>	Input voltage			5.5		5.5	V
I <sub>OH</sub>	High-level output current	A port	−12		−12		mA
		B port	−24		−32		
I <sub>OL</sub>	Low-level output current	A port	12		12		mA
		B port	48		64		
Δt/Δv	Input transition rise or fall rate	Outputs enabled	10		10		ns/V
Δt/ΔV <sub>CC</sub>	Power-up ramp rate		200		200		μs/V
T <sub>A</sub>	Operating free-air temperature		−55	125	−40	85	°C

(1) All unused or driven (floating) data inputs (I/Os) of the device must be held at logic HIGH or LOW (preferably  $V_{CC}$  or GND) to ensure proper device operation and minimize power. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

(2) Product preview

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVT162245A <sup>(1)</sup>		SN54LVT162245A		UNIT	
				MIN	TYP <sup>(2)</sup>	MAX	MIN		TYP <sup>(2)</sup>
V <sub>IK</sub>		V <sub>CC</sub> = 2.7 V, I <sub>I</sub> = −18 mA		−1.2		−1.2		V	
V <sub>OH</sub>	A port	V <sub>CC</sub> = 2.7 V to 3.6 V, I <sub>OH</sub> = −100 μA		V <sub>CC</sub> − 0.2		V <sub>CC</sub> − 0.2		V	
		V <sub>CC</sub> = 3 V, I <sub>OH</sub> = −12 mA		2		2			
	B port	V <sub>CC</sub> = 2.7 V to 3.6 V, I <sub>OH</sub> = −100 μA		V <sub>CC</sub> − 0.2		V <sub>CC</sub> − 0.2			
		V <sub>CC</sub> = 2.7 V, I <sub>OH</sub> = −8 mA		2.4		2.4			
		V <sub>CC</sub> = 3 V	I <sub>OH</sub> = −24 mA		2				
			I <sub>OH</sub> = −32 mA				2		
V <sub>OL</sub>	A port	V <sub>CC</sub> = 2.7 V to 3.6 V, I <sub>OL</sub> = 100 μA		0.2		0.2		V	
		V <sub>CC</sub> = 3 V, I <sub>OL</sub> = 12 mA		0.8		0.8			
	B port	V <sub>CC</sub> = 2.7 V	I <sub>OL</sub> = 100 μA		0.2		0.2		
			I <sub>OL</sub> = 24 mA		0.5		0.5		
		V <sub>CC</sub> = 3 V	I <sub>OL</sub> = 16 mA		0.4		0.4		
			I <sub>OL</sub> = 32 mA		0.5		0.5		
			I <sub>OL</sub> = 48 mA		0.55				
			I <sub>OL</sub> = 64 mA				0.55		
I <sub>I</sub>	Control inputs	V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = V <sub>CC</sub> or GND		±1		±1		μA	
		V <sub>CC</sub> = 0 or 3.6 V, V <sub>I</sub> = 5.5 V		10		10			
	A or B port <sup>(3)</sup>	V <sub>CC</sub> = 3.6 V	V <sub>I</sub> = 5.5 V		20		20		
			V <sub>I</sub> = V <sub>CC</sub>		5		5		
			V <sub>I</sub> = 0		−10		−10		
I <sub>off</sub>		V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5 V				±100		μA	
I <sub>OZPU</sub>		V <sub>CC</sub> = 0 to 1.5 V, V <sub>O</sub> = 0.5 V to 3 V, OE = don't care		±100 <sup>(4)</sup>		±100		μA	
I <sub>OZPD</sub>		V <sub>CC</sub> = 1.5 to 0 V, V <sub>O</sub> = 0.5 V to 3 V, OE = don't care		±100 <sup>(4)</sup>		±100		μA	
I <sub>CC</sub>		V <sub>CC</sub> = 3.6 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	Outputs high		0.19		0.19		mA
			Outputs low		5		5		
			Outputs disabled		0.19		0.19		
ΔI <sub>CC</sub> <sup>(5)</sup>		V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> − 0.6 V, Other inputs at V <sub>CC</sub> or GND		0.3		0.2		mA	
C <sub>i</sub>		V <sub>I</sub> = 3 V or 0		4		4		pF	
C <sub>io</sub>		V <sub>O</sub> = 3 V or 0		10		10		pF	

(1) Product preview

(2) All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

(3) Unused pins at  $V_{CC}\text{ or GND}$

(4) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(5) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}\text{ or GND}$ .

# SN54LVT162245A, SN74LVT162245A

## 3.3-V ABT 16-BIT BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

SCBS714D—FEBRUARY 2000—REVISED NOVEMBER 2006

## Switching Characteristics

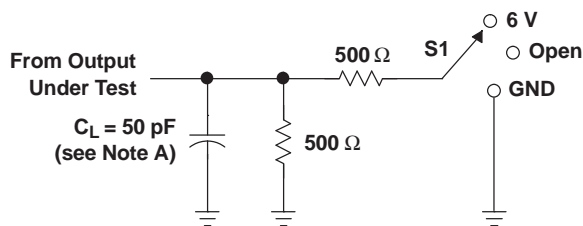
over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT162245A <sup>(1)</sup>				SN74LVT162245A				UNIT	
			V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V			V <sub>CC</sub> = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP <sup>(2)</sup>	MAX	MIN		MAX
t <sub>PLH</sub>	A	B	1	3.5		4	1	2.3	3.3		3.7	ns
t <sub>PHL</sub>			1	3.5		3.9	1	2.2	3.3		3.5	
t <sub>PLH</sub>	B	A	1	4.3		5.3	1	2.8	4		4.6	ns
t <sub>PHL</sub>			1	4.2		4.5	1	2.5	3.4		3.6	
t <sub>PZH</sub>	OE	B	1	4.8		5.9	1	2.8	4.6		5.4	ns
t <sub>PZL</sub>			1	4.8		5.5	1	3	4.6		5.2	
t <sub>PZH</sub>	OE	A	1	5.5		7.2	1	3.3	5.3		6.3	ns
t <sub>PZL</sub>			1	5.4		6.4	1	3.3	5.1		5.8	
t <sub>PHZ</sub>	OE	B	1.5	5.5		5.8	1.5	3.8	5.2		5.5	ns
t <sub>PLZ</sub>			1.5	5.5		5.8	1.5	3.5	5.1		5.4	
t <sub>PHZ</sub>	OE	A	1.5	5.8		6.5	1.5	4	5.6		5.9	ns
t <sub>PLZ</sub>			1.2	6.3		6.3	1.5	3.8	5.5		5.5	
t <sub>sk</sub> (LH)									0.5			ns
t <sub>sk</sub> (HL)									0.5			

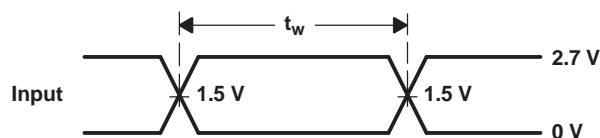
(1) Product preview

(2) All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

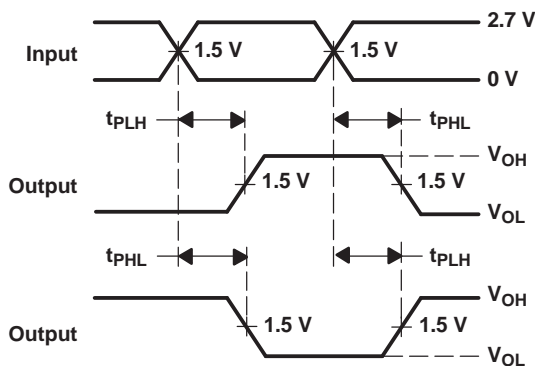
## PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

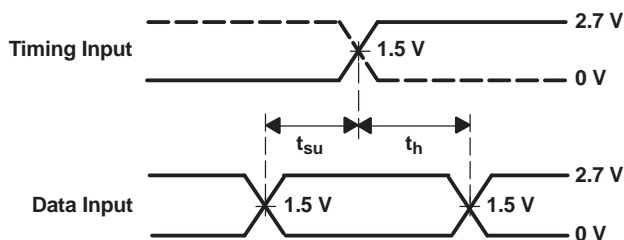


VOLTAGE WAVEFORMS  
PULSE DURATION

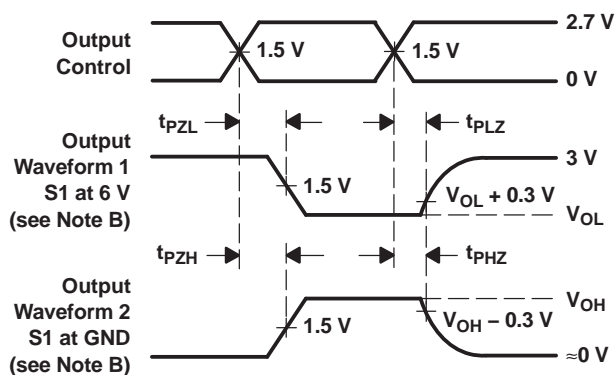


VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74LVT162245ADGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVT162245ADGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVT162245ADLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVT162245ADGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVT162245ADL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVT162245ADLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVT162245ADLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVT162245AGQLR	NRND	BGA MI CROSTAR JUNIOR	GQL	56	1000	TBD	SNPB	Level-1-240C-UNLIM
SN74LVT162245AGRDR	ACTIVE	BGA MI CROSTAR JUNIOR	GRD	54	1000	TBD	SNPB	Level-1-240C-UNLIM
SN74LVT162245AZQLR	ACTIVE	BGA MI CROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
SN74LVT162245AZRDR	ACTIVE	BGA MI CROSTAR JUNIOR	ZRD	54	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

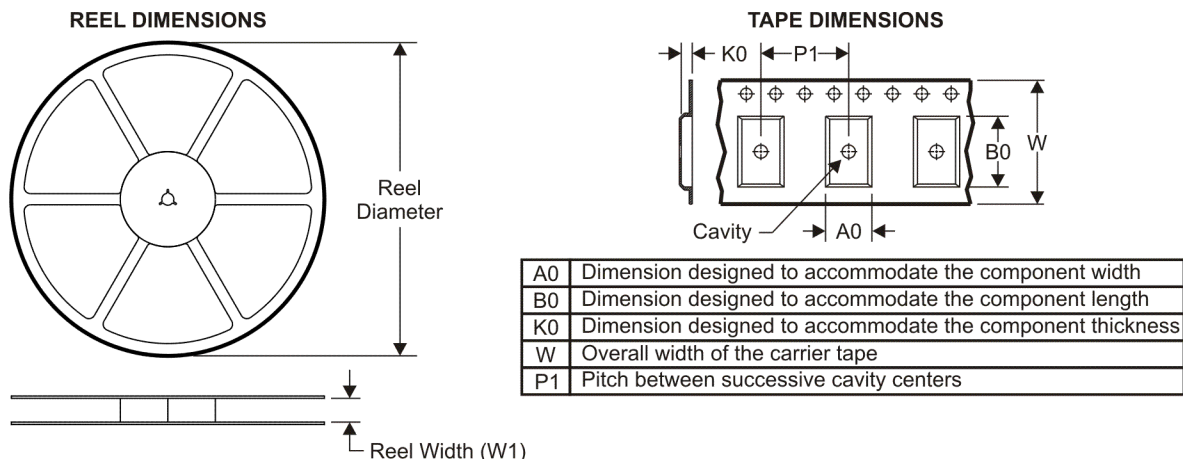
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

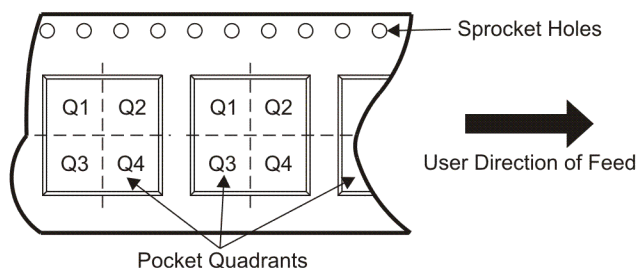
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**TAPE AND REEL INFORMATION**



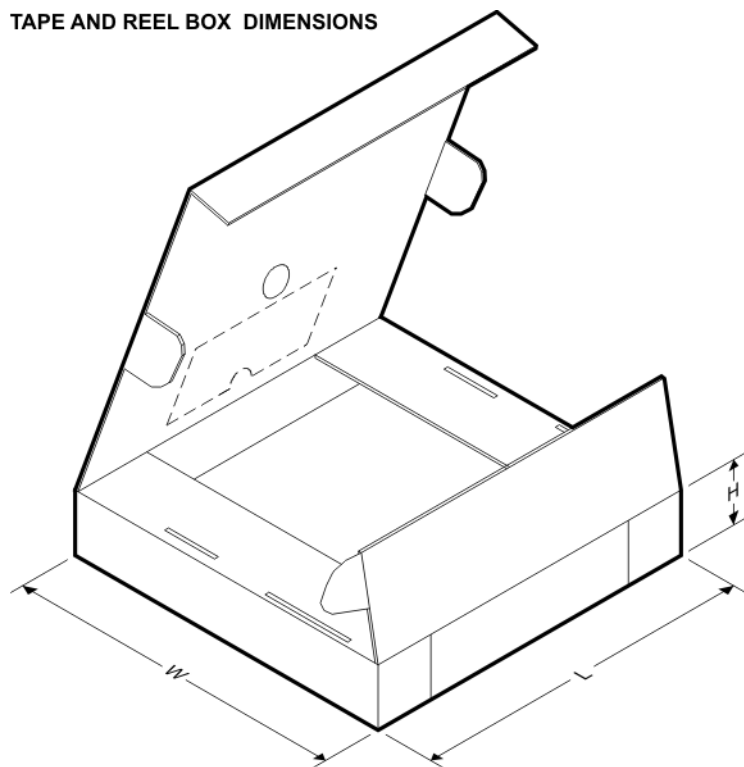
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVT162245ADGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74LVT162245ADLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
SN74LVT162245AGQLR	BGA MICROSTAR JUNIOR	GQL	56	1000	330.0	16.4	4.8	7.3	1.45	8.0	16.0	Q1
SN74LVT162245AGRDR	BGA MICROSTAR JUNIOR	GRD	54	1000	330.0	16.4	5.8	8.3	1.55	8.0	16.0	Q1
SN74LVT162245AZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	330.0	16.4	4.8	7.3	1.45	8.0	16.0	Q1
SN74LVT162245AZRDR	BGA MICROSTAR JUNIOR	ZRD	54	1000	330.0	16.4	5.8	8.3	1.55	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS

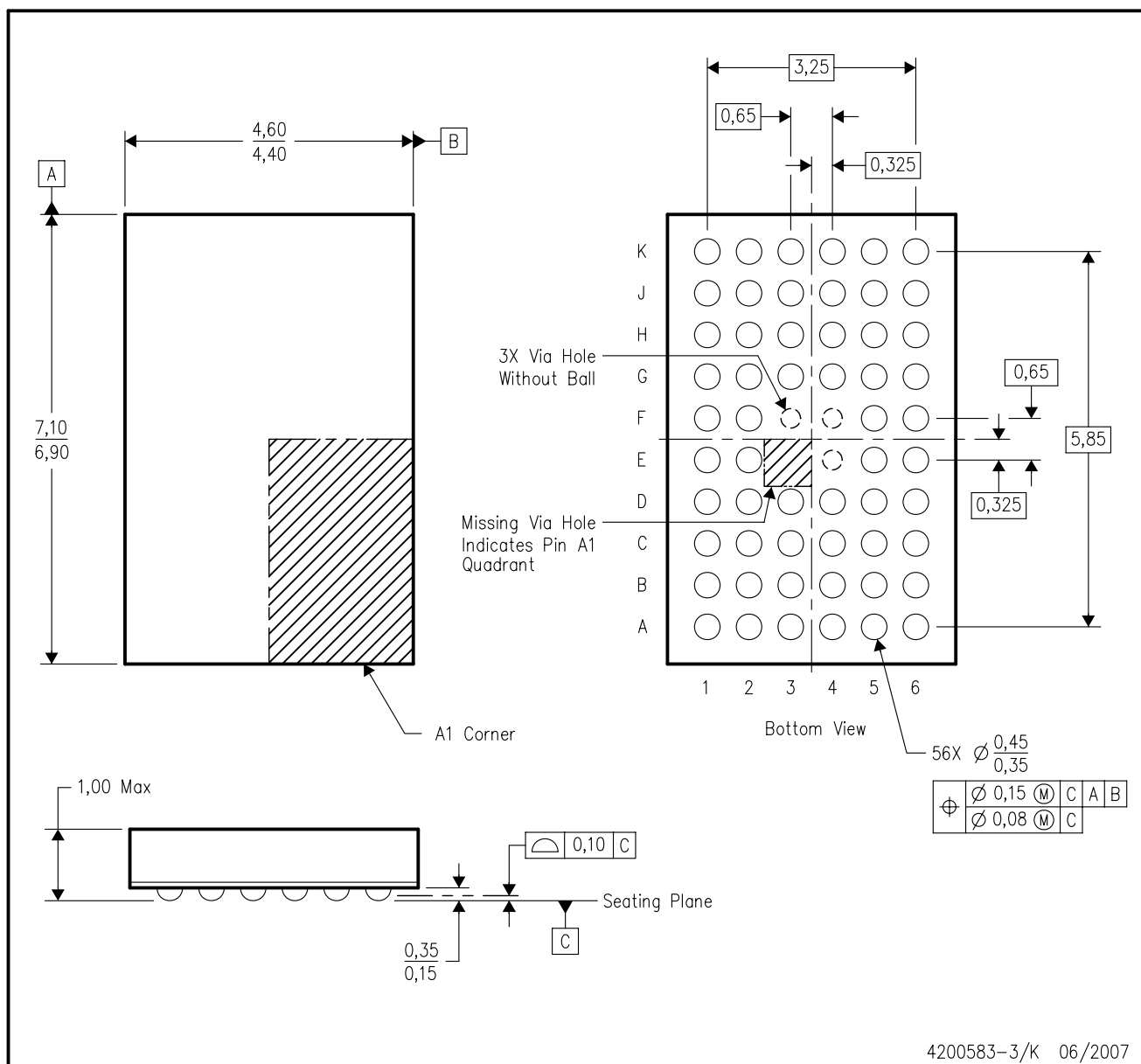


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVT162245ADGGR	TSSOP	DGG	48	2000	346.0	346.0	41.0
SN74LVT162245ADLR	SSOP	DL	48	1000	346.0	346.0	49.0
SN74LVT162245AGQLR	BGA MICROSTAR JUNIOR	GQL	56	1000	346.0	346.0	33.0
SN74LVT162245AGRDR	BGA MICROSTAR JUNIOR	GRD	54	1000	346.0	346.0	33.0
SN74LVT162245AZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	346.0	346.0	33.0
SN74LVT162245AZRDR	BGA MICROSTAR JUNIOR	ZRD	54	1000	346.0	346.0	33.0

## GQL (R-PBGA-N56)

## PLASTIC BALL GRID ARRAY

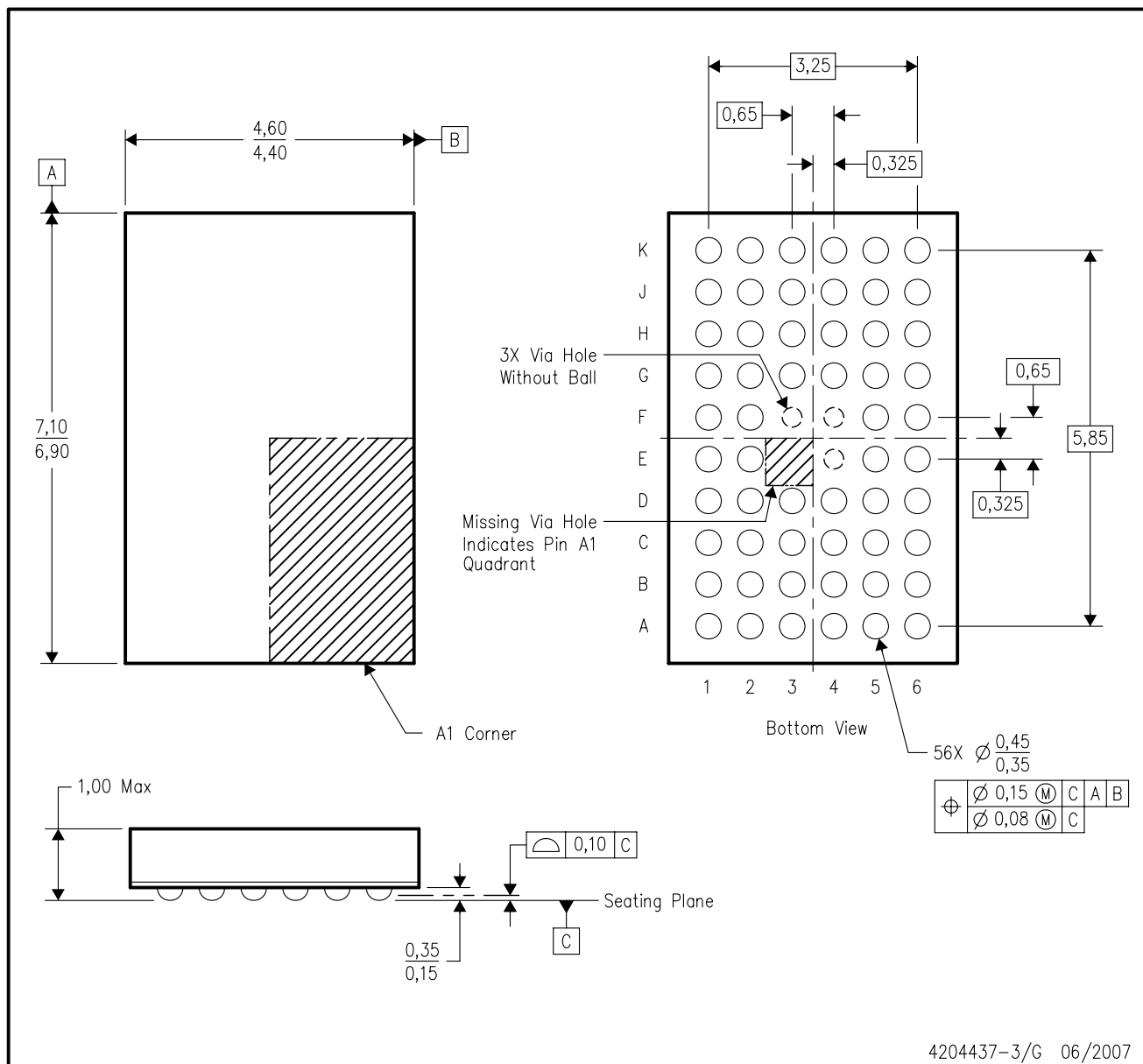


4200583-3/K 06/2007

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Falls within JEDEC MO-285 variation BA-2.
  - This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

## ZQL (R-PBGA-N56)

## PLASTIC BALL GRID ARRAY



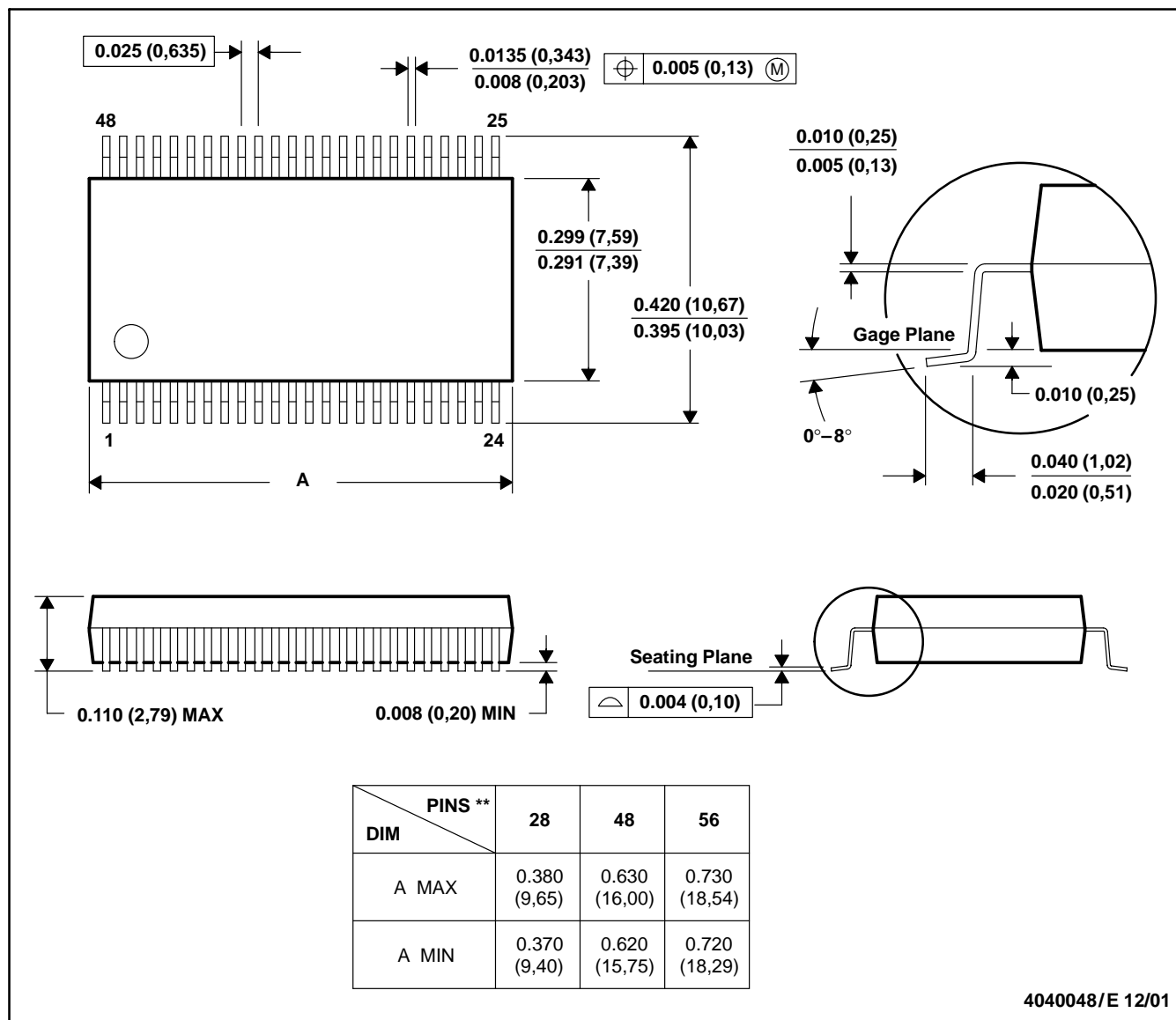
4204437-3/G 06/2007

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-285 variation BA-2.
  - D. This package is lead-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

DL (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

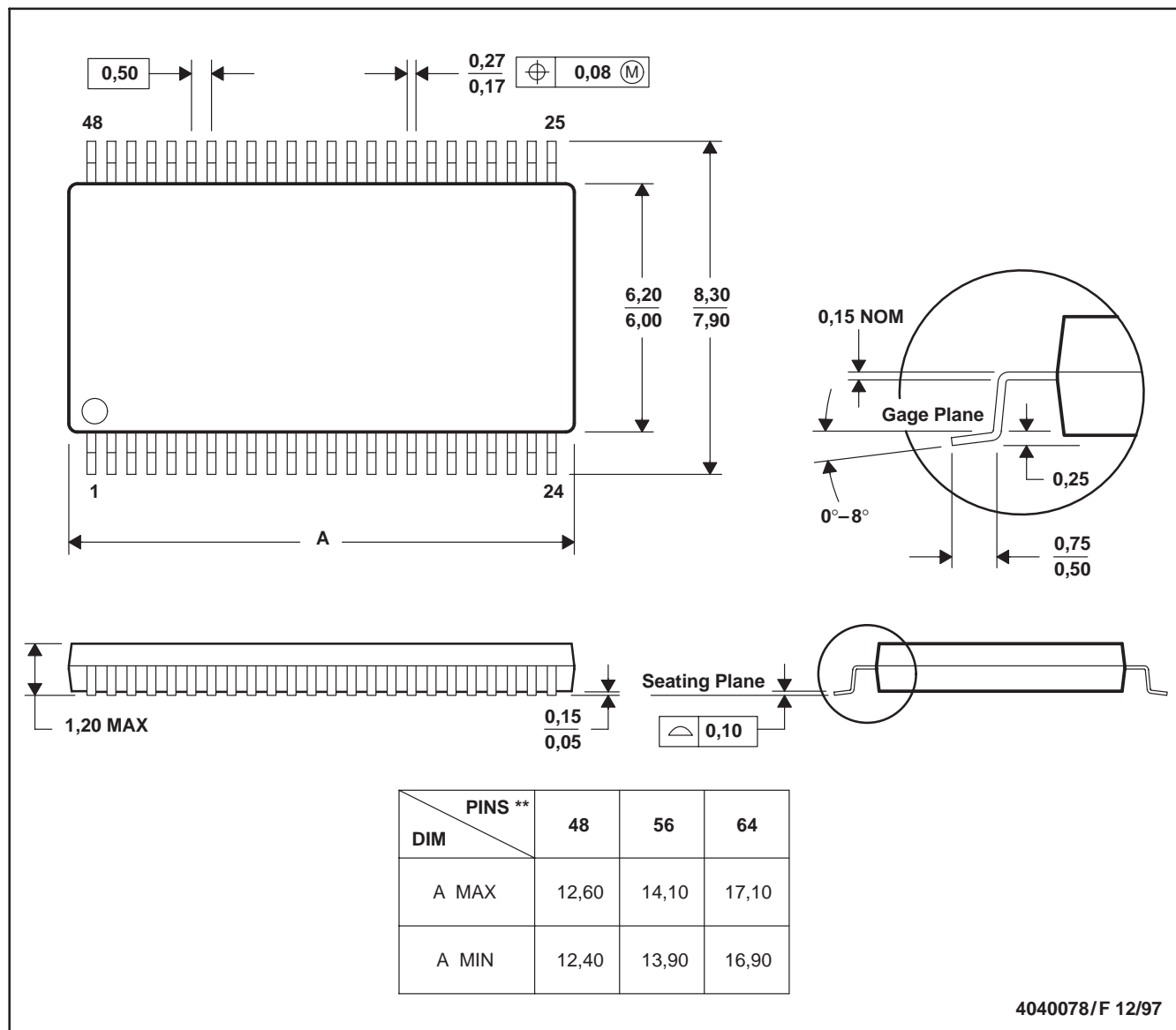


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118

## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

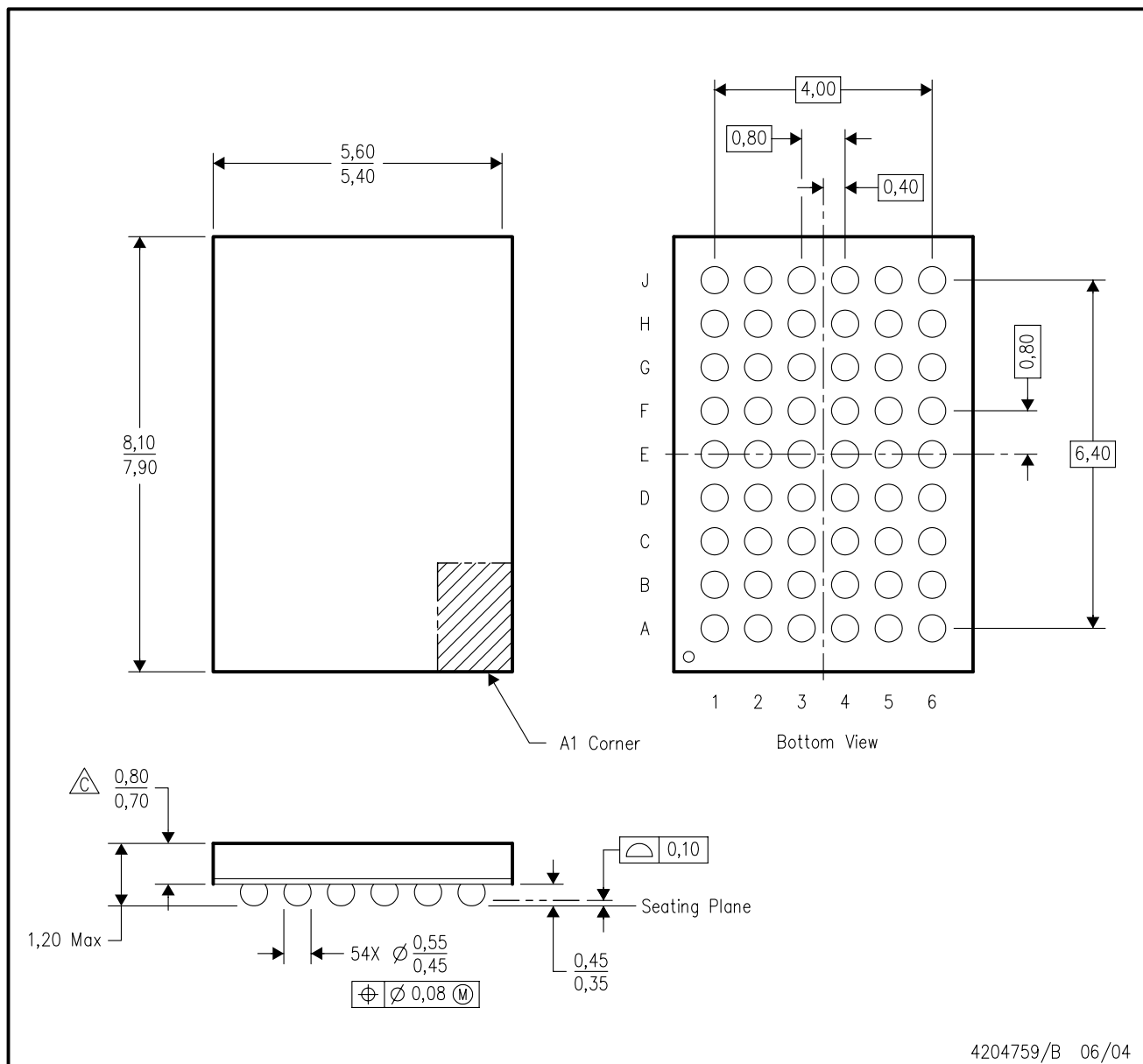
48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

## GRD (R-PBGA-N54)

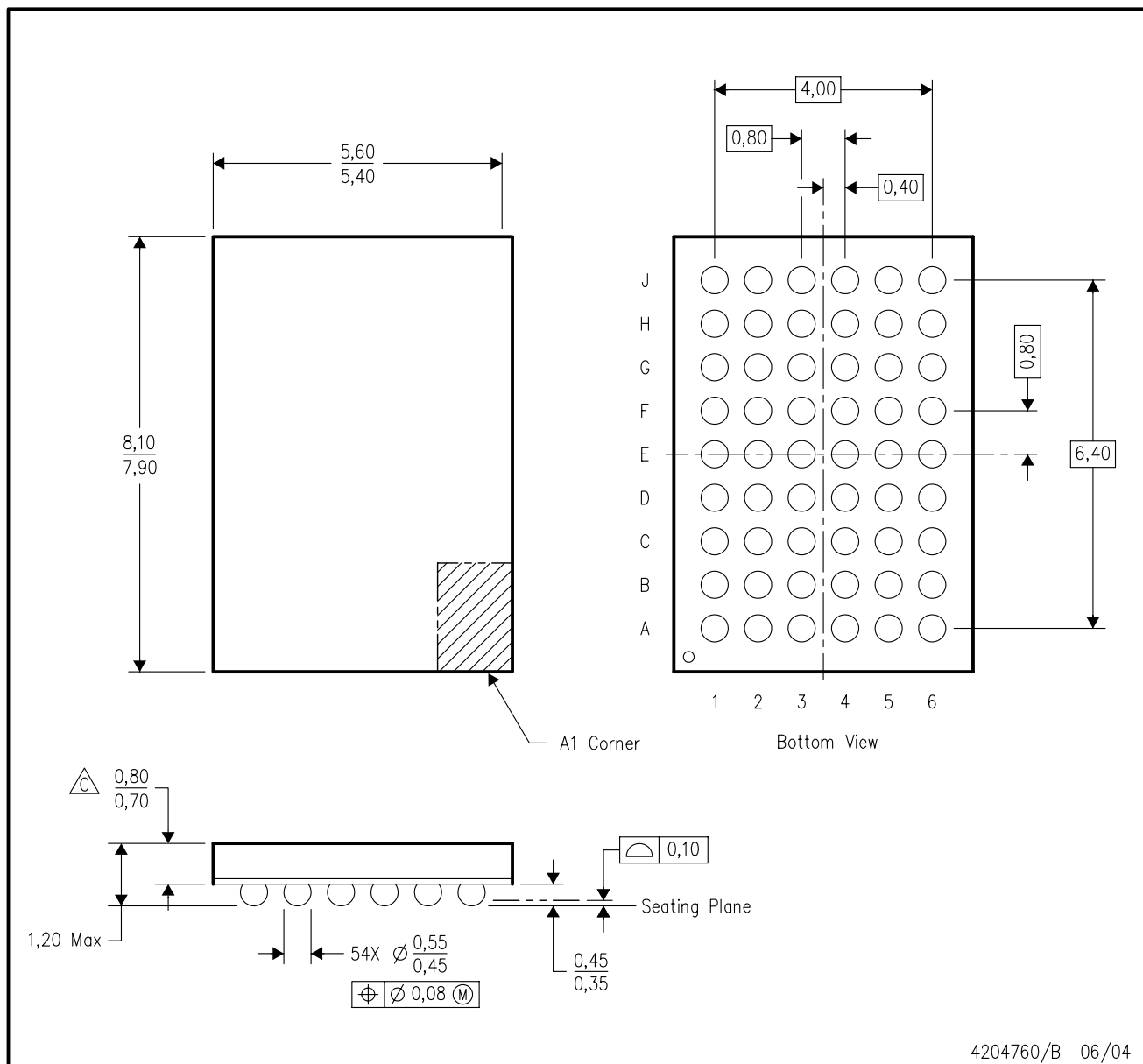
## PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-205 variation DD.
  - D. This package is tin-lead (SnPb). Refer to the 54 ZRD package (drawing 4204760) for lead-free.

ZRD (R-PBGA-N54)

## PLASTIC BALL GRID ARRAY



NOTES:

- A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
**C.** Falls within JEDEC MO-205 variation DD.  
D. This package is lead-free. Refer to the 54 GRD package (drawing 4204759) for tin-lead (SnPb).

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