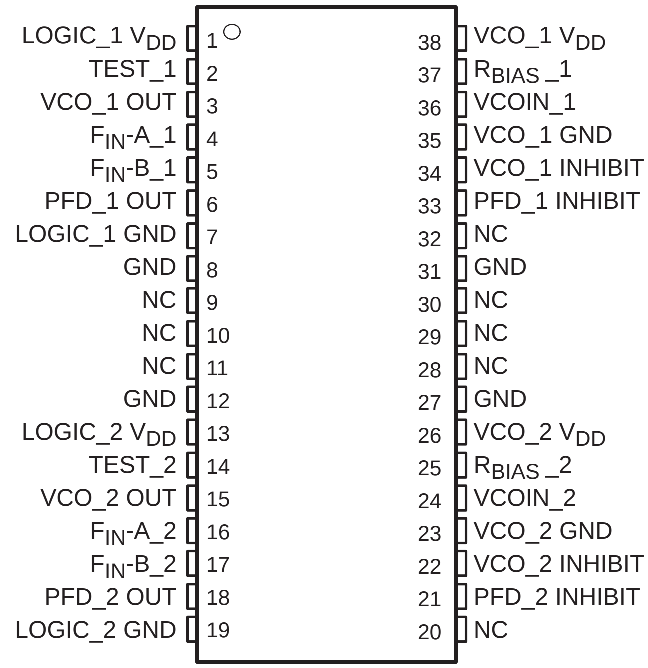
- **Dual TLC2933 by Multichip Module (MCM) Technology**
- **Voltage-Controlled Oscillators (VCO) Section**
  - **Complete Oscillator Using Only One External Bias Resistor (RBIAS)**
  - **Recommended Lock Frequency Range**
    - **37 MHz to 60 MHz (V_{DD} = 3.3 V ± 0.15 V, T_A = –20°C to 75°C)**
    - **43 MHz to 100 MHz (V_{DD} = 5 V ± 0.25 V, T_A = –20°C to 75°C)**
- **Includes a High Speed Edge-Triggered Phase Frequency Detector (PFD) With Internal Charge Pump**
- **Independent VCO, PFD Power-Down Mode**

DB PACKAGE (TOP VIEW)



description

The TLC2943 is a multichip module product that uses two TLC2933 chips. The TLC2933 chip is composed of a voltage-controlled oscillator (VCO) and an edge-triggered-type phase frequency detector (PFD). The oscillation frequency range of the VCO is set by an external bias resistor (R_{BIAS}). The high-speed PFD with internal charge pump detects the phase difference between the reference frequency input and signal frequency input from the external counter. Both the VCO and the PFD have inhibit functions that can be used as a power-down mode. The high-speed and stable VCO characteristics of the TLC2933 make the TLC2943 suitable for use in dual high-performance phase-locked loop (PLL) systems.

AVAILABLE OPTIONS

T_A	PACKAGE
	SMALL OUTLINE (DB)
–20°C to 75°C	TLC2943IDB
	TLC2943IDBR (Tape and Reel)

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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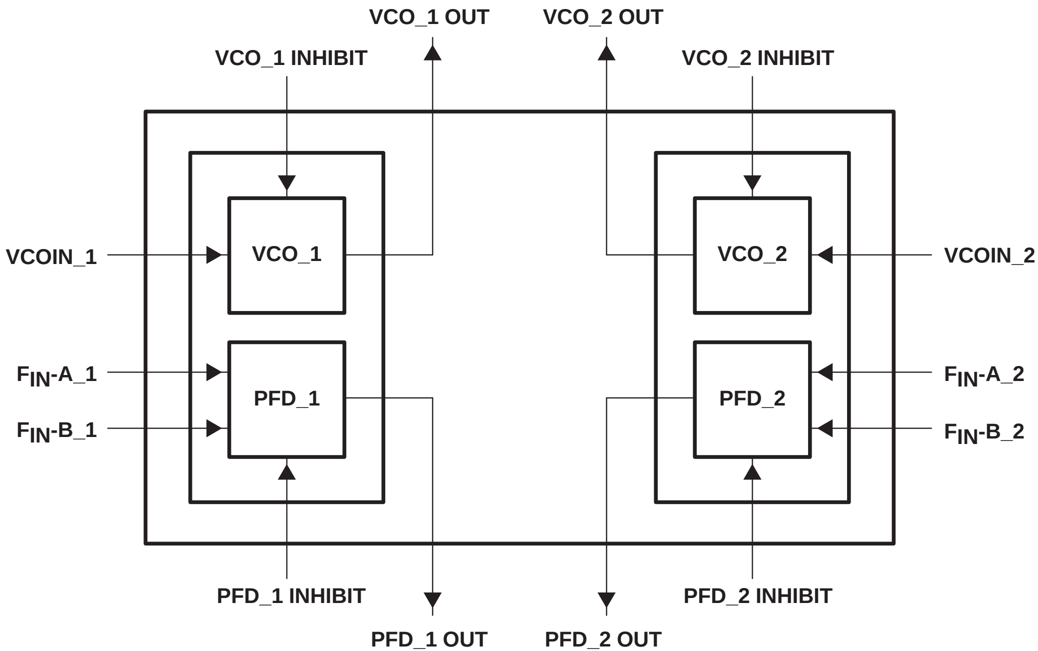
functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND	8, 31		Common GND for chip 1
	12, 27		Common GND for chip 2
F_{IN}–A_1, F_{IN}–B_1	4 5	I	Reference frequency signal input and comparison frequency signal input for PFD_1. fREF–IN_1 inputs to F_{IN}-A_1, and comparison frequency input from external counter logic to F_{IN}–B_1, for a lag-lead filter use as LPF.
F_{IN}–A_2, F_{IN}–B_2	16 17	I	Reference frequency signal input and comparison frequency signal input for PFD_2. fREF–IN_2 inputs to F_{IN}-A_2, and comparison frequency input from external counter logic to F_{IN}-B_2, for a lag-lead filter use as LPF.
LOGIC_1 GND	7		Ground for the internal logic of chip 1
LOGIC_2 GND	19		Ground for the internal logic of chip 2
LOGIC_1 V_{DD}	1		Power supply for the internal logic of chip 1. This power supply should be separate from VCO V_{DD} to reduce cross-coupling between supplies.
LOGIC_2 V_{DD}	13		Power supply for the internal logic of chip 2. This power supply should be separate from VCO V_{DD} to reduce cross-coupling between supplies.
NC	9, 10, 11, 20, 28, 29, 30, 32		No internal connection
PFD_1 INHIBIT	33	I	PFD inhibit control for chip 1. When PFD_1 INHIBIT is high, PFD_1 OUT is in the high-impedance state, see Table 2.
PFD_2 INHIBIT	21	I	PFD inhibit control for chip 2. When PFD_2 INHIBIT is high, PFD_2 OUT is in the high-impedance state, see Table 2.
PFD_1 OUT	6	O	PFD output of chip 1. When the PFD_1 INHIBIT is high, PFD_1 OUT is in the high-impedance state.
PFD_2 OUT	18	O	PFD output of chip 2. When the PFD_2 INHIBIT is high, PFD_2 OUT is in the high-impedance state.
R_{BIAS}_1	37	I	Bias supply for VCO_1. An external resistor (R_{BIAS}) between VCO_1 V_{DD} and BIAS_1 supplies bias for adjusting the oscillation frequency range of VCO_1.
R_{BIAS}_2	25	I	Bias supply for VCO_2. An external resistor (R_{BIAS}) between VCO_2 V_{DD} and BIAS_2 supplies bias for adjusting the oscillation frequency range of VCO_2.
TEST_1	2		Test terminal. TEST connects to LOGIC_1 GND for normal operation.
TEST_2	14		Test terminal. TEST connects to LOGIC_2 GND for normal operation.
VCO_1 GND	35		GND for VCO_1
VCO_2 GND	23		GND for VCO_2
VCO_1 INHIBIT	34	I	VCO inhibit control for chip 1. When VCO_1 INHIBIT is high, VCO_1 OUT is low (see Table 1).
VCO_2 INHIBIT	22	I	VCO inhibit control for chip 2. When VCO_2 INHIBIT is high, VCO_2 OUT is low (see Table 1).
VCO_1 OUT	3	O	VCO output of chip 1. When VCO_1 INHIBIT is high, VCO_1 OUT is low.
VCO_2 OUT	15	O	VCO output of chip 2. When VCO_2 INHIBIT is high, VCO_2 OUT is low.
VCO_1 V_{DD}	38		Power supply for VCO_1. This power supply should be separate from LOGIC V_{DD} to reduce cross-coupling between supplies.
VCO_2 V_{DD}	26		Power supply for VCO_2. This power supply should be separate from LOGIC V_{DD} to reduce cross-coupling between supplies.
VCOIN_1	36	I	VCO_1 control voltage input. Nominally the external loop filter output connects to VCO IN to control VCO oscillation frequency.
VCOIN_2	24	I	VCO_2 control voltage input. Nominally the external loop filter output connects to VCO IN to control VCO oscillation frequency.

detailed description

MCM (multichip module) technology for TLC2943

The TLC2943 is a multichip module (MCM) product that uses two TLC2933 chips. Inside the package, two chips are completely isolated by a special formed lead-frame. Therefore,when using the TLC2943 in two asynchronous PLL circuits, there is no performance degradation by electrical interference between chips inside the package. So, the same performance as TLC2933 can be easily expected by using TLC2943.

The NC terminals in the middle on both sides of the package are to achieve complete isolation inside the package. To get the best performance from this MCM technology, it is better to make a careful board layout of the external power supply, ground, and signal lines.

voltage controlled oscillator (VCO)

VCO_1 and VCO_2 have the same typical characteristics. Each VCO oscillation frequency is determined by an external resistor (R_{BIAS}) connected between the VCO V_{DD} and the BIAS terminals. The oscillation frequency and range depend on this resistor value. The bias resistor value for the minimum temperature coefficient is nominally 2.2 kΩ with V_{DD} = 3.3 V and nominally 2.4 kΩ with V_{DD} = 5 V. For the lock frequency range, refer to the recommended operating conditions. Figure 1 shows the typical frequency variation and VCO control voltage.

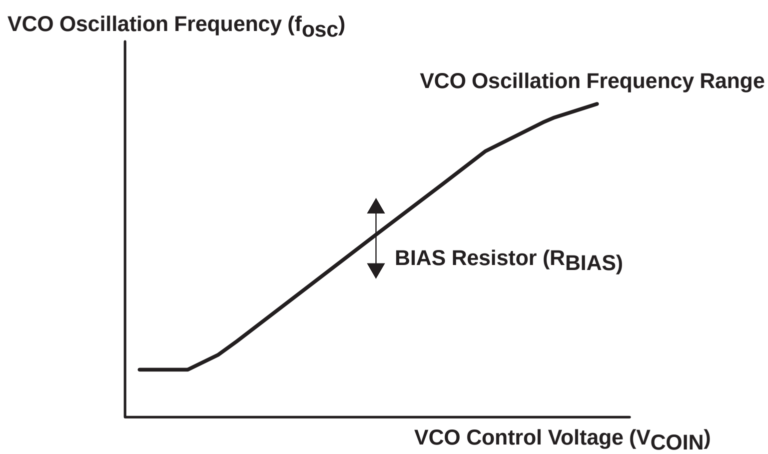


Figure 1. VCO_1 and VCO_2 Oscillation Frequency

VCO inhibit function

Each VCO has an externally controlled inhibit function that inhibits the VCO output. The VCO oscillation is stopped during a high level on VCOINHIBIT, so the high level can also be used as the power-down mode. The VCO output maintains a low level during the power-down mode (see Table 1 and Table 2).

Table 1. VCO_1 Inhibit Function

VCO_1 INHIBIT	VCO_1 OSCILLATOR	VCO_1 OUT	VCO_1 I_{DD}
Low	Active	Active	Normal
High	Stop	Low	Power down

Table 2. VCO_2 Inhibit Function

VCO_2 INHIBIT	VCO_2 OSCILLATOR	VCO_2 OUT	VCO_2 I_{DD}
Low	Active	Active	Normal
High	Stop	Low	Power down

detailed description (continued)

phase frequency detector (PFD)

The PFD is a high-speed, edge-triggered detector with an internal charge pump. The PFD detects the phase difference between two frequency inputs supplied to F_{IN}-A and F_{IN}-B as shown in Figure 2. Nominally the reference is supplied to F_{IN}-A, and the frequency from the external counter output is fed to F_{IN}-B. For clock recovery PLL systems, other types of phase detectors should be used.

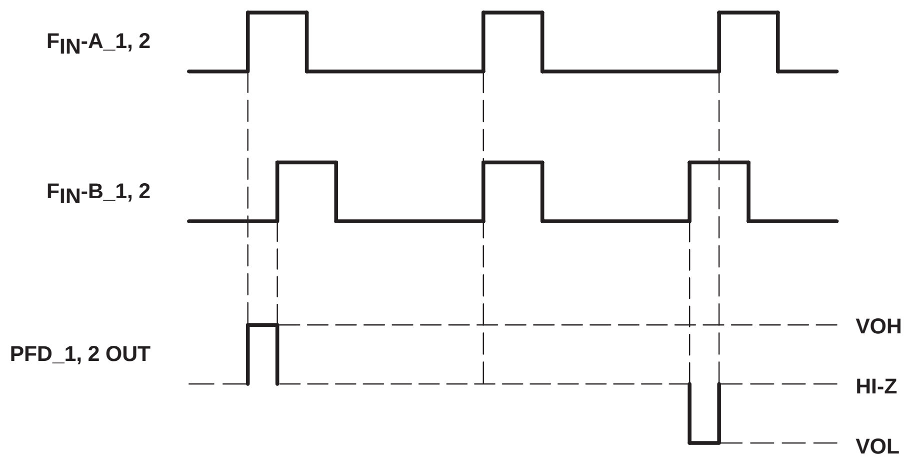


Figure 2. PFD Function Timing Chart

PFD output control

A high level on PFD INHIBIT places the PFD OUT in the high impedance state and the PFD stops phase detection as shown in Table 3 and Table 4. A high level on PFD inhibit also can be used as the power-down mode for the PFD.

Table 3. PFD_1 Inhibit Function

PFD_1 INHIBIT	PFD_1	PFD_1 OUT	PFD_1 I_{DD}
Low	Active	Active	Normal
High	Stop	Hi-Z	Power down

Table 4. PFD_2 Inhibit Function

PFD_2 INHIBIT	PFD_2	PFD_2 OUT	PFD_2 I_{DD}
Low	Active	Active	Normal
High	Stop	Hi-Z	Power down

internal function block diagram

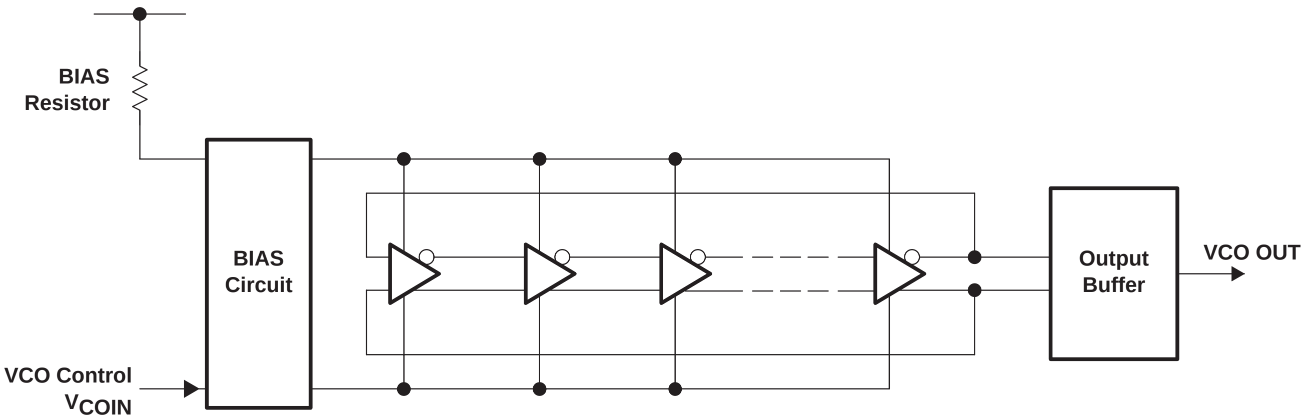


Figure 3. VCO Block Schematic (VCO_1, VCO_2)

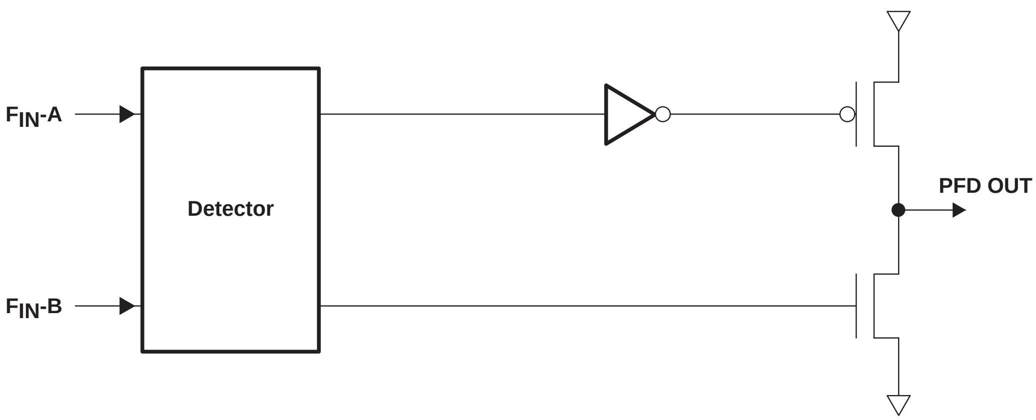


Figure 4. PFD Block Schematic (PFD_1, PFD_2)

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage (each supply), V_{DD} (see Note 1) .... 7 V
Input voltage range (each input), V_I (see Note 1) .... –0.5 to V_{DD} + 0.5 V
Input current (each input), I_I .... ±20 mA
Output current (each output), I_O .... ±20 mA
Continuous total power dissipation at (or below) T_A = 25°C (see Note 2) .... 1160 mW
Operating free-air temperature range, T_A .... –20°C to 75°C
Storage temperature range, T_{stg} .... –65°C to 150°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 9.3 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage (each supply, see Notes 3 and 4), V_{DD}	V_{DD} = 3 V	2.85	3	3.15	V
	V_{DD} = 3.3 V	3.15	3.3	3.45	
	V_{DD} = 5 V	4.75	5	5.25	
Input voltage range (input except for VCOIN_1, 2), V_I		0		V_{DD}	V
Output current (each output), I_O		0		±2	mA
Control voltage, VCOIN		1		V_{DD}	V
Clock frequency, f	V_{DD} = 3 V	37		55	MHz
	V_{DD} = 3.3 V	37		60	
	V_{DD} = 5 V	43		100	
Oscillation frequency range set resistor (each RBIAS), R_{BIAS} VCO	V_{DD} = 3 V	1.8		2.7	kΩ
	V_{DD} = 3.3 V	1.8		3.0	
	V_{DD} = 5 V	2.2		3.0	
Top operating temperature range		–20		75	°C

NOTES: 3. It is recommended that the logic supply terminal (LOGIC V_{DD}) and the VCO supply terminal (VCO V_{DD}) be at the same voltage and separated from each other.
4. Insert bypass capacitors locating the nearest point to each power supply terminal.

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 3 V (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.3	V
$V_{(TH+)}$	Positive input threshold voltage		0.9	1.5	2.1	V
I_I	Input current	$V_I = V_{DD}$ or GND			±1	µA
$Z_{(VCOIN)}$	VCOIN input impedance	VCOIN = 1/2V_{DD}		10		MΩ
$I_{DD(INH)}$	VCO supply current (inhibit) (for one chip)	See Note 5		0.01	1	µA
$I_{DD(VCO)}$	VCO supply current (for one chip)	See Note 6		5.1	15	mA

NOTES: 5. The current into VCO V_{DD} and LOGIC V_{DD} when VCO INHIBIT = V_{DD} and PFD INHIBIT is high.
6. The current into VCO V_{DD} and LOGIC V_{DD} when VCO IN = 1/2 V_{DD} , R_{BIAS} = 2.4 kΩ, VCO INHIBIT = ground, and PFD INHIBIT is high.

PFD section

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA	2.7			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.2	V
I_{OZ}	High-impedance state output current	PFD INHIBIT = high, $V_O = V_{DD}$ or GND			±1	µA
V_{IH}	High-level input voltage at F_{IN}–A, F_{IN}–B		2.1			V
V_{IL}	Low-level input voltage at F_{IN}–A, F_{IN}–B				0.9	V
$V_{(TH+)}$	Positive input threshold voltage at PFD INHIBIT		0.9	1.5	2.1	V
C_I	Input capacitance at F_{IN}–A, F_{IN}–B			5		pF
Z_I	Input impedance at F_{IN}–A, F_{IN}–B			10		MΩ
$I_{DD(PFD)}$	PFD supply current	See Note 7		0.7	4	mA

NOTE 7: The current into LOGIC V_{DD} when F_{IN}–A and F_{IN}–B = 30 MHz ($V_{I(PP)}$ = 3 V, rectangular wave), PFD INHIBIT = GND, PFD OUT open, and VCO OUT is inhibited.

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 3.3 V (unless otherwise noted) (continued)

VCO section

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA	2.7			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4	V
$V_{(TH+)}$	Positive input threshold voltage		1	1.65	2.3	V
I_I	Input current	V_I = V_{DD} or GND			±1	μA
$Z_{(VCOIN)}$	VCOIN input impedance	VCOIN = 1/2V_{DD}		10		MΩ
$I_{DD(INH)}$	VCO supply current (inhibit) (for one chip)	See Note 5		0.01	1	μA
$I_{DD(VCO)}$	VCO supply current (for one chip)	See Note 6		6.2	16	mA

NOTES: 5. The current into VCO V_{DD} and LOGIC V_{DD} when VCO INHIBIT = V_{DD} and PFD INHIBIT is high.
6. The current into VCO V_{DD} and LOGIC V_{DD} when VCO IN = 1/2 V_{DD} , R_{BIAS} = 2.4 kΩ, VCO INHIBIT = ground, and PFD INHIBIT is high.

PFD section

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA	3			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.2	V
I_{OZ}	High-impedance state output current	PFD INHIBIT = high, V_O = V_{DD} or GND			±1	μA
V_{IH}	High-level input voltage at F_{IN}–A, F_{IN}–B		2.3			V
V_{IL}	Low-level input voltage at F_{IN}–A, F_{IN}–B				1	V
$V_{(TH+)}$	Positive input threshold voltage at PFD INHIBIT		1	1.65	2.3	V
C_I	Input capacitance at F_{IN}–A, F_{IN}–B			5		pF
Z_I	Input impedance at F_{IN}–A, F_{IN}–B			10		MΩ
$I_{DD(PFD)}$	PFD supply current	See Note 8		0.8	5	mA

NOTE 8: The current into LOGIC V_{DD} when F_{IN}–A and F_{IN}–B = 30 MHz (V I(PP) = 3.3 V, rectangular wave), PFD INHIBIT = GND, PFD OUT open, and VCO OUT is inhibited.

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 5 V (unless otherwise noted) (continued)

VCO section

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA	4.5			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.5	V
$V_{(TH+)}$	Positive input threshold voltage		1.5	2.5	3.5	V
I_I	Input current	V_I = V_{DD} or GND			±1	µA
$Z_{(VCOIN)}$	VCOIN input impedance	VCOIN = 1/2V_{DD}		10		MΩ
$I_{DD(INH)}$	VCO supply current (inhibit) (for one chip)	See Note 5		0.01	1	µA
$I_{DD(VCO)}$	VCO supply current (for one chip)	See Note 6		14	35	mA

NOTES: 5. The current into VCO V_{DD} and LOGIC V_{DD} when VCO INHIBIT = V_{DD} and PFD INHIBIT is high.
6. The current into VCO V_{DD} and LOGIC V_{DD} when VCO IN = 1/2 V_{DD} , R_{BIAS} = 2.4 kΩ, VCO INHIBIT = ground, and PFD INHIBIT is high.

PFD section

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA	4.5			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.2	V
I_{OZ}	High-impedance state output current	PFD INHIBIT = high, V_O = V_{DD} or GND			±1	µA
V_{IH}	High-level input voltage at F_{IN}–A, F_{IN}–B		3.5			V
V_{IL}	Low-level input voltage at F_{IN}–A, F_{IN}–B				1.5	V
$V_{(TH+)}$	Positive input threshold voltage at PFD INHIBIT		1.5	2.5	3.5	V
C_I	Input capacitance at F_{IN}–A, F_{IN}–B			7		pF
Z_I	Input impedance at F_{IN}–A, F_{IN}–B			10		MΩ
$I_{DD(PFD)}$	PFD supply current	See Note 9		2.6	8	mA

NOTE 9: The current into LOGIC V_{DD} when F_{IN}–A and F_{IN}–B = 50 MHz (V I(PP) = 5 V, rectangular wave), PFD INHIBIT = GND, PFD OUT open, and VCO OUT is inhibited.

operating characteristics at V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$f_{(OSC)}$	Oscillation frequency	R_{BIAS} = 2.4 kΩ,	VCOIN = 1/2V_{DD}	38	48	58	MHz
$t_{(STB)}$	Time to stable oscillation	See Note 10				10	µs
t_r	Output rise time	C_L = 15 pF,	See Figure 5		3.3	10	ns
t_f	Output fall time	C_L = 15 pF,	See Figure 5		2	8	ns
$f_{(DUTY)}$	Duty cycle	R_{BIAS} = 2.4 kΩ,	VCOIN = 1/2V_{DD}	45%	50%	55%	
$f_{(TA)}$	Temperature coefficient of oscillation frequency	R_{BIAS} = 2.4 kΩ, Top = –20°C to 75°C	VCOIN = 1/2V_{DD}		0.03		%/°C
$f_{(VDD)}$	Supply voltage coefficient of oscillation frequency supply	R_{BIAS} = 2.4 kΩ, V_{DD} = 2.85 V to 3.15 V	VCOIN = 1.5 V,		0.04		%/mV

NOTE 10: The time period to the stable VCO oscillation frequency after the VCO INHIBIT terminal is changed to a low level.

PFD section

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
f_{MAX}	Maximum operating frequency			30			MHz
t_{PLZ}	PFD output disable time from low level	See Figure 6 and Figure 7, and Table 5			20	40	ns
t_{PHZ}	PFD output disable time from high level				18	40	
t_{PZL}	PFD output enable time to low level				4.1	18	ns
t_{PZH}	PFD output enable time to high level				4.8	18	
t_r	Rise time	C_L = 15 pF,	See Figure 6		3.1	9	ns
t_f	Fall time				1.5	9	

operating characteristics at V_{DD} = 3.3 V, T_A = 25°C (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$f_{(OSC)}$	Oscillation frequency	R_{BIAS} = 2.4 kΩ,	VCOIN = 1/2V_{DD}	42	52	62	MHz
$t_{(STB)}$	Time to stable oscillation	See Note 10				10	µs
t_r	Output rise time	C_L = 15 pF,	See Figure 5		3	8	ns
t_f	Output fall time	C_L = 15 pF,	See Figure 5		1.9	7	ns
$f_{(DUTY)}$	Duty cycle	R_{BIAS} = 2.4 kΩ,	VCOIN = 1/2V_{DD}	45%	50%	55%	
$f_{(TA)}$	Temperature coefficient of oscillation frequency	R_{BIAS} = 2.4 kΩ, Top = –20°C to 75°C	VCOIN = 1/2V_{DD}		0.03		%/°C
$f_{(VDD)}$	Supply voltage coefficient of oscillation frequency supply	R_{BIAS} = 2.4 kΩ, V_{DD} = 3.15 V to 3.45 V	VCOIN = 1.65 V,		0.04		%/mV

NOTE 10: The time period to the stable VCO oscillation frequency after the VCO INHIBIT terminal is changed to a low level.

PFD section

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
f_{MAX}	Maximum operating frequency			30			MHz
t_{PLZ}	PFD output disable time from low level	See Figure 6 and Figure 7, and Table 5			20	40	ns
t_{PHZ}	PFD output disable time from high level				18	40	
t_{PZL}	PFD output enable time to low level					16	ns
t_{PZH}	PFD output enable time to high level					16	
t_r	Rise time	C_L = 15 pF,	See Figure 6			8	ns
t_f	Fall time					8	

operating characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$f_{(OSC)}$	Oscillation frequency	R_{BIAS} = 2.4 kΩ,	VCOIN = 1/2V_{DD}	64	80	96	MHz
$t_{(STB)}$	Time to stable oscillation	See Note 10				10	µs
t_r	Output rise time	C_L = 15 pF,	See Figure 5		2.1	5	ns
t_f	Output fall time	C_L = 15 pF,	See Figure 5		1.5	4	ns
$f_{(DUTY)}$	Duty cycle	R_{BIAS} = 2.4 kΩ,	VCOIN = 1/2V_{DD}	45%	50%	55%	
$f_{(TA)}$	Temperature coefficient of oscillation frequency	R_{BIAS} = 2.4 kΩ, Top = –20°C to 75°C	VCOIN = 1/2V_{DD}		0.03		%/°C
$f_{(VDD)}$	Supply voltage coefficient of oscillation frequency supply	R_{BIAS} = 2.4 kΩ, V_{DD} = 4.75 V to 5.25 V	VCOIN = 2.5 V,		0.02		%/mV

PFD section

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
f_{MAX}	Maximum operating frequency			50			MHz
t_{PLZ}	PFD output disable time from low level	See Figure 6 and Figure 7, and Table 5			20	40	ns
t_{PHZ}	PFD output disable time from high level				17	40	
t_{PZL}	PFD output enable time to low level				3.7	10	ns
t_{PZH}	PFD output enable time to high level				3.5	10	
t_r	Rise time	C_L = 15 pF,	See Figure 6		1.7	5	ns
t_f	Fall time				1.3	5	

PARAMETER MEASUREMENT INFORMATION

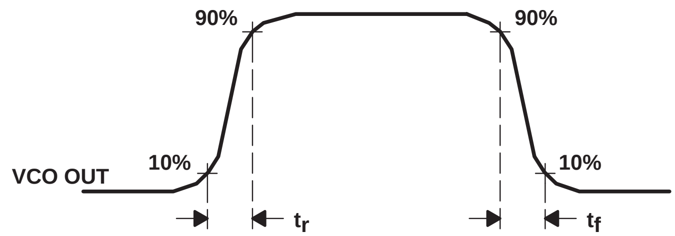


Figure 5. VCO Output Voltage Waveform (Each VCO)

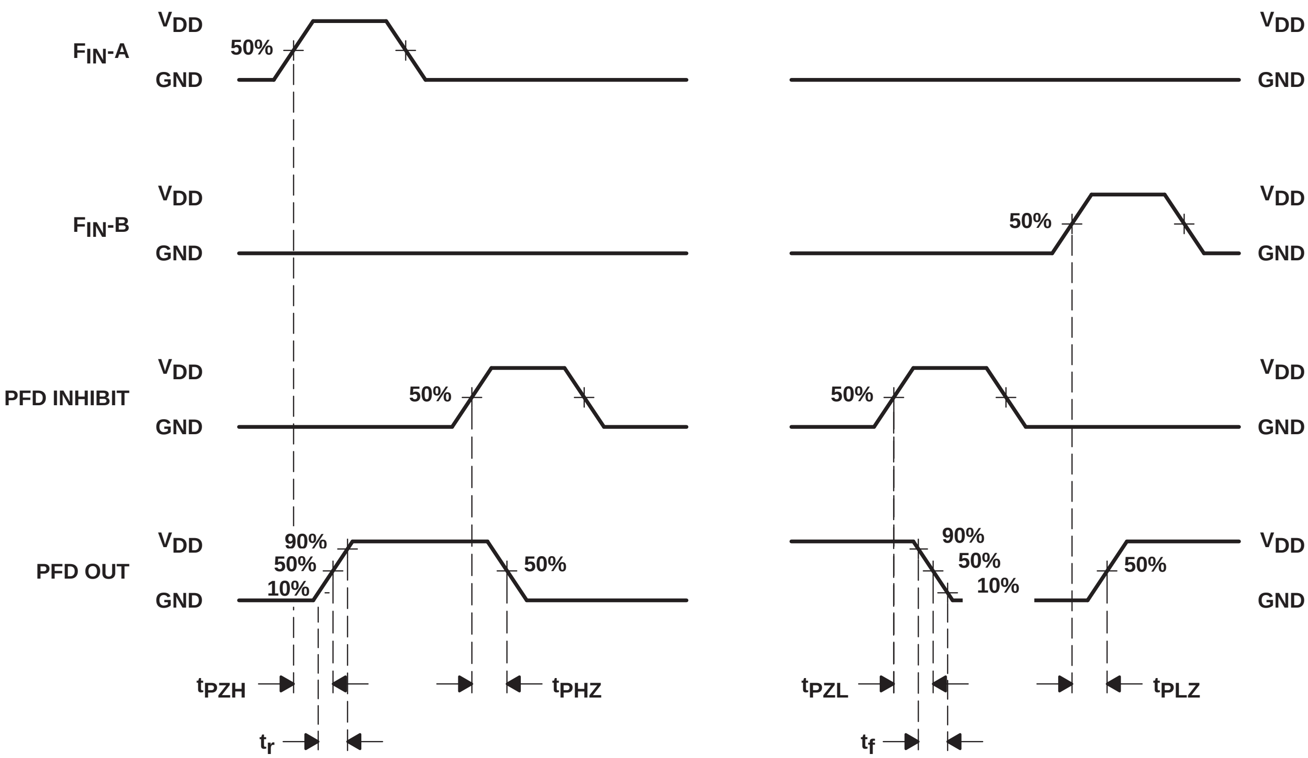


Figure 6. PFD Output Voltage Waveform

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PARAMETER MEASUREMENT INFORMATION

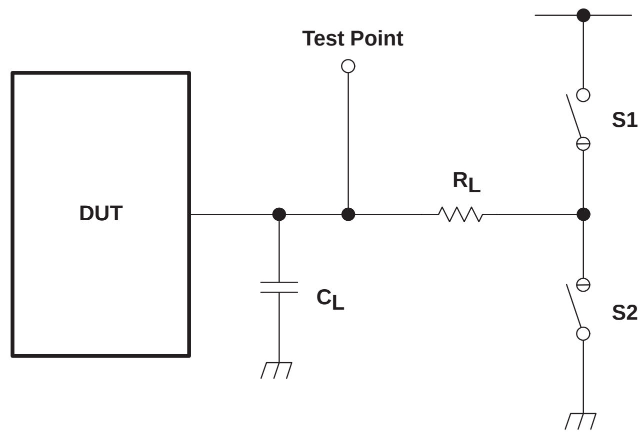


Figure 7. PFD Output Test Conditions

Table 5. PFD Output Test Conditions

PARAMETER	R_L	C_L	S1	S2
t_{PZH}	1 kΩ	15 pF	OPEN	CLOSE
t_{PHZ}				
t_r				
t_{PZL}			CLOSE	OPEN
t_{PLZ}				
t_f				

TYPICAL CHARACTERISTICS

OSCILLATION FREQUENCY
vs
CONTROL VOLTAGE

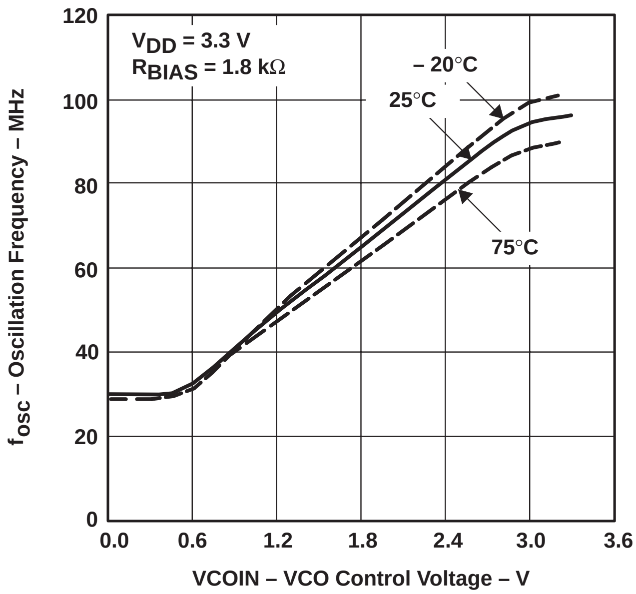


Figure 8

OSCILLATION FREQUENCY
vs
CONTROL VOLTAGE

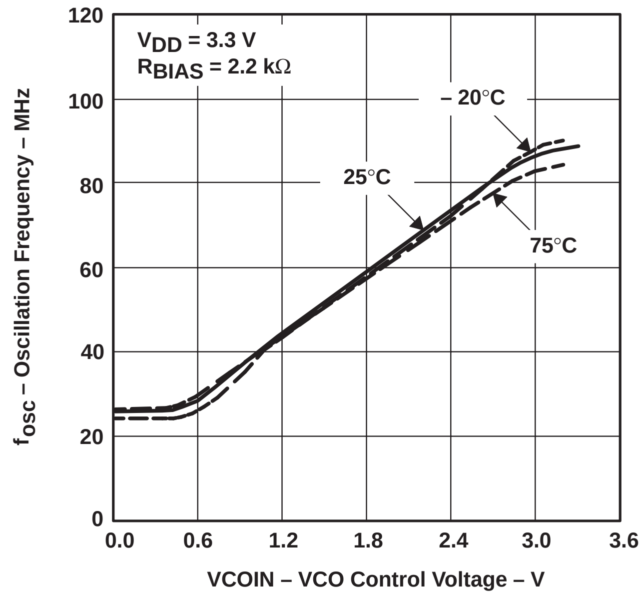


Figure 9

OSCILLATION FREQUENCY
vs
CONTROL VOLTAGE

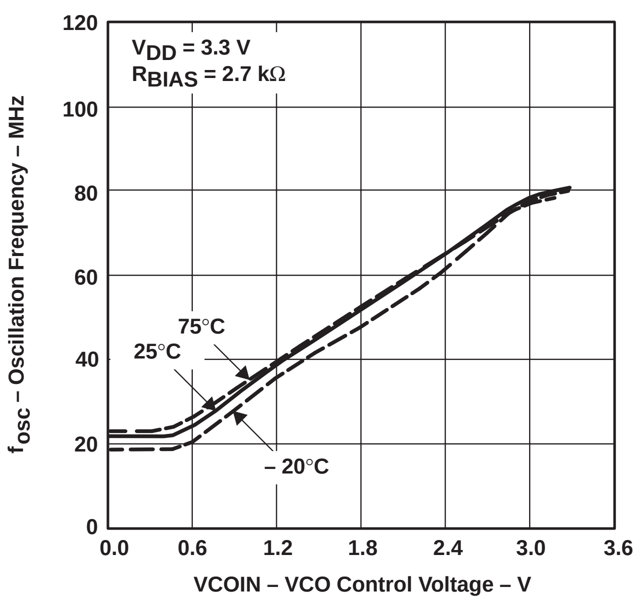


Figure 10

OSCILLATION FREQUENCY
vs
CONTROL VOLTAGE

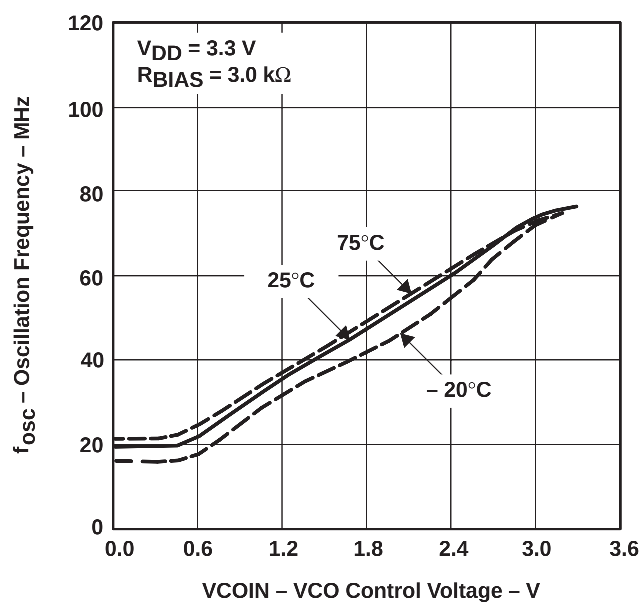


Figure 11

TYPICAL CHARACTERISTICS

OSCILLATION FREQUENCY
vs
CONTROL VOLTAGE

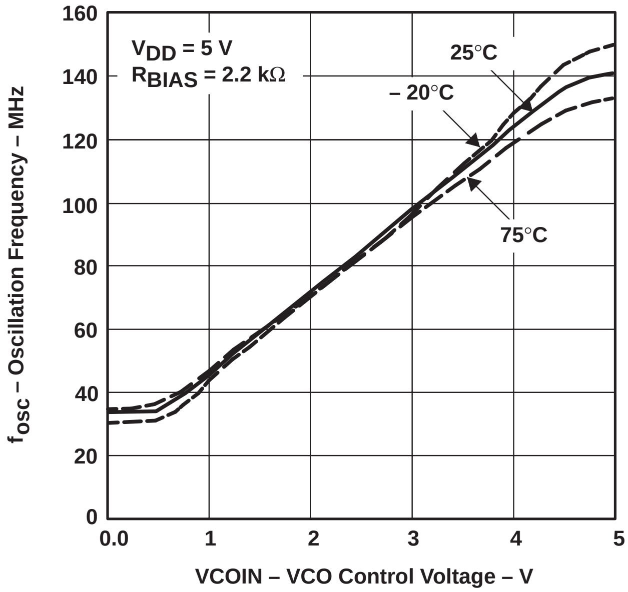


Figure 12

OSCILLATION FREQUENCY
vs
CONTROL VOLTAGE

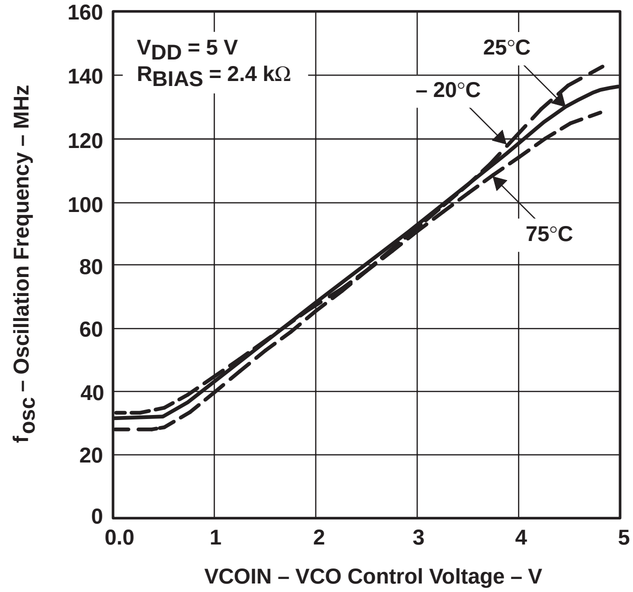


Figure 13

OSCILLATION FREQUENCY
vs
CONTROL VOLTAGE

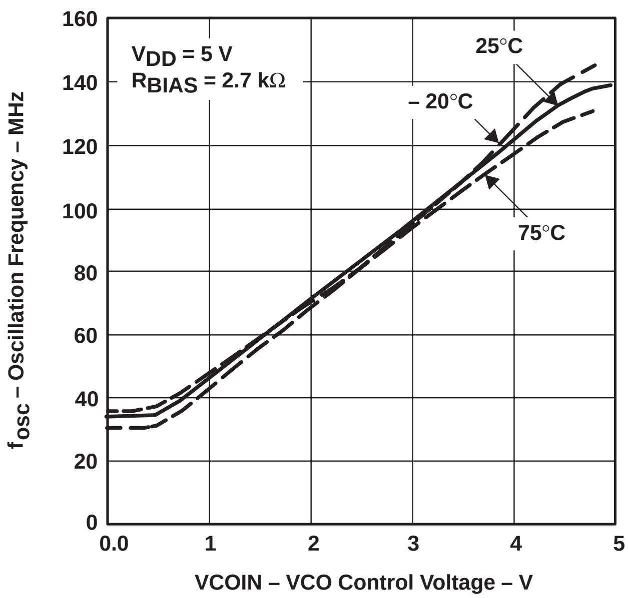


Figure 14

OSCILLATION FREQUENCY
vs
CONTROL VOLTAGE

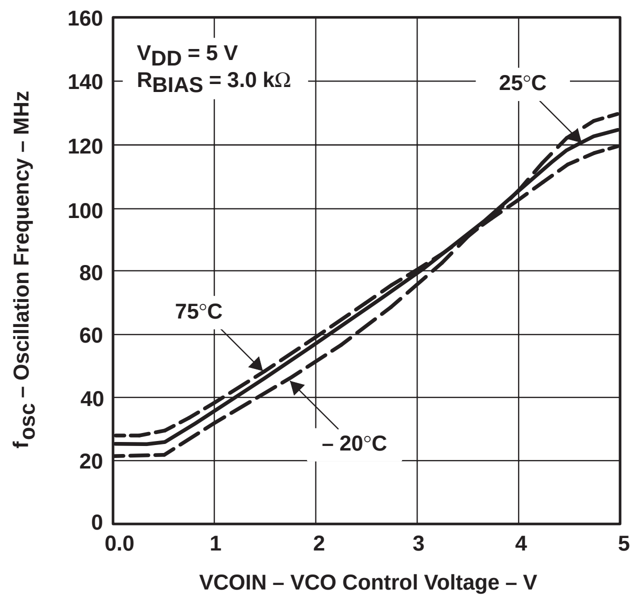


Figure 15

TYPICAL CHARACTERISTICS

LOCK FREQUENCY RANGE
vs
BIAS RESISTANCE

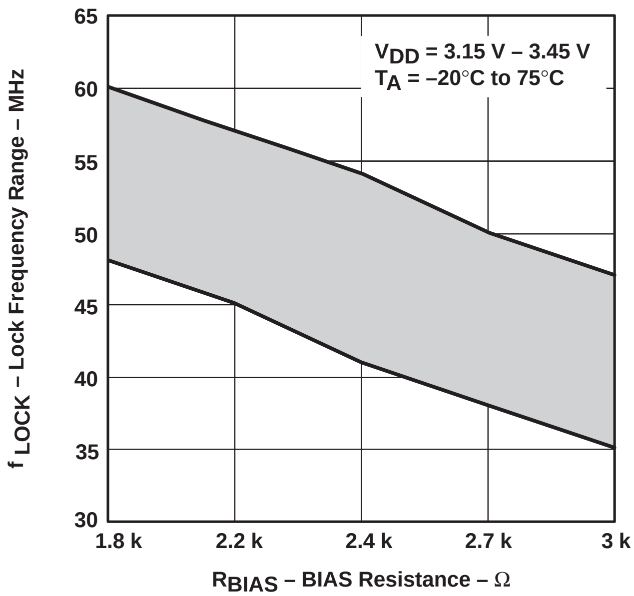


Figure 16

LOCK FREQUENCY RANGE
vs
BIAS RESISTANCE

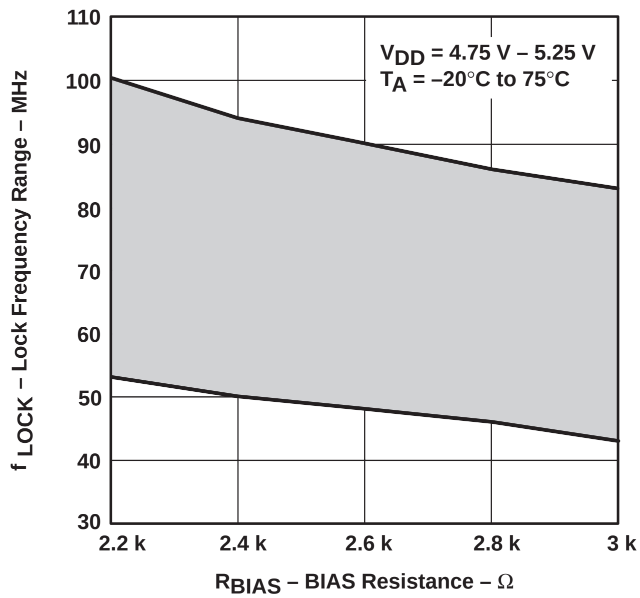


Figure 17

APPLICATION INFORMATION

gain of VCO and PFD

Figure 18 is a block diagram of the PLL. The divider N value depends on the input frequency and the desired VCO output frequency according to the system application requirements. The K_p and K_V values are obtained from the operating characteristics of the device as shown in Figure 18. K_p is defined from the phase detector V_{OL} and V_{OH} specifications and the equation shown in Figure 18(b). K_V is defined from Figures 8, 9, 10, and 11 as shown in Figure 18(c).

The parameters for the block diagram with the units are as follows:

K_V : VCO gain (rad/s/V)
K_p : PFD gain (V/rad)
K_f : LPF gain (V/V)
K_N : countdown divider gain (1/N)

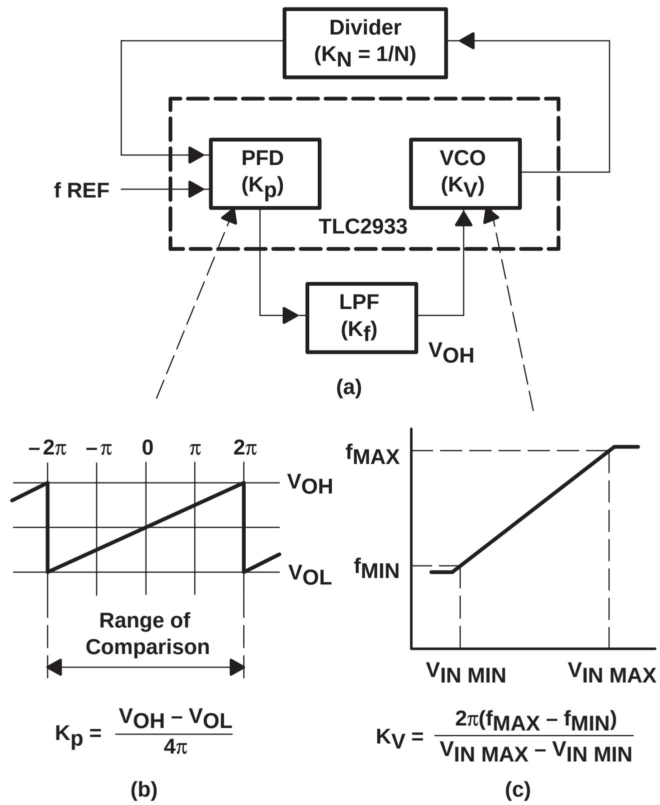


Figure 18. Example of a PLL Block Diagram

external counter

When a large N counter is required by the application, there is a possibility that the PLL response becomes slow due to the counter response delay time. In the case of a high frequency application, the counter delay time should be accounted for in the overall PLL design.

R_{BIAS}

The external bias resistor sets the VCO center frequency with 1/2 V_{DD} applied to the VCO IN terminal. For the most accurate results, a metal-film resistor is the better choice, but a carbon-composition resistor can also be used with excellent results. A 0.22 µF capacitor should be connected from the BIAS terminal to ground as close to the device terminals as possible.

hold-in range

From the technical literature, the maximum hold-in range for an input frequency step for the three types of filter configurations shown in Figure 17 is as follows:

$$\Delta\omega_H \simeq 0.8 \left(K_p\right)\left(K_V\right)\left(K_f\ (\infty)\right) \quad (1)$$

Where

K_f (∞) = the filter transfer function value at ω = ∞

APPLICATION INFORMATION

low-pass-filter (LPF) configurations

References that include detailed design information about LPFs should be consulted for additional information. Lag-lead filters or active filters are often used. Examples of LPFs are shown in Figure 19. When the active filter of Figure 19(c) is used, the reference should be applied to F_{IN}-B because of the amplifier inversion. Also, in practical filter implementations, C2 is used as additional filtering at the VCO input. The value of C2 should be equal to or less than one tenth the value of C1.

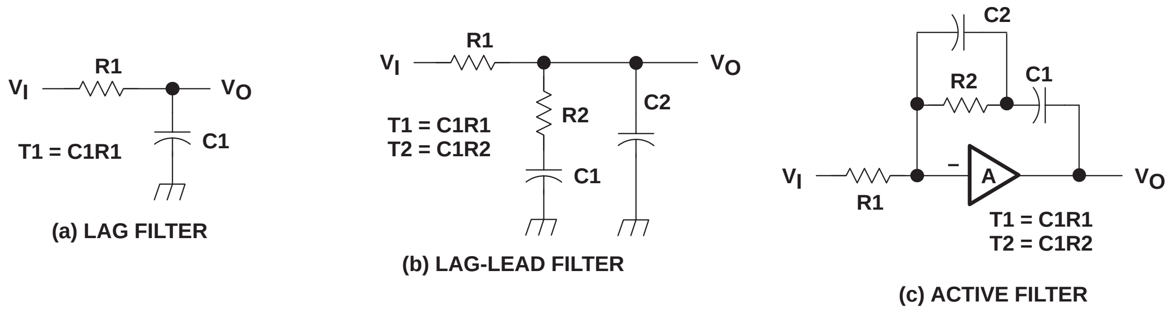


Figure 19. LPF Examples for PLL

passive filter

The transfer function for the low-pass filter shown in Figure 17(b) is;

$$\frac{V_O}{V_{IN}} = \frac{1 + s \times T2}{1 + s \times (T1 + T2)} \tag{2}$$

Where

$$T1 = R1 \times C1 \text{ and } T2 = R2 \times C1$$

Using this filter makes the closed-loop PLL system a type 1 second-order system. The response curves of this system to a unit step are shown in Figure 20.

active filter

When using the active filter shown in Figure 19(c), the phase detector inputs must be reversed, since the filter adds an additional inversion. Therefore, the input reference frequency should be applied to the F_{IN}-B terminal and the output of the VCO divider should be applied to the input reference terminal, F_{IN}-A.

The transfer function for the active filter shown in Figure 19(c) is:

$$F(s) = \frac{1 + s \times R2 \times C1}{s \times R1 \times C1} \tag{3}$$

Using this filter makes the closed-loop PLL system a type 2 second-order system. The response curves of this system to a unit step are shown in Figure 21.

APPLICATION INFORMATION

Using the lag-lead filter in Figure 19(b) and divider N value, the transfer function for phase and frequency are shown in equations 4 and 5. Note that the transfer function for phase differs from the transfer function for frequency by only the divider N value. The difference arises from the fact that the feedback for phase is unity, while the feedback for frequency is 1/N.

Hence, the transfer function of Figure 19(a) for phase is

$$\frac{\Phi 2(s)}{\Phi 1(s)} = \frac{K_p \times K_V}{N \times (T1 + T2)} \left[\frac{1 + s \times T2}{s^2 + s \left[1 + \frac{K_p \times K_V \times T2}{N \times (T1 + T2)} \right] + \frac{K_p \times K_V}{N \times (T1 + T2)}} \right] \tag{4}$$

and the transfer function for frequency is

$$\frac{F_{OUT(s)}}{F_{REF(s)}} = \frac{K_p \times K_V}{(T1 + T2)} \left[\frac{1 + s \times T2}{s^2 + s \times \left[1 + \frac{K_p \times K_V \times T2}{N \times (T1 + T2)} \right] + \frac{K_p \times K_V}{N \times (T1 + T2)}} \right] \tag{5}$$

The standard 2-pole denominator is $D = s^2 + 2\,\zeta\,\omega_n\,s + \omega_n{}^2$ and comparing the coefficients of the denominator of equation (4) and (5) with the standard 2-pole denominator gives the following results.

$$\omega_n = \sqrt{\frac{K_p \times K_V}{N \times (T1 + T2)}} \tag{6}$$

Solving for T1 + T2

$$T1 + T2 = \frac{K_p \times K_V}{N \times \omega_n{}^2}$$

and by using this value for T1 + T2 in equation (6) the damping factor is

$$\zeta = \frac{\omega_n}{2} \times \left(T2 + \frac{N}{K_p \times K_V} \right) \tag{7}$$

solving for T2

$$T2 = \frac{2\,\zeta}{\omega} - \frac{N}{K_p \times K_V} \tag{8}$$

then by substituting for T2 in equation (6)

$$T1 = \frac{K_V \times K_p}{N \times \omega_n{}^2} - \frac{2\,\zeta}{\omega_n} + \frac{N}{K_p \times K_V} \tag{9}$$

APPLICATION INFORMATION

From the circuit constants and the initial design parameters then

$$R2 = \left[\frac{2\,\zeta}{\omega_n} - \frac{N}{K_p \times K_V}\right]\frac{1}{C1} \tag{10}$$

$$R1 = \left[\frac{K_p \times K_V}{{\omega_n}^2 \times N} - \frac{2\,\zeta}{\omega_n} + \frac{N}{K_p \times K_V}\right]\frac{1}{C1} \tag{11}$$

The capacitor, C1, is usually chosen between 1 µF and 0.1 µF to allow for reasonable resistor values and physical capacitor size.

APPLICATION INFORMATION

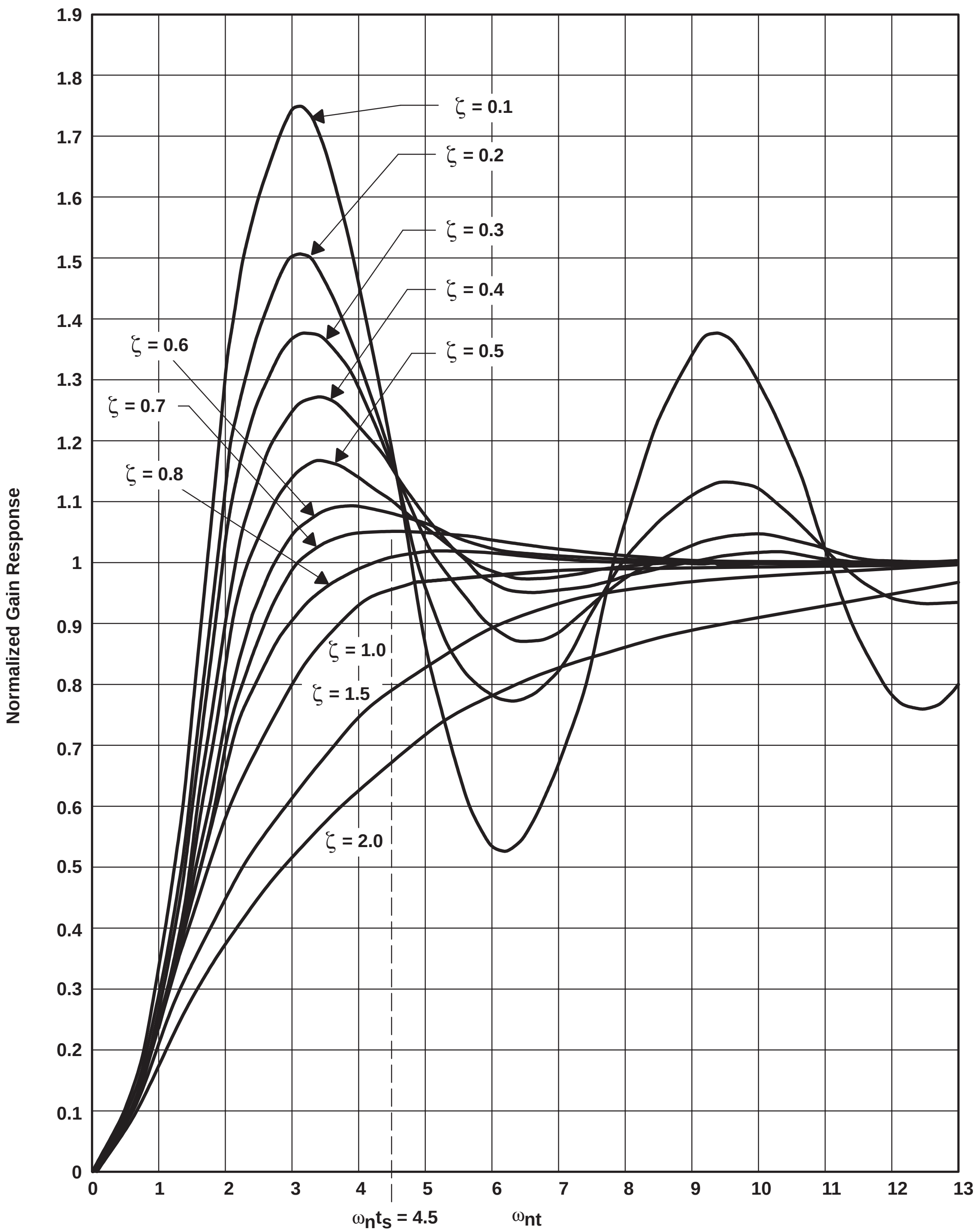


Figure 20. Type 1 Second-Order Step Response

APPLICATION INFORMATION

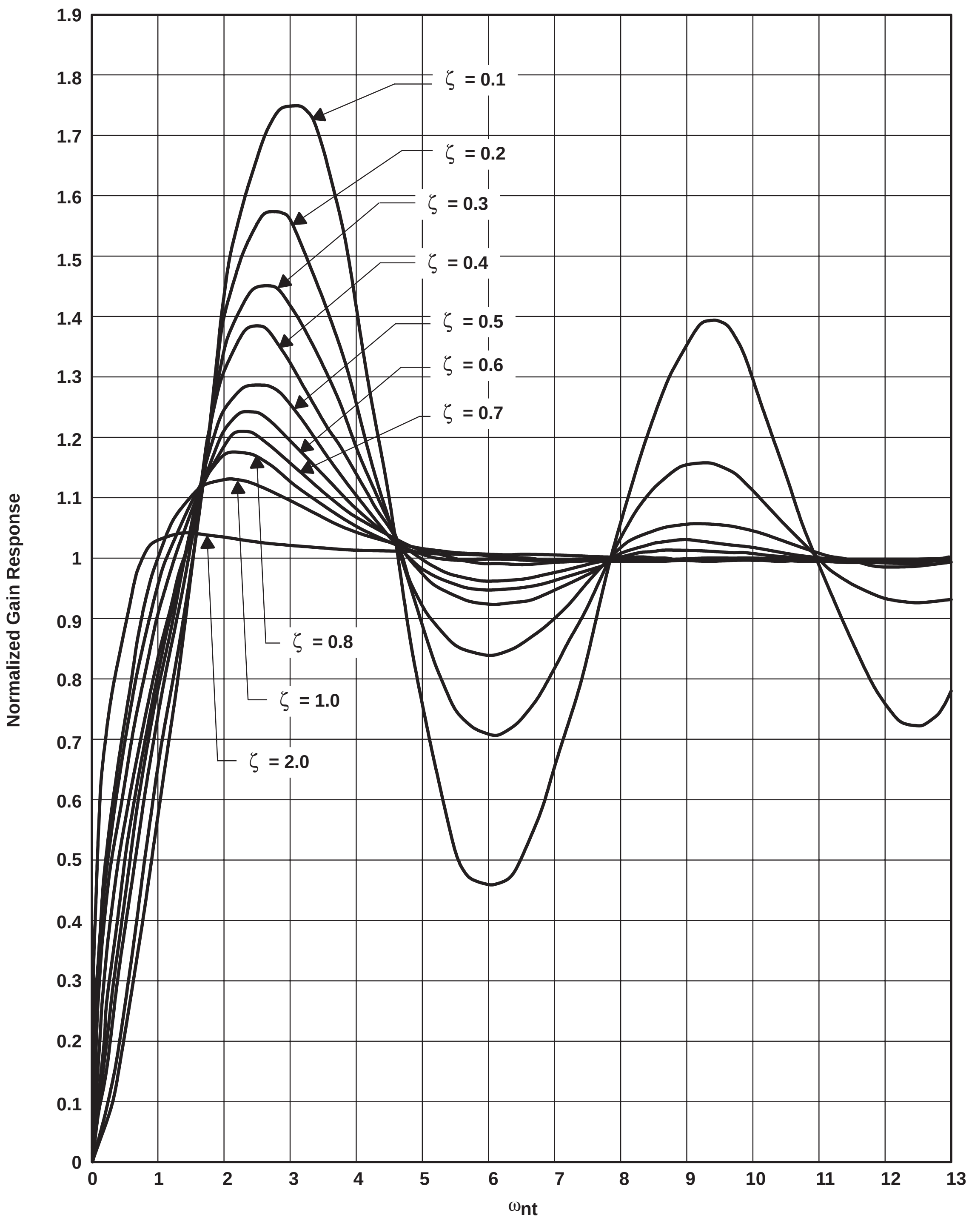


Figure 21. Type 2 Second-Order Step Response

APPLICATION INFORMATION

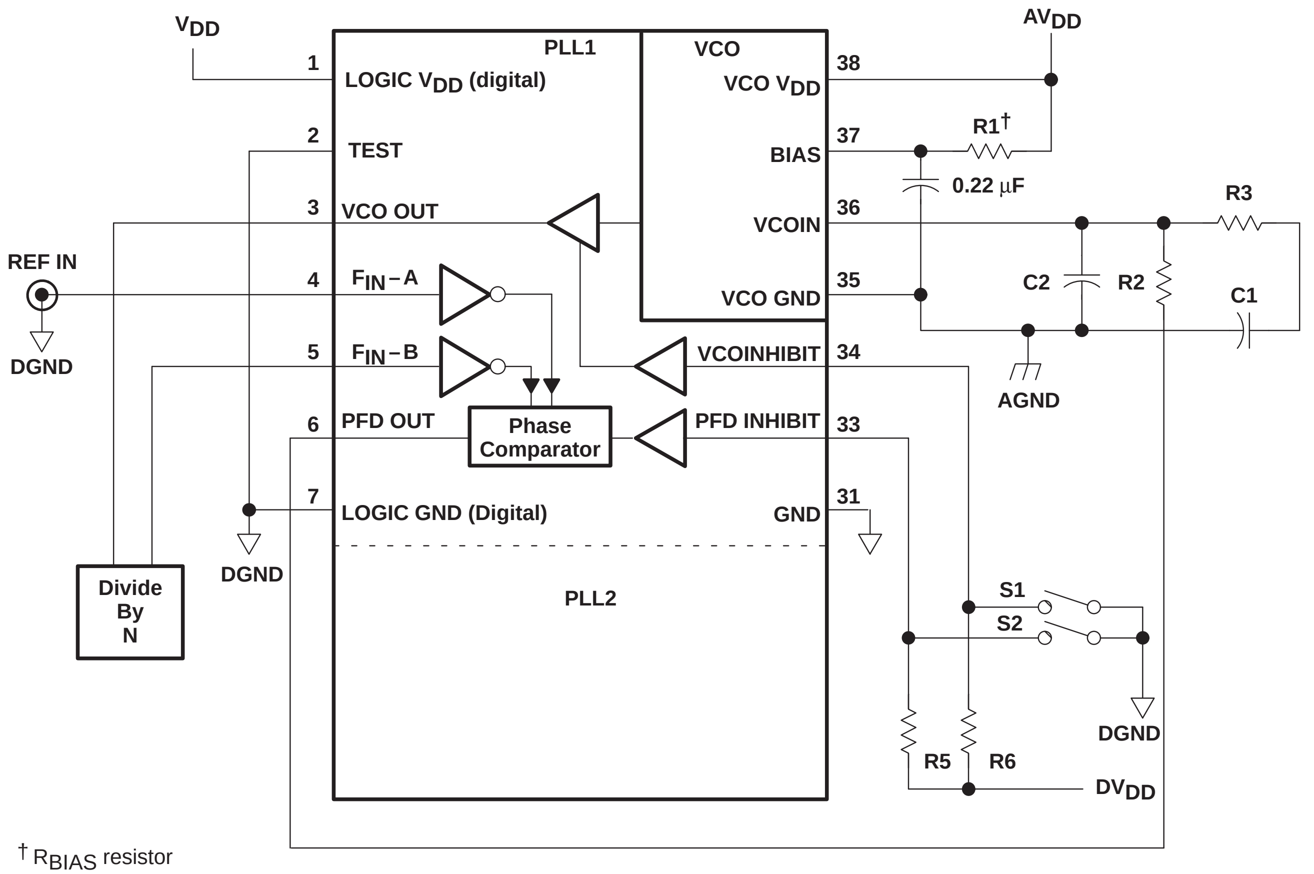
PCB layout considerations

The TLC2943 contains high frequency analog oscillators; therefore, very careful breadboarding and printed-circuit-board (PCB) layout is required for evaluation.

The following design recommendations benefit the TLC2943 user:

- External analog and digital circuitry should be physically separated and shielded as much as possible to reduce system noise.
- RF breadboarding or RF PCB techniques should be used throughout the evaluation and production process.
- Wide ground leads or a ground plane should be used on the PCB layouts to minimize parasitic inductance and resistance. The ground plane is the better choice for noise reduction.
- LOGIC V_{DD} and VCO V_{DD} should be separate PCB traces and connected to the best filtered supply point available in the system to minimize supply cross-coupling.
- VCO V_{DD} to GND and LOGIC V_{DD} to GND should be decoupled with a 0.1-µF capacitor placed as close as possible to the appropriate device terminals.
- The no-connection (NC) terminal on the package should be connected to GND.

The evaluation and operation schematic for the TLC2943 is shown in Figure 22.



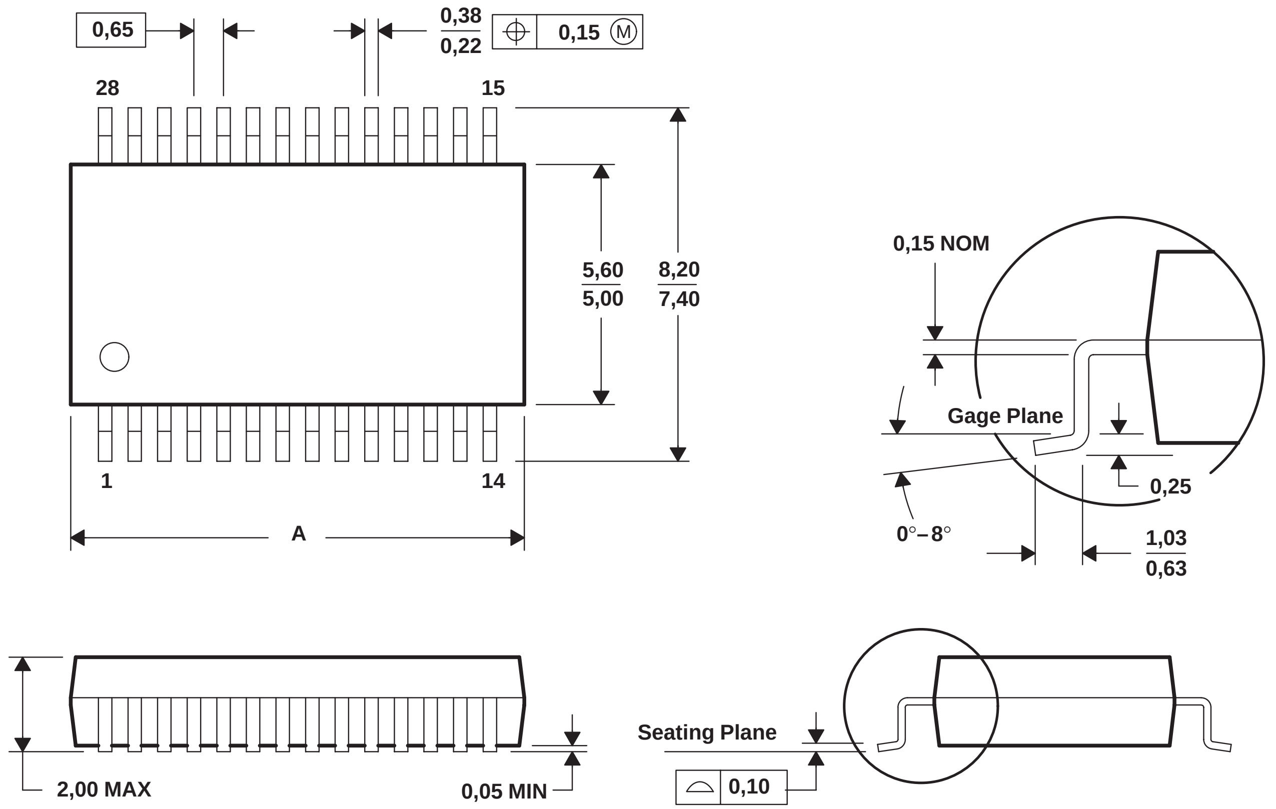
† R_{BIAS} resistor

Figure 22. Evaluation and Operation Schematic

MECHANICAL DATA

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

28 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28	30	38
A MAX	3,30	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	2,70	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 / C 10/95

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TLC2943IDB	OBSOLETE	SSOP	DB	38		TBD	Call TI	Call TI
TLC2943IDBR	OBSOLETE	SSOP	DB	38		TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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