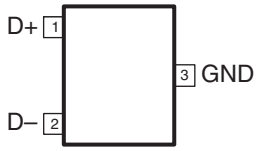
2, 4-CHANNEL ESD SOLUTION FOR SUPER-SPEED (6 GBPS) USB 3.0 INTERFACE

Check for Samples: TPD2EUSB30, TPD4EUSB30

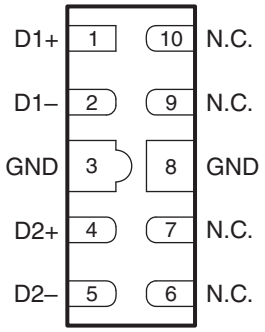
FEATURES

- **Single and Dual-Pair Differential Lines to Protect the Differential Data and Clock Lines of the USB3.0, eSATA, or LVD Interface**
- **Flow-Through Pin Mapping for the High-Speed Lines Ensures Zero Additional Skew Due to Board Layout While Placing ESD-Protection Chip Near the Connector**
- **Supports Data Rates in Excess of 6 Gbps**
- **ESD Protection Meets or Exceeds IEC61000-4-2 (Level 4)**
- **Low Capacitance 0.05pF (IO to IO)**
- **5-A Peak Pulse Current (per 8/20 μs Pulse)**
- **Industrial Temperature Range: –40°C to 85°C**
- **Space-Saving DRT, DQA Packages**

TPD2EUSB30DRTR PACKAGE
(TOP VIEW)



TPD4EUSB30DQAR PACKAGE
(TOP VIEW)



APPLICATIONS

- **Notebooks**
- **Set-Top Boxes**
- **DVD Players**
- **Media Players**
- **Portable Computers**

DESCRIPTION/ORDERING INFORMATION

The TPD2EUSB30 and TPD4EUSB30 provide 2 and 4 channel ESD clamp circuits with flow-through pin mapping for ease of board layout. These devices have been designed to protect sensitive components which are connected to ultra high-speed data and transmission lines. The TPDxEUSB30 offer protection from stress caused by ESD (electrostatic discharge). These devices also offer 5 A (8/20 μs) peak pulse current ratings per IEC 61000-4-5 (lightning) specification.

The monolithic silicon technology allows matching between the differential signal pairs. The differential 0.05-pF capacitance ensures that the signal distortion due to added ESD clamp remains minimal at high-speed differential data transmission.

The TPD2EUSB30 and TPD4EUSB30 conform to IEC61000-4-2 (Level 4) ESD protection. The TPD2EUSB30 is offered in space saving DRT (1 mm × 1 mm) package. The TPD4EUSB30 is offered in space saving DQA (1 mm × 2.5 mm) package.

The TPD2EUSB30 and TPD4EUSB30 are characterized for operation over ambient air temperature range of –40°C to 85°C.

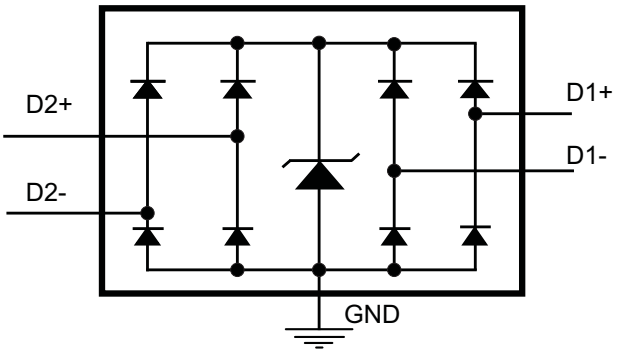
ORDERING INFORMATION

T_A	PACKAGE(1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOT – DRT	Tape and reel	TPD2EUSB30DRTR	5PX
	SON – DQA	Tape and reel	TPD4EUSB30DQAR	66R

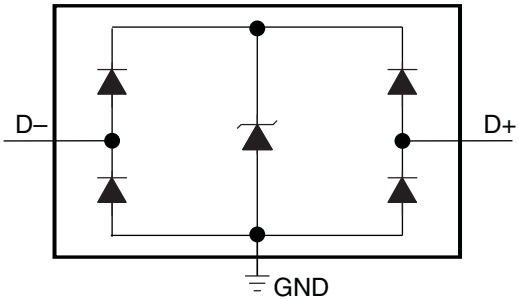
(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

CIRCUIT DIAGRAMS

TPD4EUSB30DQA Circuit



TPD2EUSB30DRT Circuit



TERMINAL FUNCTIONS

TERMINAL			TYPE	DESCRIPTION
NAME	DRT PIN NO.	DQA PIN NO.		
Dx+, Dx–	1, 2	1,2, 4, 5	ESD port	High-speed ESD clamp, provides ESD protection to the high-speed differential data lines
GND	3	3, 8	GND	Ground
N.C.		6, 7, 9, 10		Not normally connected

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
	IO voltage tolerance		D+, D– pins	0	6	
T_A	Operating free-air temperature range			–40	85	°C
T_{stg}	Storage temperature range			–65	125	°C
	ESD protection	IEC 61000-4-2 Contact Discharge	D+, D– pins		±8	kV
		IEC 61000-4-2 Air-Gap Discharge (TPD2EUSB30)	D+, D– pins		±8	kV
		IEC 61000-4-2 Air-Gap Discharge (TPD4EUSB30)	D+, D– pins		±9	kV
	Peak pulse current (t_p = 8/20 μs)		D+, D– pins		5	A
	Peak pulse power (t_p = 8/20 μs)		D+, D– pins		45	W

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	D+,D– pins to ground				5.5	V
V_{clamp}	Clamp voltage	D+,D– pins to ground,	I_{IO} = 1 A			8	V
I_{IO}	Current from IO port to supply pins	V_{IO} = 2.5 V,	I_D = 8 mA		0.01	0.1	μA
V_D	Diode forward voltage	D+,D– pins, lower clamp diode,	V_{IO} = 2.5 V, I_D = 8 mA	0.6	0.8	0.95	V
R_{dyn}	Dynamic resistance	D+,D– pins	I = 1 A		1		Ω
C_{IO-IO}	Capacitance IO to IO	D+,D– pins	V_{IO} = 2.5 V		0.05		pF
C_{IO-GND}	Capacitance IO to GND	D+,D– pins (DRT)	V_{IO} = 2.5 V		0.7		pF
		D1+, D1-, D2+, D2- (DQA)			0.8		
V_{BR}	Break-down voltage	I_{IO} = 1 mA		7			V

TYPICAL OPERATING CHARACTERISTICS

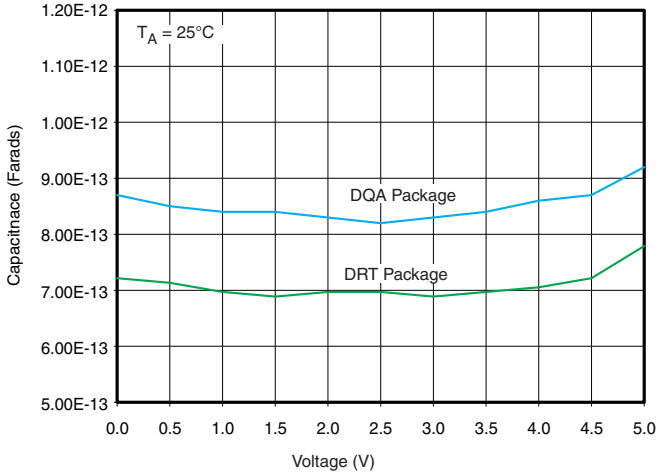


Figure 1. IO Capacitance vs IO Voltage

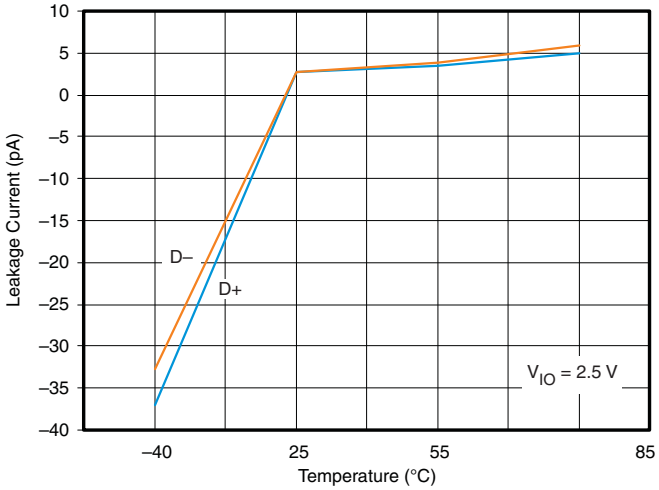


Figure 2. Leakage Current vs Temperature

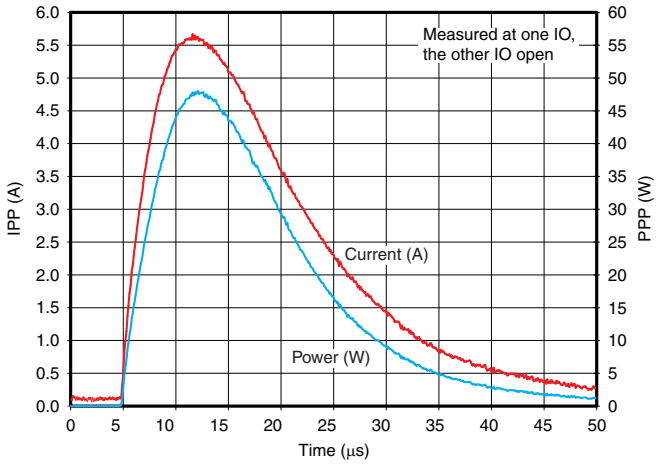


Figure 3. Peak Pulse Waveforms

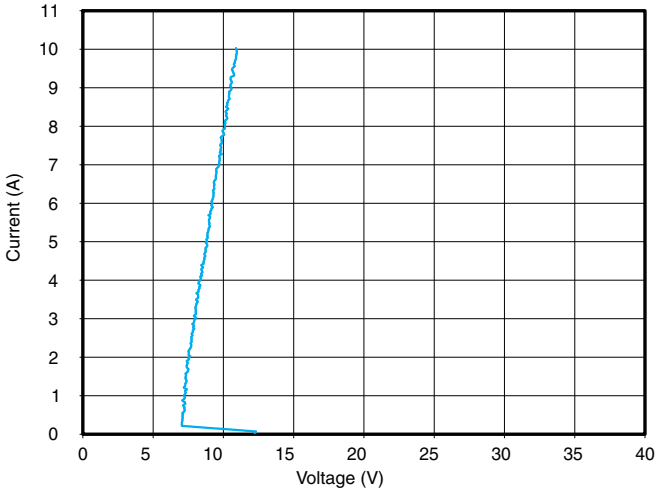


Figure 4. D+,D– Transmission Line Pulser Plot (100 ns Pulse, 10 ns Rise Time)

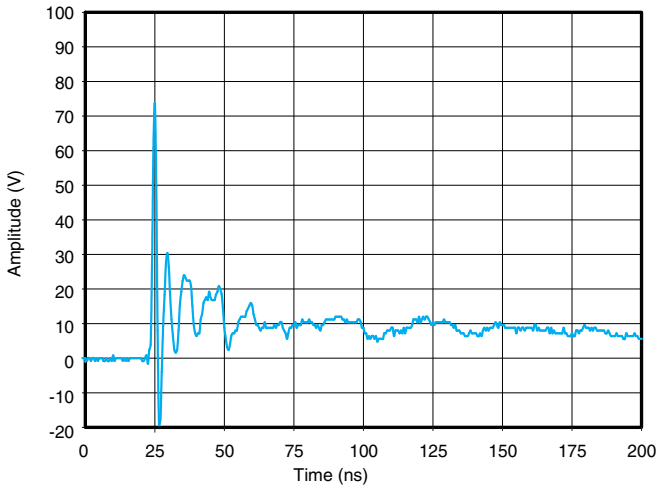


Figure 5. IEC Clamping Waveforms (8 kV Contact)

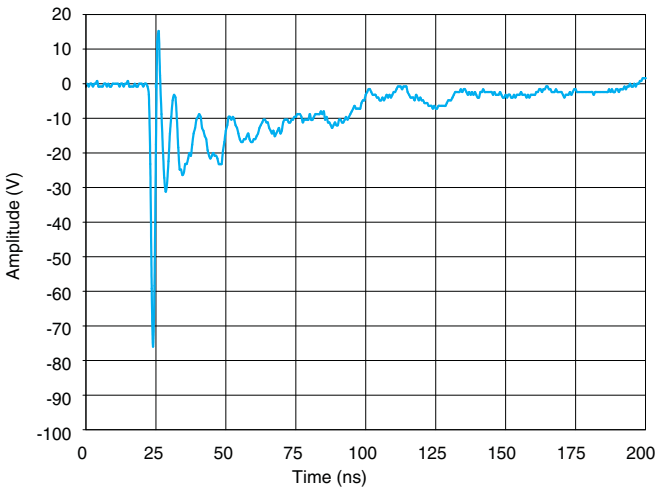


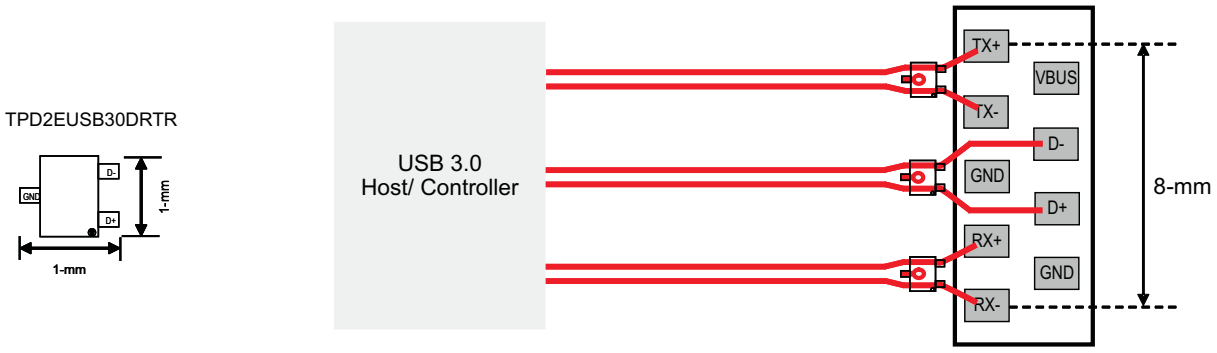
Figure 6. IEC Clamping Waveforms (–8 kV Contact)

APPLICATION INFORMATION

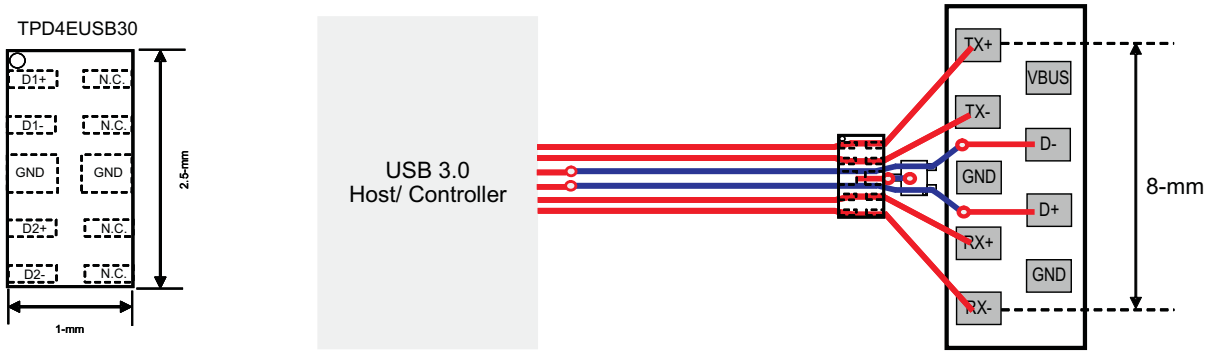
Layout Guide with TPDxEUSB30DRTR

Refer to Figure 7, the TPD2EUSB30DRTR is offered in space saving DRT package. The DRT package is a 1mm* 1mm package with flow-through pin-mapping for the high-speed differential lines. The TPD4EUSB30DRTR is offered in space saving DQA package. The DQA is a 1mm* 2.5mm package with flow-through pin-mapping for the high-speed differential lines. It is recommended to place the package right next to the USB 3.0 connector. The GND pin should connected to GND plane of the board through a large VIA. If a dedicated GND plane is not present right underneath, it is recommended to route to the GND plane through a wide trace. The current associated with IEC ESD stress can be in the range of 30Amps or higher momentarily. A good, low impedance GND path ensures the system robustness against IEC ESD stress.

The TPDxEUSB30 can provide system level ESD protection to the high-speed differential ports (>6 Gbps data rate). The flow-through package offers flexibility for board routing with traces up to 15 mills wide. It allows the differential signal pairs couple together right after they touch the ESD ports of the TPDxEUSB30.



Three TPD2EUSB30 to Protect USB3.0 Class A connector (One Layer Routing)



One TPD4EUSB30 & One TPD2EUSB30 to Protect USB3.0 Class A connec tor (Two Layer Routing)

Figure 7. Layout Guide with the TPDxEUSB30 at the USB3.0 Class A Connector

TPDxEUSB30 Eye Pattern Test

See Figure 9 for a demonstration of the TPDxEUSB30 performance the lab set-up. Figure 8 shows a lab board that was designed to demonstrate the degradation of the eye pattern quality with and without the TPD2EUSB30 in the USB 3.0 signal path. Figure 10 shows that there is only ~2 ps jitter penalty to the differential signal when the TPD2EUSB30 device was added in the signal path. Similar setup was employed to measure eye pattern for the TPD4EUSB30.

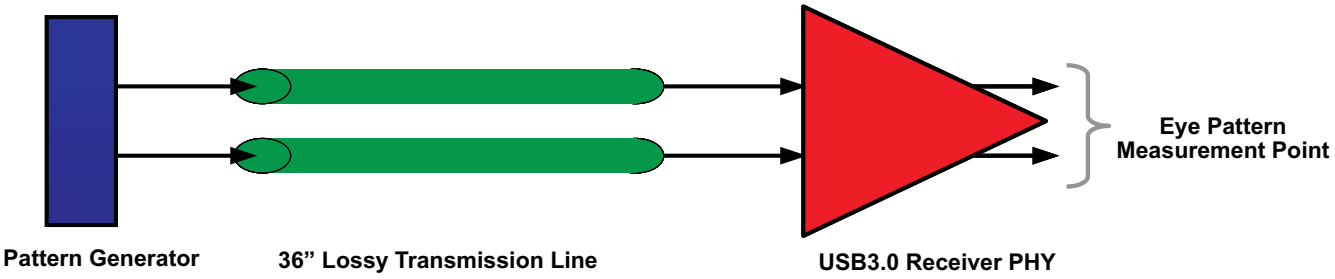


Figure 8. Measurement Setup to collect the Eye Pattern on a Reference Board with TPD2EUSB30

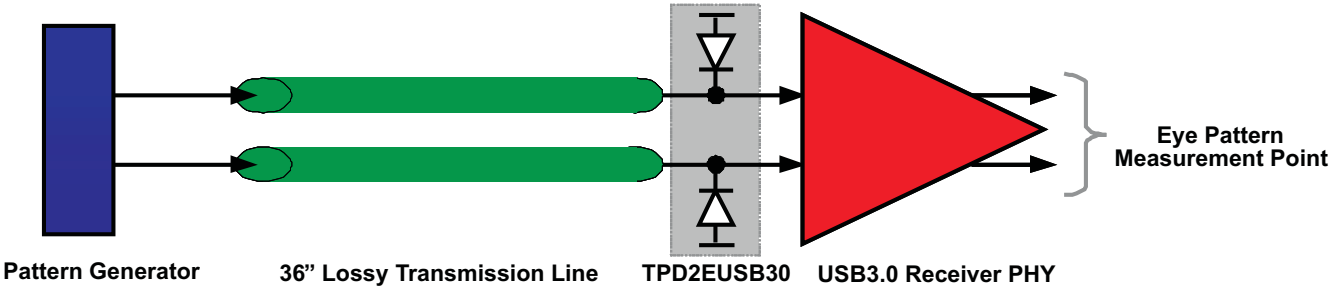


Figure 9. Measurement Setup to collect the Eye Pattern on a Reference Board with TPD2EUSB30

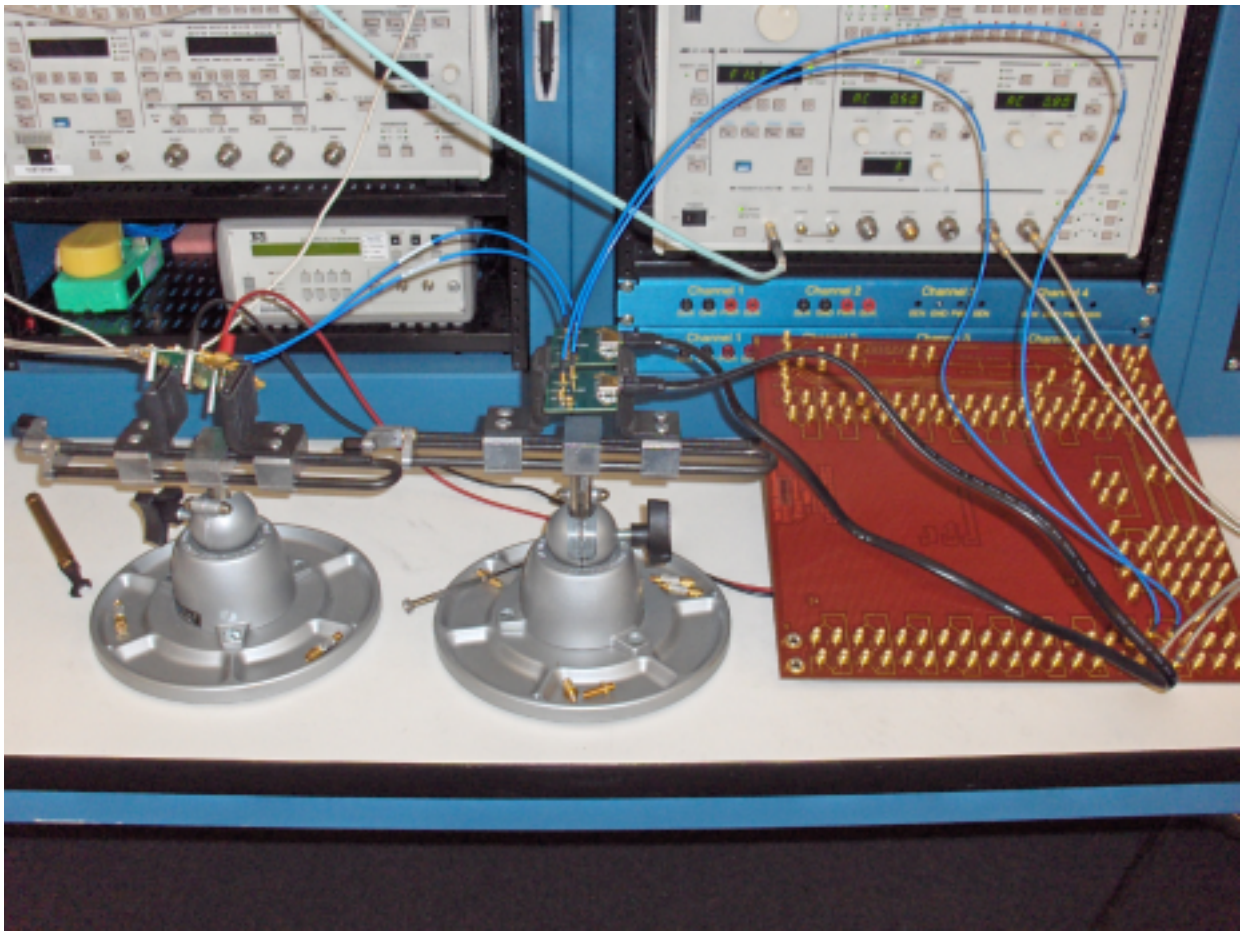


Figure 10. Lab Setup for the Eye-Pattern Measurement with TPDxEUSB30

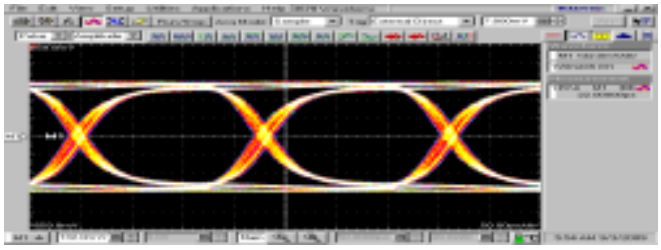


Figure 11. Output Eye Diagram Without TPD2EUSB30 (Figure 8 Setup, 5 Gbps Data Rate)

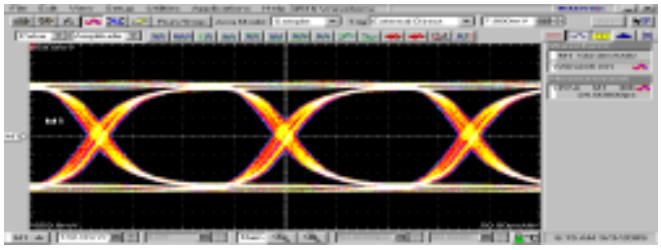


Figure 12. Output Eye Diagram with the TPD2EUSB30 (Figure 8 Setup, 5 Gbps Data Rate)

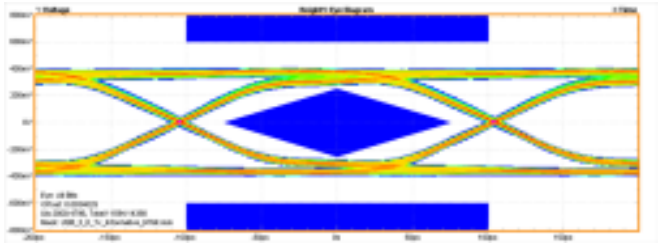


Figure 13. Output Eye Diagram Without the TPD4EUSV30 (5 Gbps Data Rate)

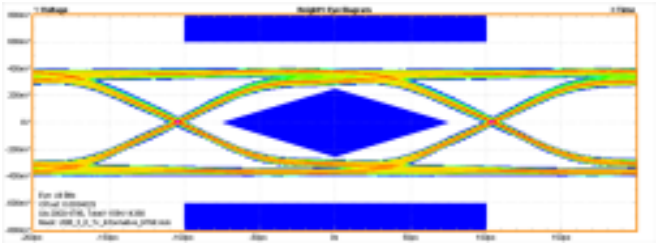


Figure 14. Output Eye Diagram with the TPD4EUSV30 (5 Gbps Data Rate)

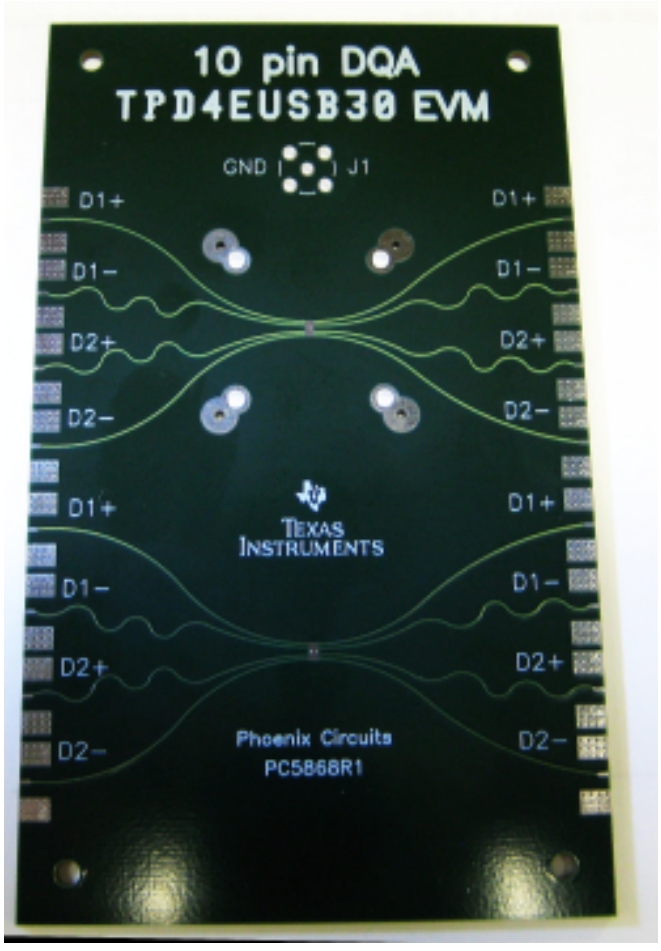


Figure 15. TPDxEUSV30 EVM – TPD4EUSB30 Side

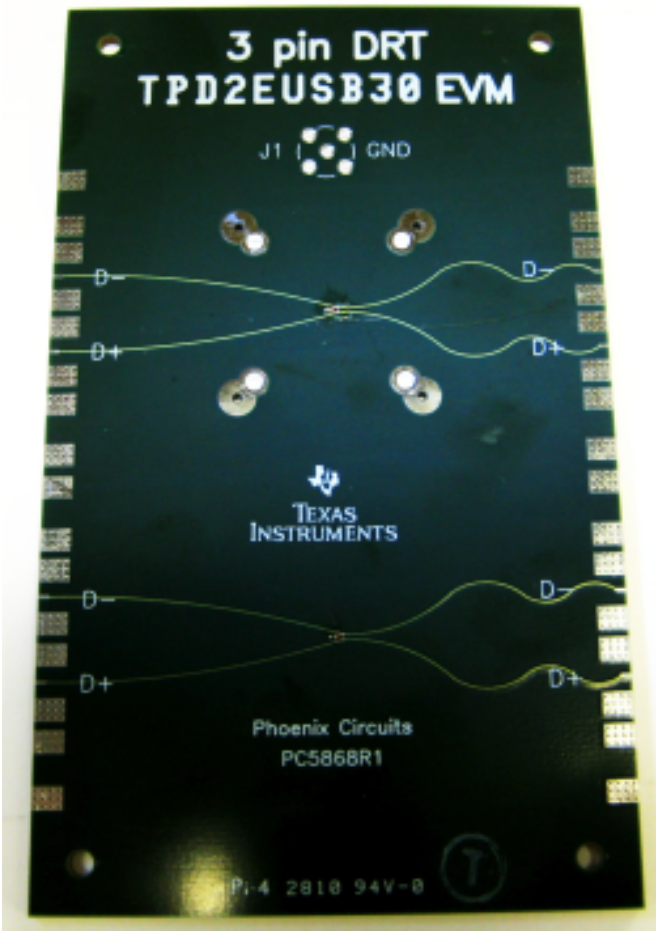


Figure 16. TPDxEUSV30 EVM – TPD2EUSB30 Side

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPD2EUSB30DRTR	ACTIVE	SOT	DRT	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
TPD4EUSB30DQAR	ACTIVE	SON	DQA	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples

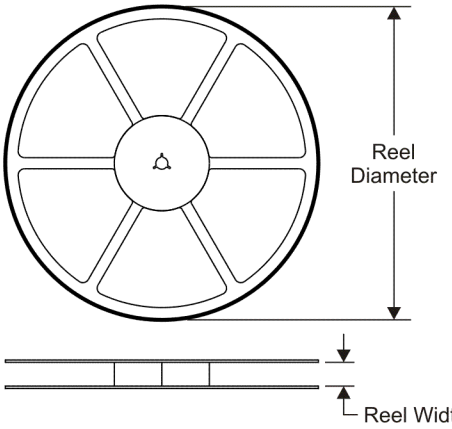
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

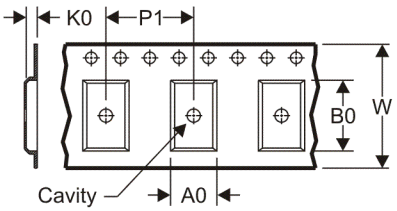
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

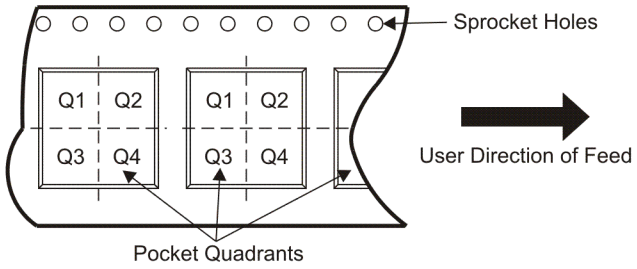


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

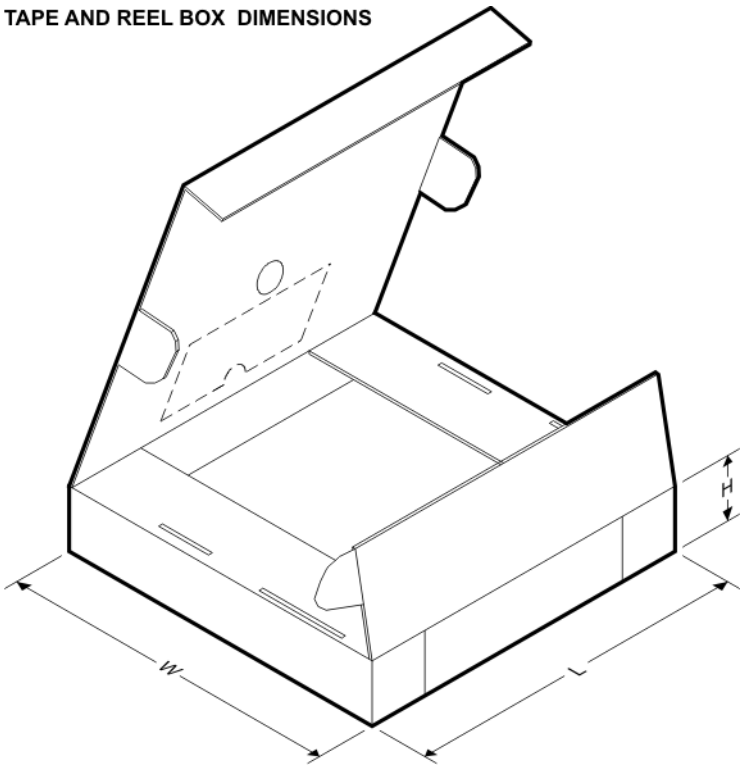
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

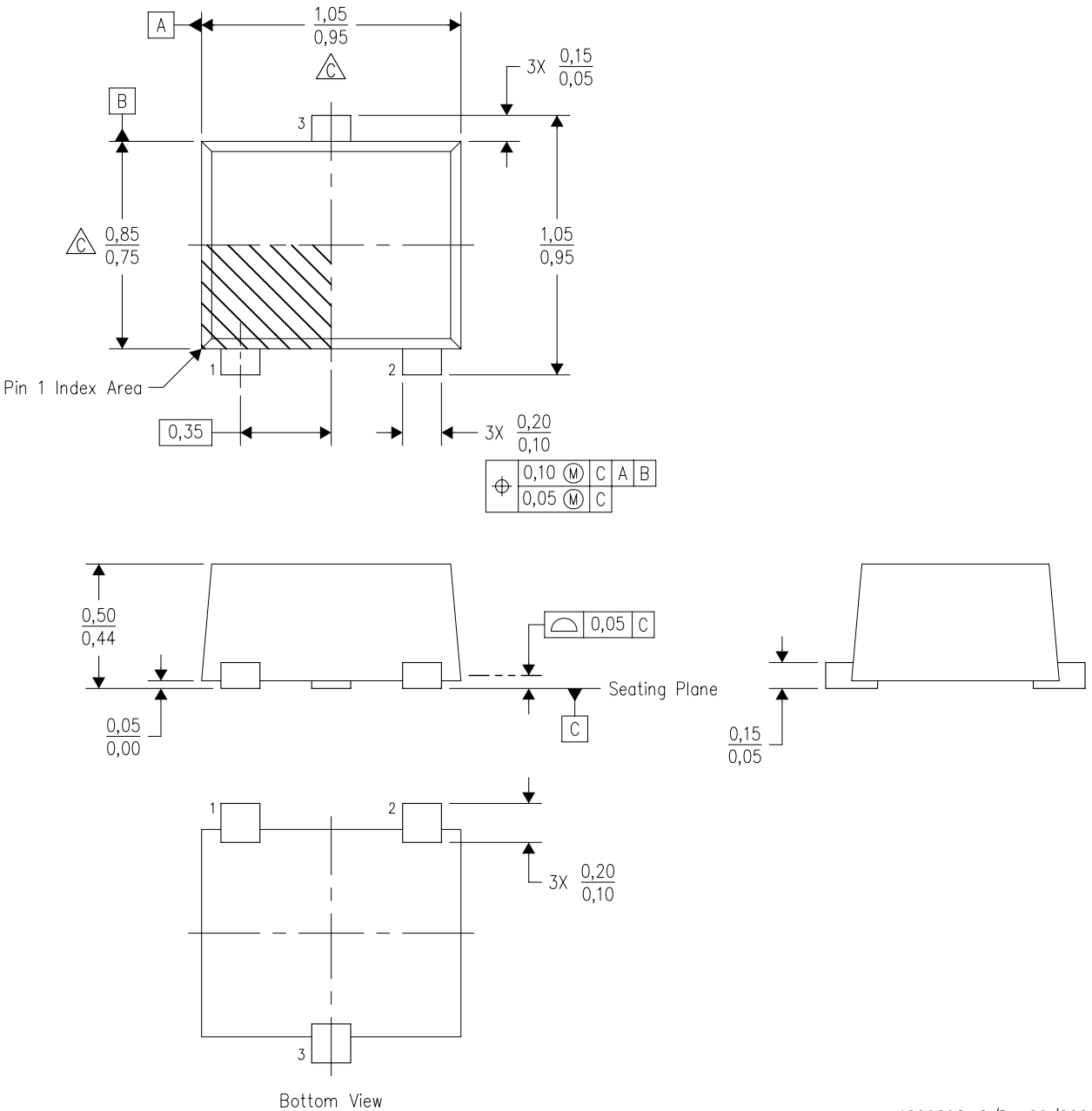
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD2EUSB30DRTR	SOT	DRT	3	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q3
TPD4EUSB30DQAR	SON	DQA	10	3000	180.0	8.4	1.3	2.83	0.65	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



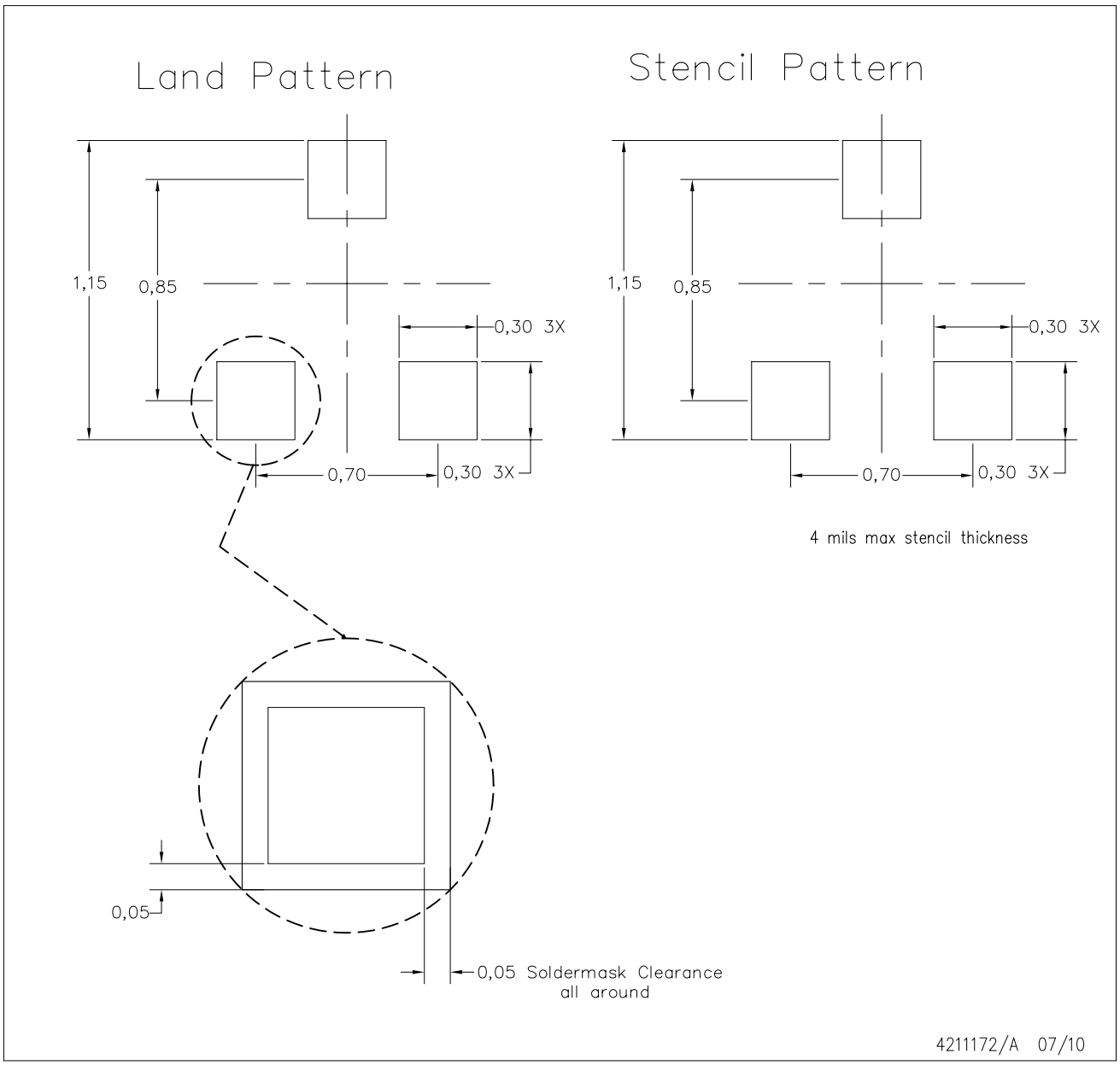
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD2EUSB30DRTR	SOT	DRT	3	3000	202.0	201.0	28.0
TPD4EUSB30DQAR	SON	DQA	10	3000	202.0	201.0	28.0



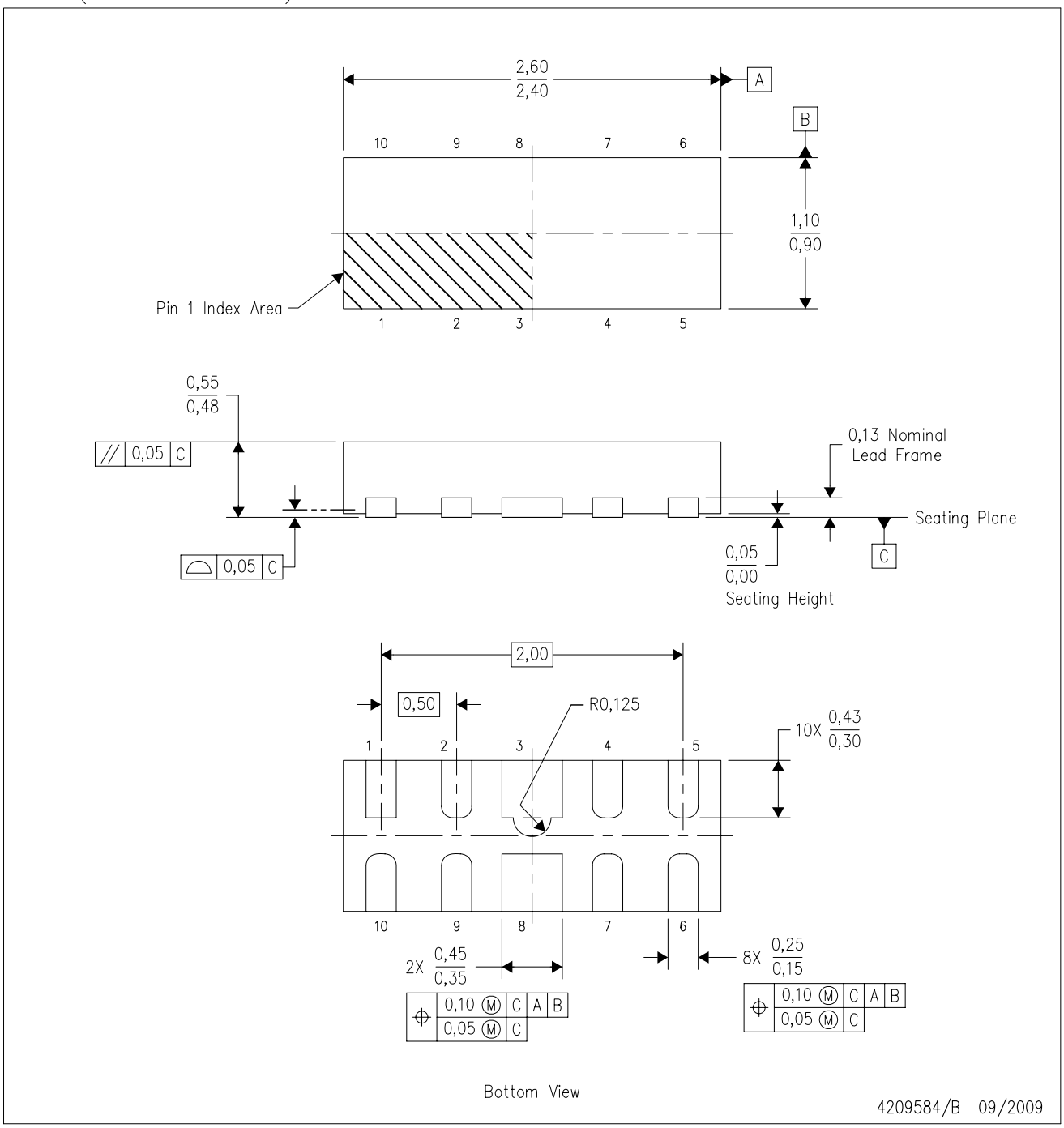
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,10 per end or side.
D. JEDEC package registration is pending.

DRT (S–PDSO–N3) PLASTIC SMALL OUTLINE



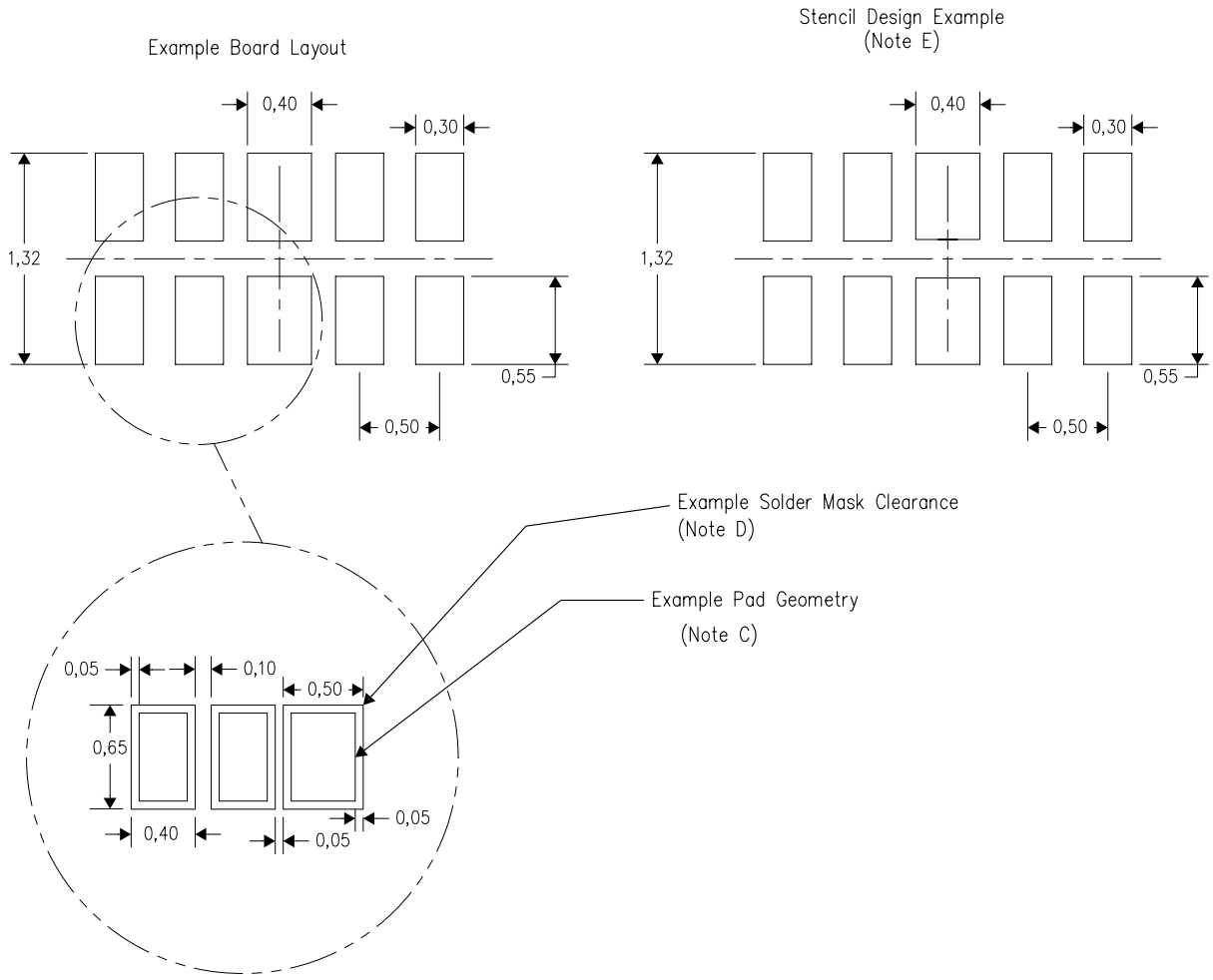
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DQA (R–PSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.

DQA (R–PSON–N10)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Communications and Telecom	www.ti.com/communications
DSP	dsp.ti.com	Computers and Peripherals	www.ti.com/computers
Clocks and Timers	www.ti.com/clocks	Consumer Electronics	www.ti.com/consumer-apps
Interface	interface.ti.com	Energy	www.ti.com/energy
Logic	logic.ti.com	Industrial	www.ti.com/industrial
Power Mgmt	power.ti.com	Medical	www.ti.com/medical
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Space, Avionics & Defense	www.ti.com/space-avionics-defense
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video and Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless-apps

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265