TPD4E001
LOW-CAPACITANCE 4-CHANNEL ±15-kV ESD PROTECTION ARRAY FOR HIGH-SPEED DATA INTERFACES

SLLS682C – JULY 2006 – REVISED APRIL 2007

FEATURES

- **ESD Protection Exceeds**
  - **±15-kV Human-Body Model (HBM)**
  - **±8-kV IEC 61000-4-2 Contact Discharge**
  - **±15-kV IEC 61000-4-2 Air-Gap Discharge**
- **Low 1.5-pF Input Capacitance**
- **Low 1-nA (Max) Leakage Current**
- **Low 1-nA Supply Current**
- **0.9-V to 5.5-V Supply-Voltage Range**
- **Four-Channel Device**
- **Space-Saving DRL and QFN Package Options**
- **Alternate 2-, 3-, 6-Channel Options Available: TPD2E001, TPD3E001, and TPD6E001**

APPLICATIONS

- **USB 2.0**
- **Ethernet**
- **FireWire™**
- **Video**
- **Cell Phones**
- **SVGA Video Connections**
- **Glucosemeters**

DESCRIPTION/ORDERING INFORMATION

The TPD4E001 is a low-capacitance ±15-kV ESD-protection diode array designed to protect sensitive electronics attached to communication lines. Each channel consists of a pair of diodes that steer ESD current pulses to V_{CC} or GND. The TPD4E001 protects against ESD pulses up to ±15-kV Human-Body Model (HBM), ±8-kV Contact Discharge, and ±15-kV Air-Gap Discharge, as specified in IEC 61000-4-2. This device has a 1.5-pF capacitance per channel, making it ideal for use in high-speed data IO interfaces.

The TPD4E001 is a quad-ESD structure designed for Ethernet and FireWire™ applications.

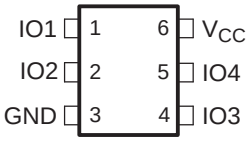
The TPD4E001 is available in DRL and thin QFN packages and is specified for –40°C to 85°C operation.

ORDERING INFORMATION

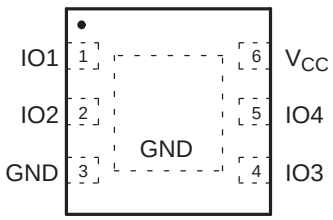
T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	1.6 × 1.6 DRL	Reel of 4000	TPD4E001DRLR	2CR
	3 × 3 QFN	Reel of 1000	TPD4E001DRSR	ZWM

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

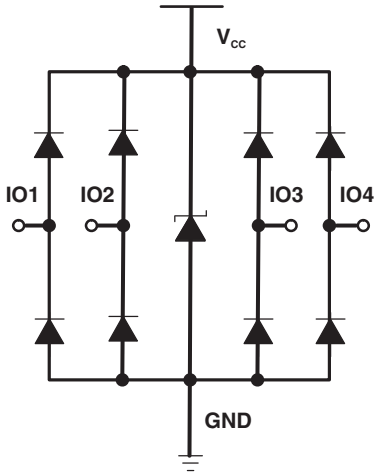
DRL PACKAGE (TOP VIEW)



QFN PACKAGE (TOP VIEW)



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

QFN/DRL NO.	NAME	FUNCTION
1, 2, 4, 5	IOx	ESD-protected channel
3	GND	Ground
6	V_{CC}	Power-supply input. Bypass V_{CC} to GND with a 0.1-µF ceramic capacitor.
EP	EP	Exposed pad. Connect to GND.

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}			–0.3	7	V
$V_{I/O}$			–0.3	V_{CC} + 0.3	V
T_{stg}	Storage temperature range		–65	150	°C
T_J	Junction temperature			150	°C
	Bump temperature (soldering)	Infrared (15 s)		220	°C
		Vapor phase (60 s)		215	
	Lead temperature (soldering, 10 s)			300	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

V_{CC} = 5 V ± 10%, T_A = -40°C to 85°C (unless otherwise noted)

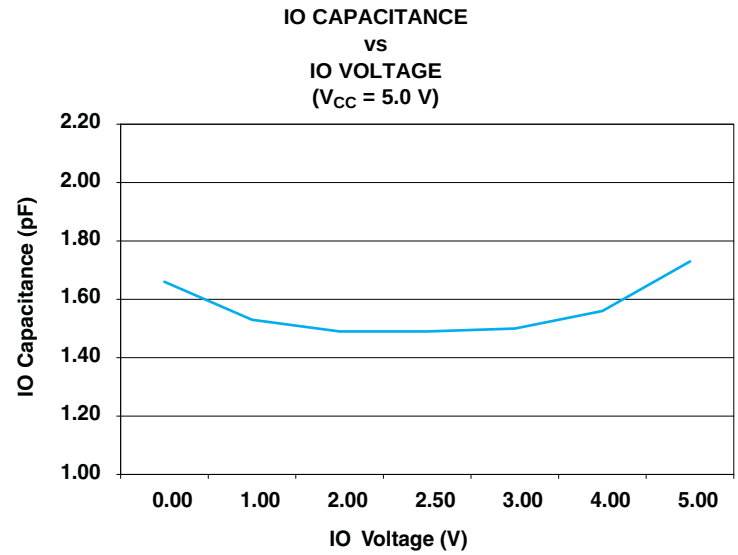
PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{CC}	Supply voltage			0.9		5.5	V
I_{CC}	Supply current				1	100	nA
V_F	Diode forward voltage	I_F = 10 mA		0.65		0.95	V
V_{BR}	Breakdown Voltage	I_{BR} = 10mA		11			V
V_C	Channel clamp voltage(2)	T_A = 25°C, ±15-kV HBM, I_F = 10 A	Positive transients			V_{CC} + 25	V
			Negative transients			–25	
		T_A = 25°C, ±8-kV Contact Discharge (IEC 61000-4-2), I_F = 24 A	Positive transients			V_{CC} + 60	
			Negative transients			–60	
		T_A = 25°C, ±15-kV Air-Gap Discharge (IEC 61000-4-2), I_F = 45 A	Positive transients			V_{CC} + 100	
			Negative transients			–100	
$I_{i/o}$	Channel leakage current	$V_{i/o}$ = GND to V_{CC}				±1	nA
$C_{i/o}$	Channel input capacitance	V_{CC} = 5 V, Bias of V_{CC}/2			1.5		pF

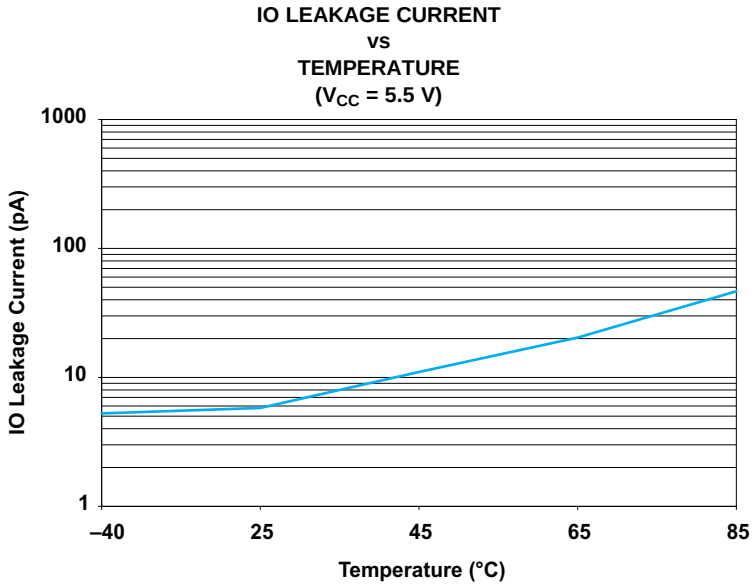
(1) Typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) Channel clamp voltage is not production tested

ESD Protection

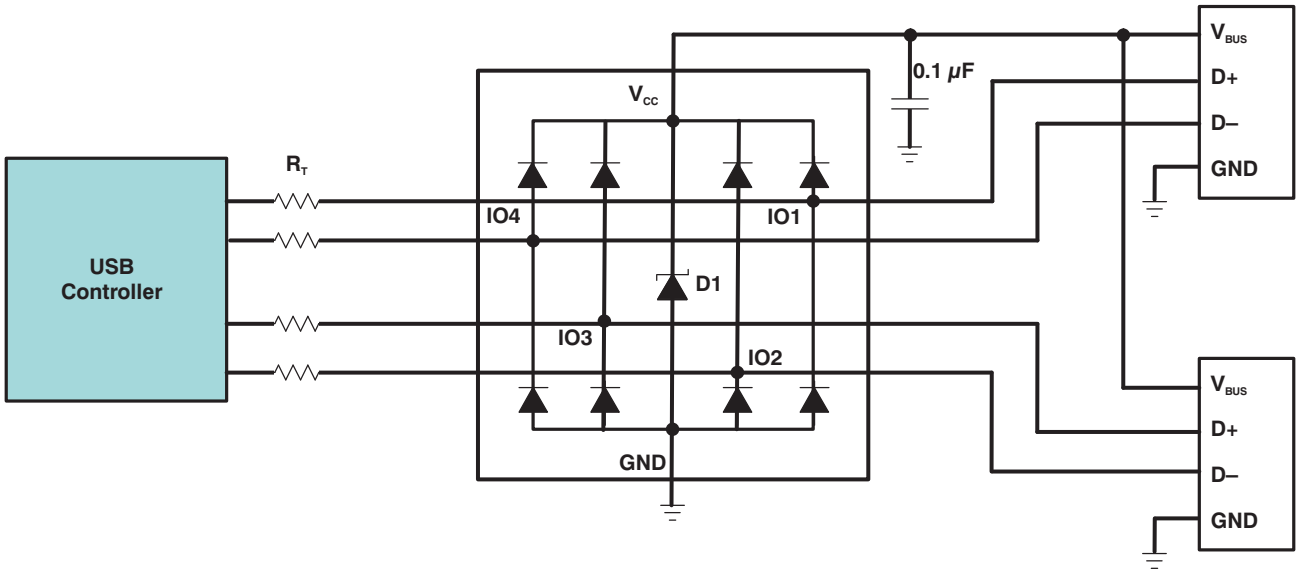
PARAMETER	TYP	UNIT
HBM	±15	kV
IEC 61000-4-2 Contact Discharge	±8	kV
IEC 61000-4-2 Air-Gap Discharge	±15	kV

TYPICAL OPERATING CHARACTERISTICS





APPLICATION INFORMATION



Detailed Description

When placed near the connector, the TPD4E001 ESD solution offers little or no signal distortion during normal operation due to low IO capacitance and ultra-low leakage current specifications. The TPD4E001 ensures that the core circuitry is protected and the system is functioning properly in the event of an ESD strike. For proper operation, the following layout/ design guidelines should be followed:

1. Place the TPD4E001 solution close to the connector. This allows the TPD4E001 to take away the energy associated with ESD strike before it reaches the internal circuitry of the system board.
2. Place a 0.1-μF capacitor very close to the V_{CC} pin. This limits any momentary voltage surge at the IO pin during the ESD strike event.
3. Ensure that there is enough metallization for the V_{CC} and GND loop. During normal operation, the TPD4E001 consumes nA leakage current. But during the ESD event, V_{CC} and GND may see 15 A to 30 A of current, depending on the ESD level. Sufficient current path enables safe discharge of all the energy associated with the ESD strike.
4. Leave the unused IO pins floating .
5. The V_{CC} pin can be connected in two different ways:
   a. If the V_{CC} pin is connected to the system power supply, the TPD4E001 works as a transient suppressor for any signal swing above V_{CC} + V_F. A 0.1-μF capacitor on the device V_{CC} pin is recommended for ESD bypass.
   b. If the V_{CC} pin is not connected to the system power supply, the TPD4E001 can tolerate higher signal swing in the range up to 10V. Please note that a 0.1μF capacitor is still recommended at the V_{CC} pin for ESD bypass.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPD4E001DRLR	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPD4E001DRLRG4	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPD4E001DRSR	ACTIVE	SON	DRS	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

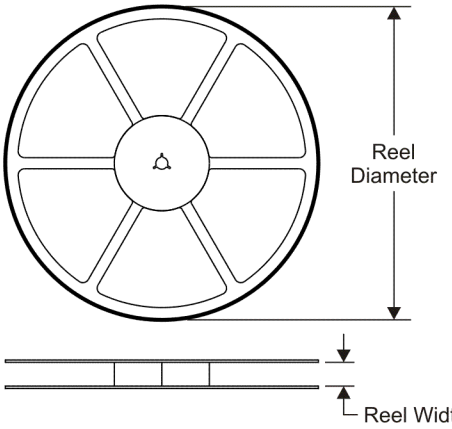
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

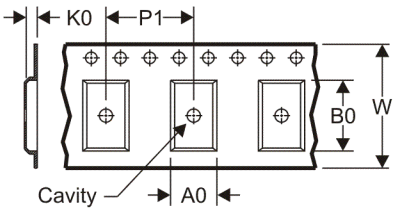
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

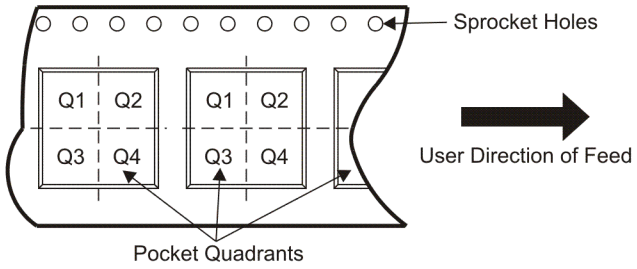


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

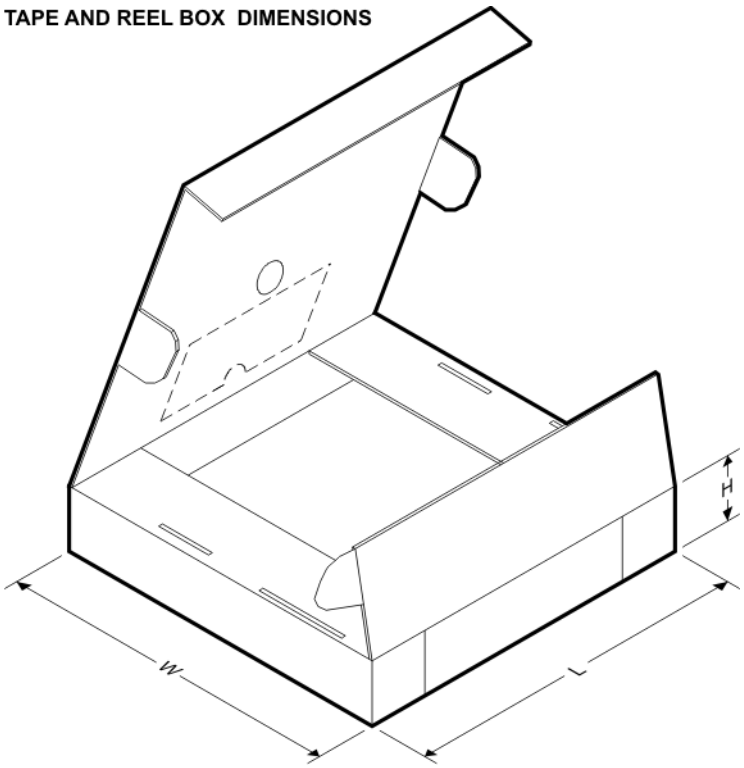
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

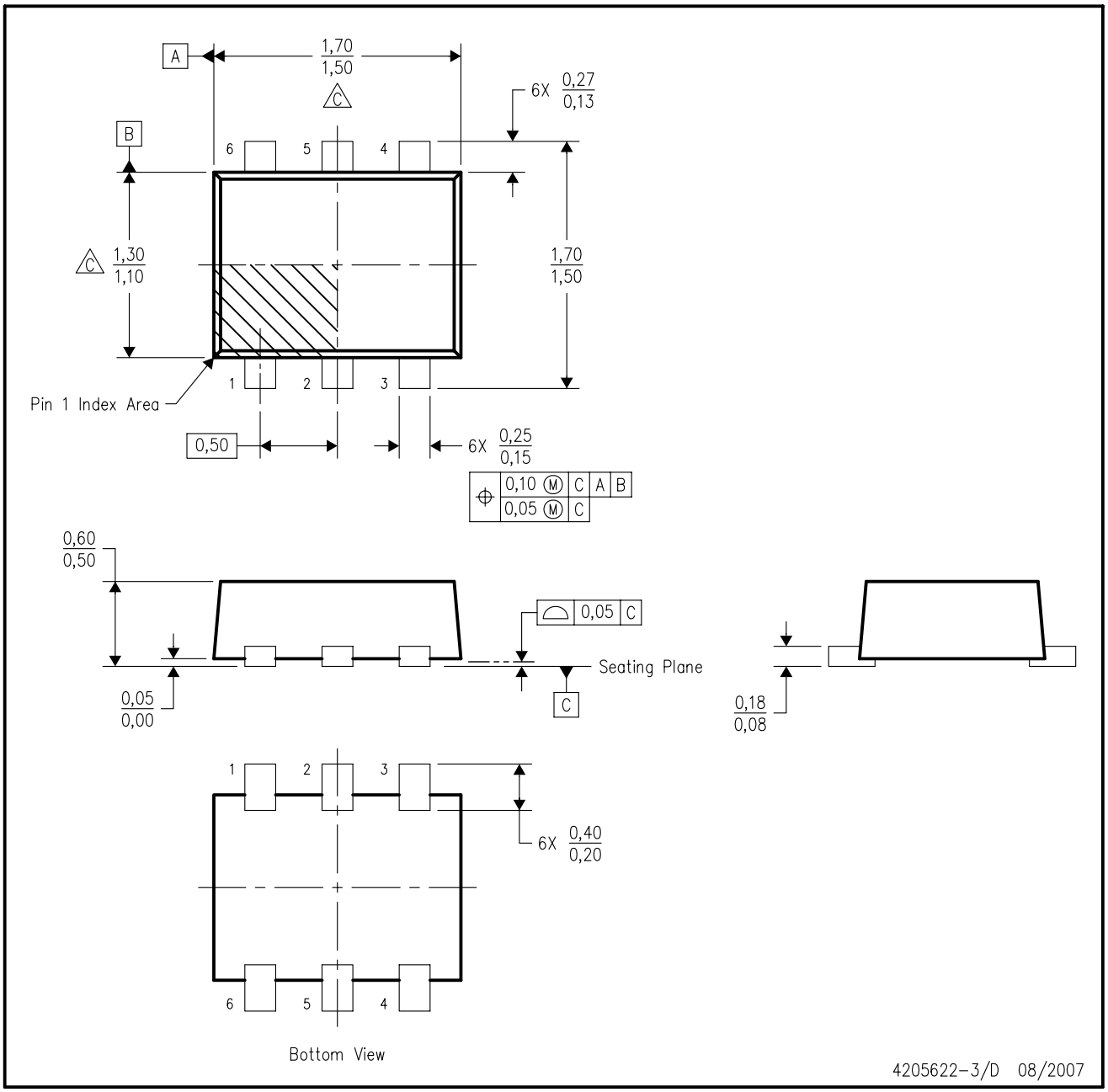
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4E001DRLR	SOT	DRL	6	4000	180.0	9.2	1.78	1.78	0.69	4.0	8.0	Q3
TPD4E001DRSR	SON	DRS	6	1000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



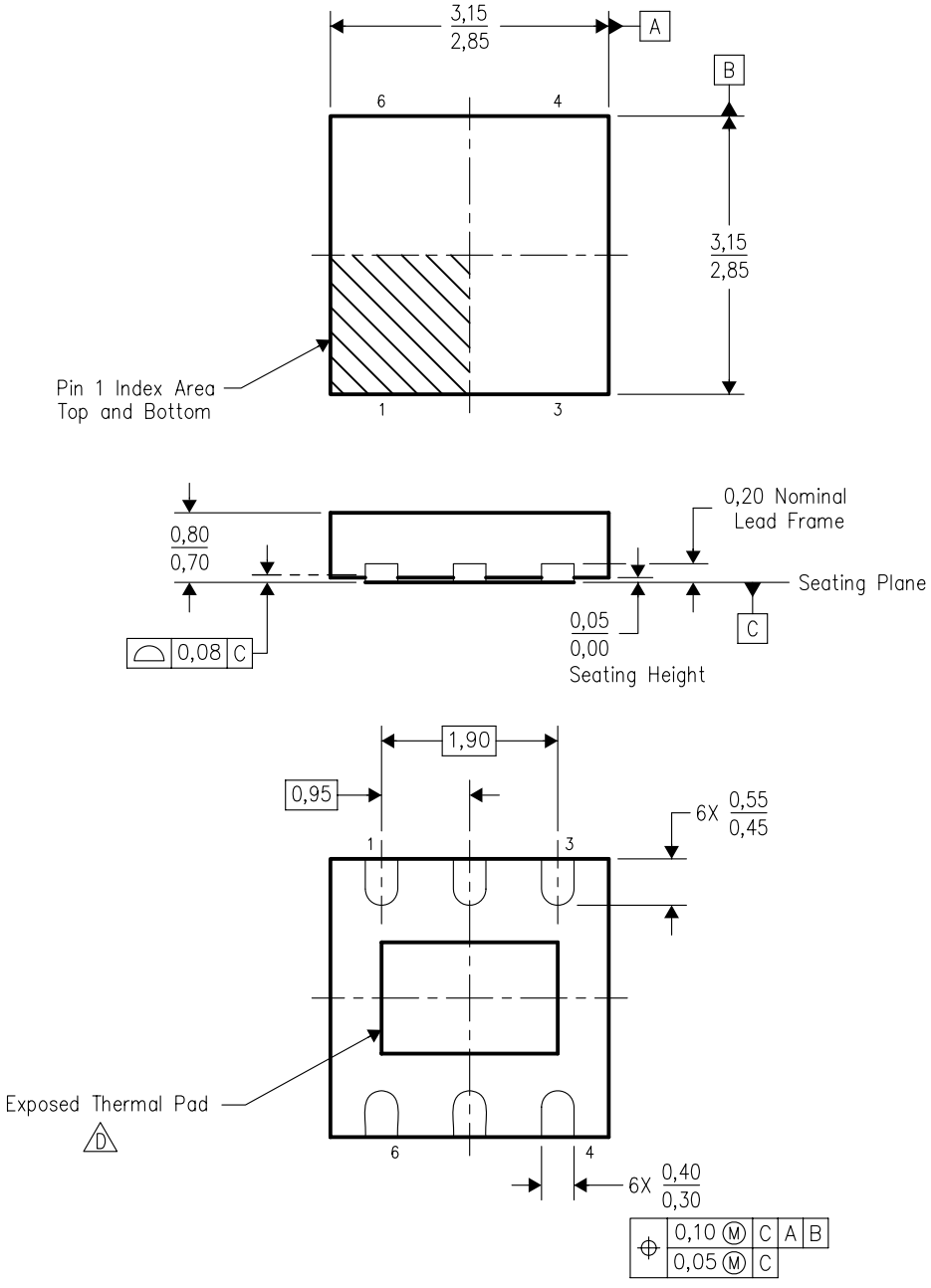
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4E001DRLR	SOT	DRL	6	4000	202.0	201.0	28.0
TPD4E001DRSR	SON	DRS	6	1000	346.0	346.0	29.0



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
D. JEDEC package registration is pending.

DRS (S–PDSO–N6) PLASTIC SMALL OUTLINE



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL PAD MECHANICAL DATA

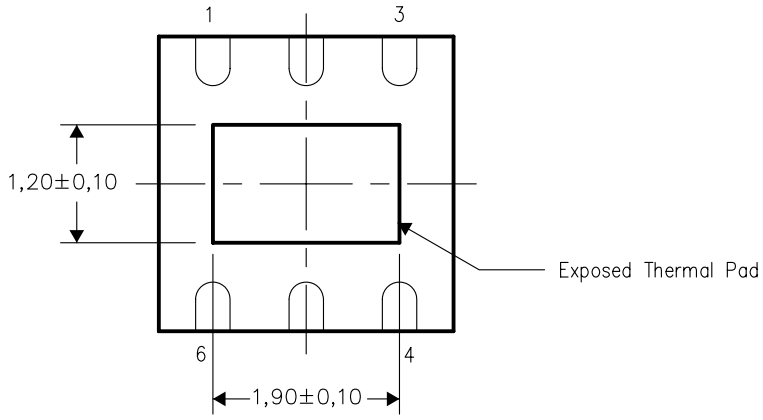
DRS (S–PDSO–N6)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

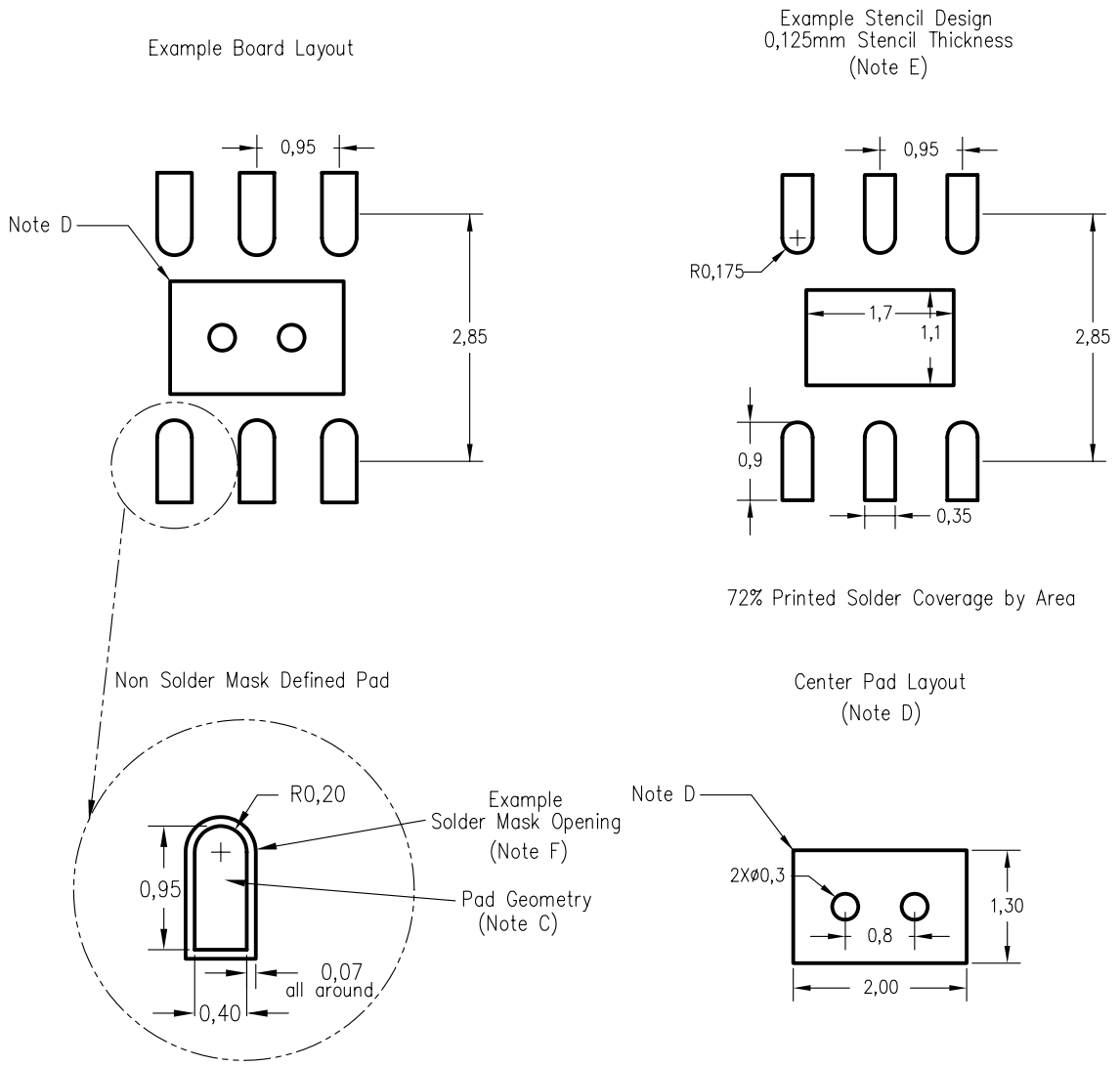


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRS (S–PDSO–N6)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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