



74ALVCH16373

LOW VOLTAGE CMOS 16-BIT D-TYPE LATCH (3-STATE) WITH 3.6V TOLERANT INPUTS AND OUTPUTS

- 3.6V TOLERANT INPUTS AND OUTPUTS
- HIGH SPEED :
 - $t_{PD} = 3.6 \text{ ns (MAX.) at } V_{CC} = 3.0 \text{ to } 3.6V$
 - $t_{PD} = 4.5 \text{ ns (MAX.) at } V_{CC} = 2.3 \text{ to } 2.7V$
 - $t_{PD} = 6.5 \text{ ns (MAX.) at } V_{CC} = 1.65V$
- POWER DOWN PROTECTION ON INPUTS AND OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
 - $|I_{OH}| = I_{OL} = 24\text{mA (MIN) at } V_{CC} = 3.0V$
 - $|I_{OH}| = I_{OL} = 18\text{mA (MIN) at } V_{CC} = 2.3V$
 - $|I_{OH}| = I_{OL} = 4\text{mA (MIN) at } V_{CC} = 1.65V$
- OPERATING VOLTAGE RANGE:
 - $V_{CC(OPR)} = 1.65V \text{ to } 3.6V$
- BUS HOLD PROVIDED ON DATA INPUTS
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 16373
- LATCH-UP PERFORMANCE EXCEEDS 300mA (JESD 17)
- ESD PERFORMANCE:
 - HBM > 2000V (MIL STD 883 method 3015);
 - MM > 200V

DESCRIPTION

The 74ALVCH16373 is a low voltage CMOS 16 BIT D-TYPE LATCH with 3 STATE OUTPUTS NON INVERTING fabricated with sub-micron silicon gate and five-layer metal wiring C²MOS technology. It is ideal for low power and very high speed 1.65 to 3.6V applications; it can be interfaced to 3.6V signal environment for both inputs and outputs.

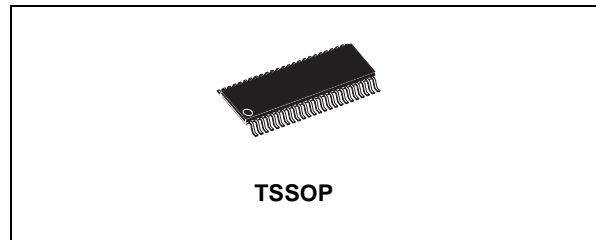
These 16 bit D-TYPE latches are bite controlled by two latch enable inputs (nLE) and two output enable inputs (OE).

While the nLE input is held at a high level, the nQ outputs will follow the data input precisely.

When the nLE is taken low, the nQ outputs will be in a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state. This device is designed to be used with 3 state memory address drivers, etc.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state.

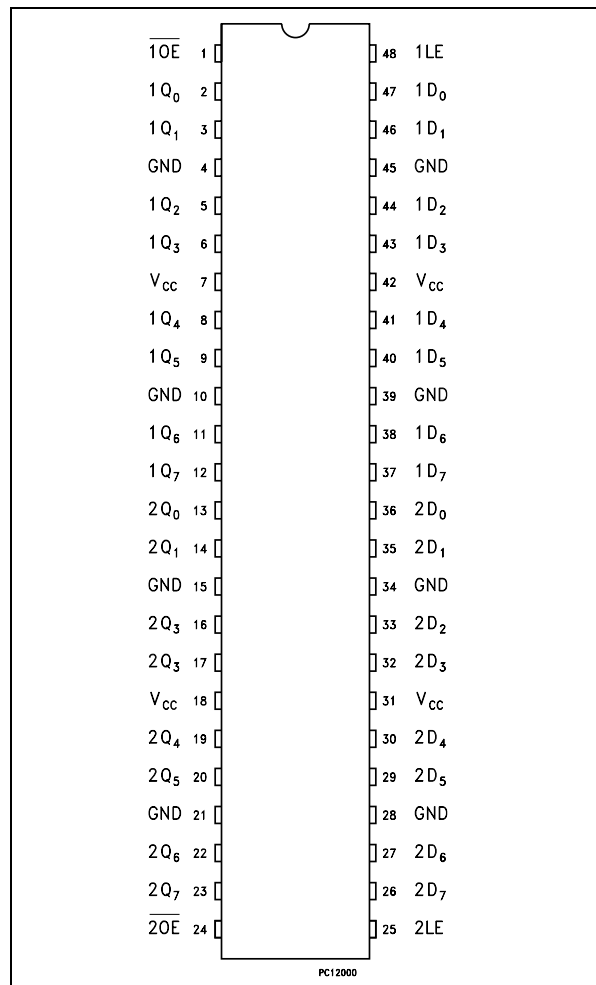
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.



ORDER CODES

PACKAGE	TUBE	T & R
TSSOP		74ALVCH16373TTR

PIN CONNECTION



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

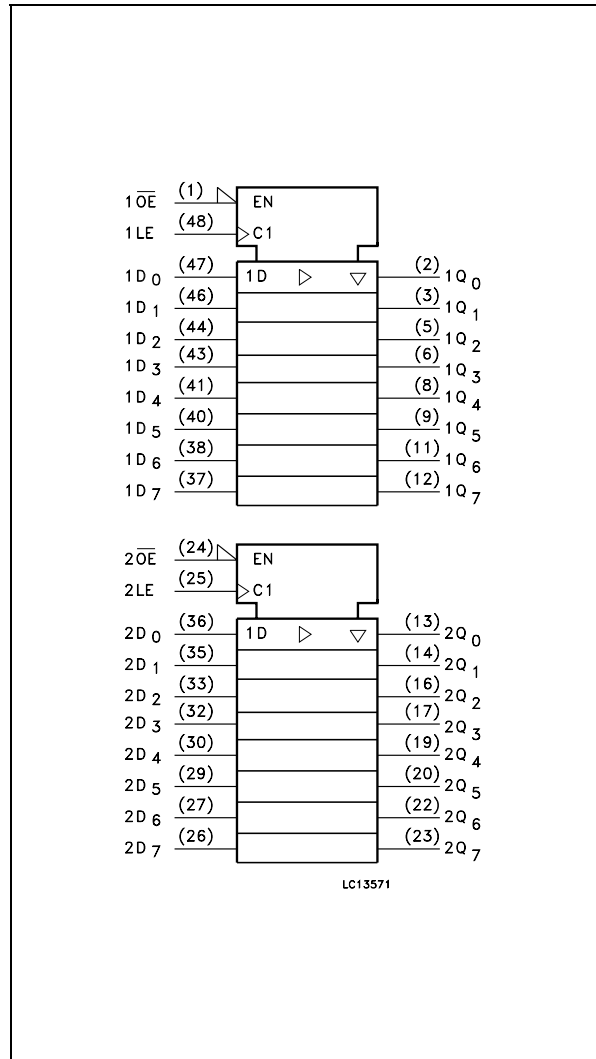
PIN No	SYMBOL	NAME AND FUNCTION
1	1OE	3 State Output Enable Input (Active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Q0 to 1Q7	3-State Outputs
13, 14, 16, 17, 19, 20, 22, 23	2Q0 to 2Q7	3-State Outputs
24	2OE	3 State Output Enable Input (Active LOW)
25	2LE	Latch Enable Input
36, 35, 33, 32, 30, 29, 27, 26	2D0 to 2D7	Data Inputs
47, 46, 44, 43, 41, 40, 38, 37	1D0 to 1D7	Data Inputs
48	1LE	Latch Enable Input
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	VCC	Positive Supply Voltage

TRUTH TABLE

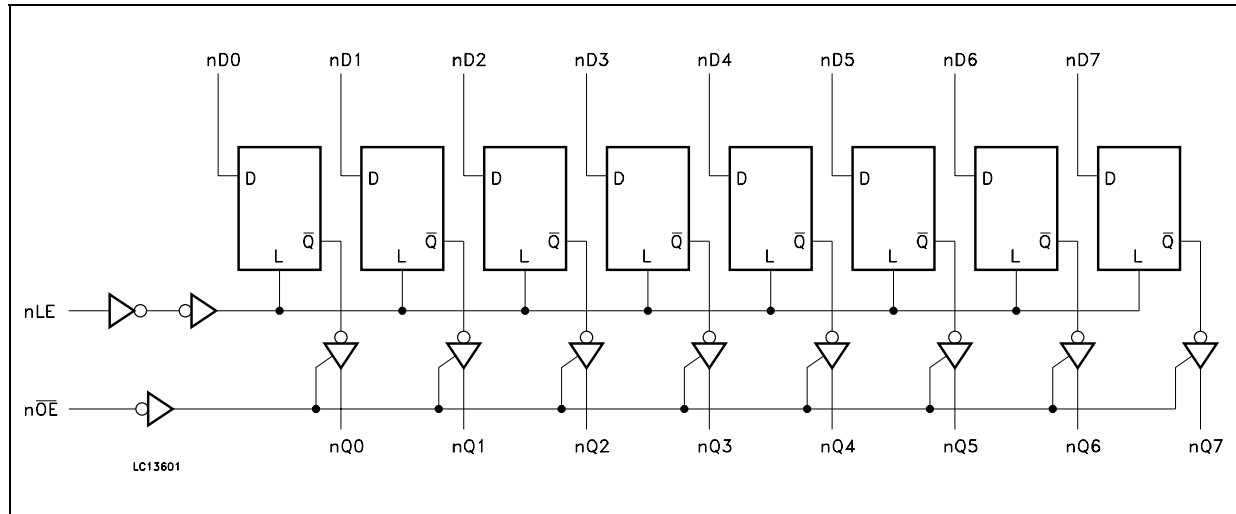
INPUTS			OUTPUT
\overline{OE}	LE	D	Q
H	X	X	Z
L	L	X	NO CHANGE *
L	H	L	L
L	H	H	H

X : Don't Care
 Z : High Impedance
 * : Q outputs are latched at the time when the LE input is taken low logic level.

IEC LOGIC SYMBOLS



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +4.6	V
V_I	DC Input Voltage	-0.5 to +4.6	V
V_O	DC Output Voltage (OFF State)	-0.5 to +4.6	V
V_O	DC Output Voltage (High or Low State) (note 1)	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	- 50	mA
I_{OK}	DC Output Diode Current (note 2)	- 50	mA
I_O	DC Output Current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Supply Pin	± 100	mA
P_D	Power Dissipation	400	mW
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}C$
T_L	Lead Temperature (10 sec)	300	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

1) I_O absolute maximum rating must be observed

2) $V_O < GND$, $V_O > V_{CC}$

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	1.65 to 3.6	V
V_I	Input Voltage	-0.3 to 3.6	V
V_O	Output Voltage (OFF State)	0 to 3.6	V
V_O	Output Voltage (High or Low State)	0 to V_{CC}	V
I_{OH} , I_{OL}	High or Low Level Output Current ($V_{CC} = 3.0$ to $3.6V$)	± 24	mA
I_{OH} , I_{OL}	High or Low Level Output Current ($V_{CC} = 2.3$ to $2.7V$)	± 12	mA
I_{OH} , I_{OL}	High or Low Level Output Current ($V_{CC} = 1.8V$)	± 4	mA
T_{op}	Operating Temperature	-55 to 125	$^{\circ}C$
dt/dv	Input Rise and Fall Time (note 1)	0 to 10	ns/V

1) V_{IN} from 0.8V to 2V at $V_{CC} = 3.0V$

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value				Unit
		V _{CC} (V)		-40 to 85 °C		-55 to 125 °C		
				Min.	Max.	Min.	Max.	
V _{IH}	High Level Input Voltage	1.65 to 1.95		0.65 V _{CC}		0.65 V _{CC}		V
		2.3 to 2.7		1.7		1.7		
		2.7 to 3.6		2.0		2.0		
V _{IL}	Low Level Input Voltage	1.65 to 1.95			0.35 V _{CC}		0.35 V _{CC}	V
		2.3 to 2.7			0.7		0.7	
		2.7 to 3.6			0.8		0.8	
V _{OH}	High Level Output Voltage	1.65 to 3.6	I _O =-100 μA	V _{CC} -0.2		V _{CC} -0.2		V
		1.65	I _O =-4 mA	1.2		1.2		
		2.3	I _O =-6 mA	2.0		2.0		
		2.3	I _O =-12 mA	1.7		1.7		
		2.7	I _O =-12 mA	2.2		2.2		
		3.0	I _O =-12 mA	2.4		2.4		
V _{OL}	Low Level Output Voltage	1.65 to 3.6	I _O =100 μA		0.2		0.2	V
		1.65	I _O =4 mA		0.45		0.45	
		2.3	I _O =6 mA		0.4		0.4	
		2.3	I _O =12 mA		0.7		0.7	
		2.7	I _O =12 mA		0.4		0.4	
		3.0	I _O =24 mA		0.55		0.55	
I _I	Input Leakage Current	3.6	V _I = 0 or 3.6V		± 5		± 5	μA
I _{IHOLD}	Bus Hold Input Leakage Current	1.65	V _I = 0.58 V	+ 25		+ 25		μA
		1.65	V _I = 1.07 V	- 25		- 25		
		2.3	V _I = 0.7 V	+ 45		+ 45		
		2.3	V _I = 1.7 V	- 45		- 45		
		3.0	V _I = 0.8 V	+ 75		+ 75		
		3.0	V _I = 2 V	- 75		- 75		
I _{off}	Power Off Leakage Current	0	V _I or V _O = 3.6V		10		20	μA
I _{OZ}	High Impedance Output Leakage Current	3.6	V _I = V _{IH} or V _{IL} V _O = 0 to V _{CC}		± 5		± 10	μA
I _{CC}	Quiescent Supply Current	3.6	V _I = V _{CC} or GND I _O = 0		20		40	μA
ΔI _{CC}	I _{CC} incr. per Input	3.0 to 3.6	V _{IH} = V _{CC} - 0.6V		500		750	μA

AC ELECTRICAL CHARACTERISTICS

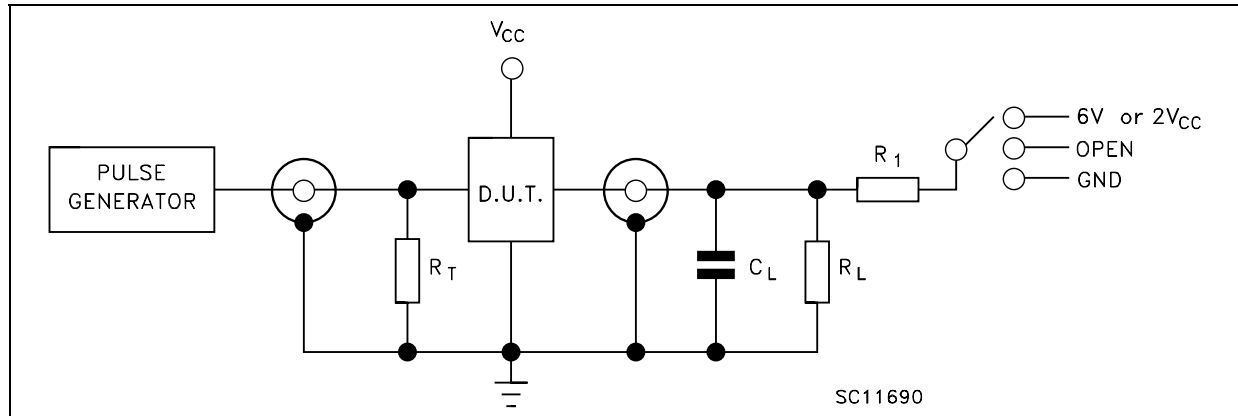
Symbol	Parameter	Test Condition				Value				Unit
		V _{CC} (V)	C _L (pF)	R _L (Ω)	t _s = t _r (ns)	-40 to 85 °C		-55 to 125 °C		
						Min.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay Time Dn to Qn	1.65 to 1.95	30	1000	2.0	1	6.5	1	6.5	ns
		2.3 to 2.7	30	500	2.0	1	4.5	1	4.5	
		2.7	50	500	2.5	1	4.3	1	4.3	
		3.0 to 3.6	50	500	2.5	1	3.6	1	3.6	
t _{PLH} t _{PHL}	Propagation Delay Time LE to Qn	1.65 to 1.95	30	1000	2.0	1	7.0	1	7.0	ns
		2.3 to 2.7	30	500	2.0	1	4.9	1	4.9	
		2.7	50	500	2.5	1	4.6	1	4.6	
		3.0 to 3.6	50	500	2.5	1	3.9	1	3.9	
t _{PZL} t _{PZH}	Output Enable Time	1.65 to 1.95	30	1000	2.0	1	8.5	1	8.5	ns
		2.3 to 2.7	30	500	2.0	1	6	1	6	
		2.7	50	500	2.5	1	5.7	1	5.7	
		3.0 to 3.6	50	500	2.5	1	4.7	1	4.7	
t _{PLZ} t _{PHZ}	Output Disable Time	1.65 to 1.95	30	1000	2.0	1	7	1	7	ns
		2.3 to 2.7	30	500	2.0	1	5.1	1	5.1	
		2.7	50	500	2.5	1	4.5	1	4.5	
		3.0 to 3.6	50	500	2.5	1	4.1	1	4.1	
t _s	Setup Time, HIGH or LOW level Dn to LE	1.65 to 1.95	30	1000	2.0	1		1		ns
		2.3 to 2.7	30	500	2.0	1		1		
		2.7	50	500	2.5	1		1		
		3.0 to 3.6	50	500	2.5	1.1		1.1		
t _h	Hold Time High or LOW level Dn to LE	1.65 to 1.95	30	1000	2.0	1.5		1.5		ns
		2.3 to 2.7	30	500	2.0	1.5		1.5		
		2.7	50	500	2.5	1.7		1.7		
		3.0 to 3.6	50	500	2.5	1.4		1.4		
t _w	LE Pulse Width, HIGH	1.65 to 1.95	30	1000	2.0	4		4		ns
		2.3 to 2.7	30	500	2.0	3.3		3.3		
		2.7	50	500	2.5	3.3		3.3		
		3.0 to 3.6	50	500	2.5	3.3		3.3		

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value			Unit
		V _{CC} (V)		T _A = 25 °C			
				Min.	Typ.	Max.	
C _{IN}	Input Capacitance Control Inputs	3.3	V _{IN} = V _{CC} or GND		3		pF
C _{IN}	Input Capacitance Data Inputs	3.3	V _{IN} = V _{CC} or GND		6		pF
C _{OUT}	Output Capacitance	3.3	V _{IN} = 0 to V _{CC}		7		pF
C _{PD}	Power Dissipation Capacitance Output enabled (note 1)	3.3	f _{IN} = 10MHz C _L = 50pF		19		pF
		2.5			16		
C _{PD}	Power Dissipation Capacitance Output disabled (note 1)	3.3	V _{IN} = 0 or V _{CC}		5		pF
		2.5			4		

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I_{CC(opr)} = C_{PD} × V_{CC} × f_{IN} + I_{CC}/16 (per circuit)

TEST CIRCUIT



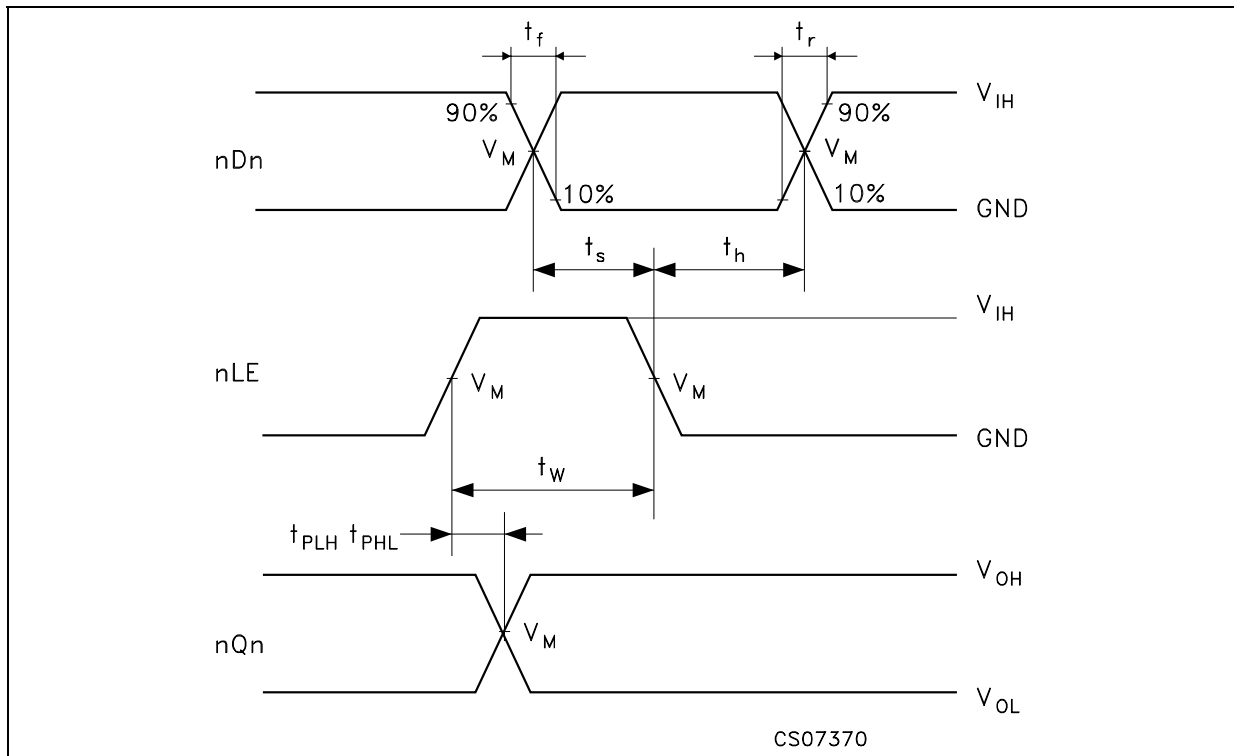
TEST	SWITCH
t _{PLH} , t _{PHL}	Open
t _{PZL} , t _{PLZ} (V _{CC} = 3.0 to 3.6V)	6V
t _{PZL} , t _{PLZ} (V _{CC} = 2.3 to 2.7V)	2V _{CC}
t _{PZH} , t _{PHZ}	GND

R_T = Z_{OUT} of pulse generator (typically 50Ω)

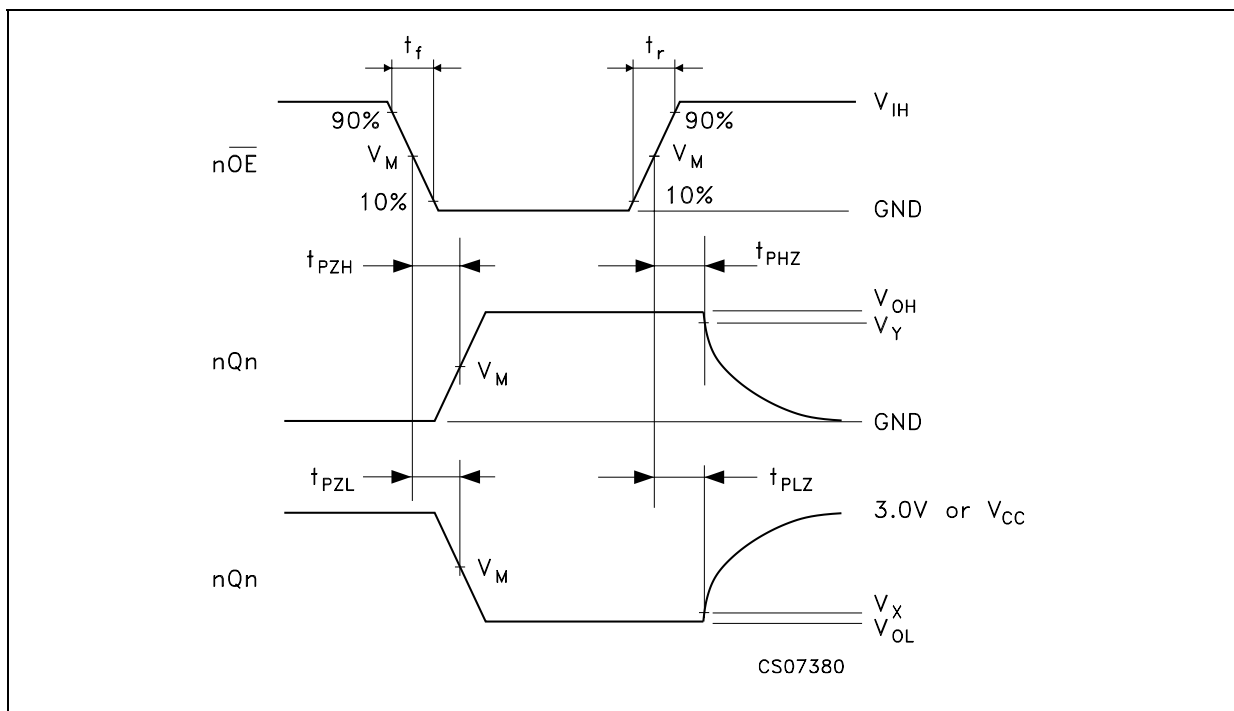
TEST CIRCUIT AND WAVEFORM SYMBOL VALUE

Symbol	V _{CC}			
	3.0 to 3.6V	2.7V	2.3 to 2.7V	1.65 to 1.95V
V _{IH}	2.7V	2.7V	V _{CC}	V _{CC}
V _M	1.5V	1.5V	V _{CC} /2	V _{CC} /2
V _X	V _{OL} + 0.3V	V _{OL} + 0.3V	V _{OL} + 0.15V	V _{OL} + 0.15V
V _Y	V _{OH} - 0.3V	V _{OH} - 0.3V	V _{OH} - 0.15V	V _{OH} - 0.15V
C _L	50pF	50pF	30pF	30pF
R _L = R ₁	500Ω	500Ω	500Ω	1000Ω
t _r = t _f	<2.5ns	<2.5ns	<2.0ns	<2.0ns

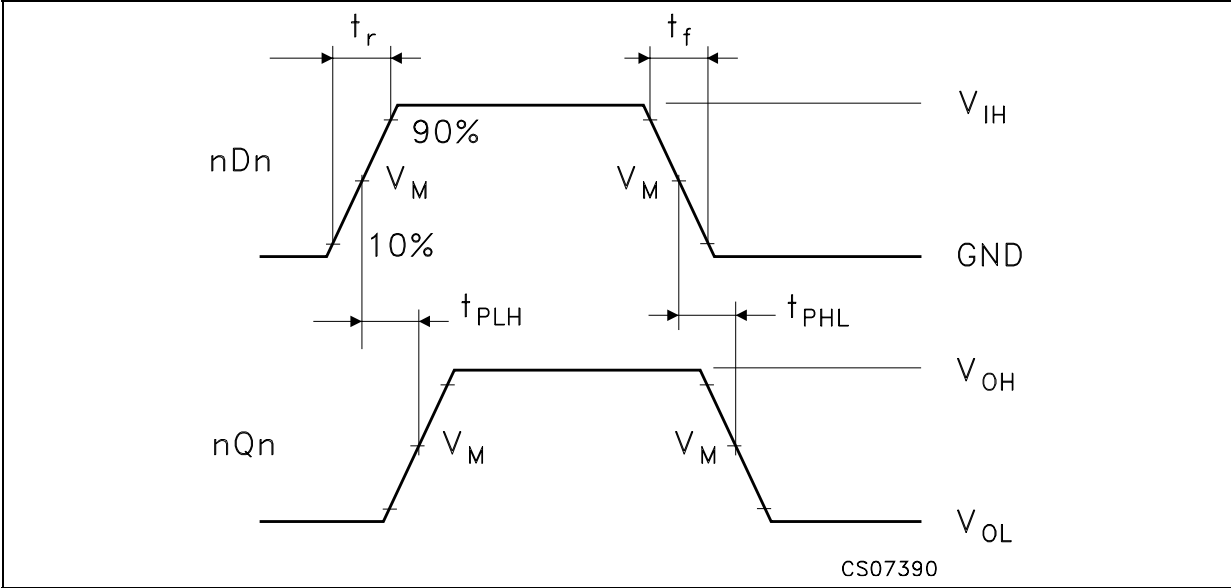
WAVEFORM 1 : LE TO Qn PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn TO LE SETUP AND HOLD TIMES (f=1MHz; 50% duty cycle)



WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIME (f=1MHz; 50% duty cycle)



WAVEFORM 3 : PROPAGATION DELAY TIME (f=1MHz; 50% duty cycle)



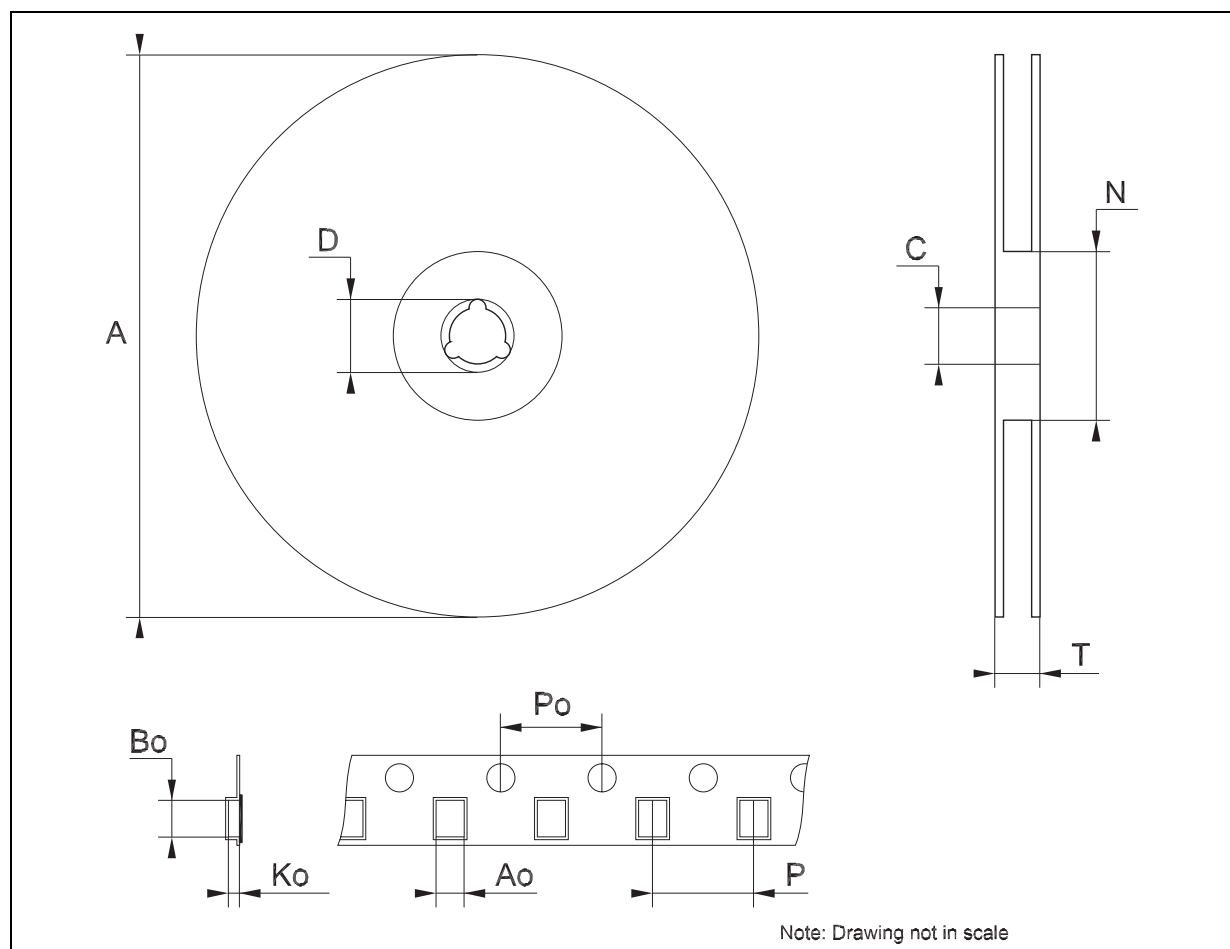
TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.17		0.27	0.0067		0.011
c	0.09		0.20	0.0035		0.0079
D	12.4		12.6	0.488		0.496
E		8.1 BSC			0.318 BSC	
E1	6.0		6.2	0.236		0.244
e		0.5 BSC			0.0197 BSC	
K	0°		8°	0°		8°
L	0.50		0.75	0.020		0.030



Tape & Reel TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	8.7		8.9	0.343		0.350
Bo	13.1		13.3	0.516		0.524
Ko	1.5		1.7	0.059		0.067
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2002 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© <http://www.st.com>

