# CD4066B
# CMOS QUAD BILATERAL SWITCH

- **15-V Digital or ±7.5-V Peak-to-Peak Switching**
- **125-$\Omega$ Typical On-State Resistance for 15-V Operation**
- **Switch On-State Resistance Matched to Within 5 $\Omega$ Over 15-V Signal-Input Range**
- **On-State Resistance Flat Over Full Peak-to-Peak Signal Range**
- **High On/Off Output-Voltage Ratio: 80 dB Typical at $f_{is}$ = 10 kHz, $R_L$ = 1 k$\Omega$**
- **High Degree of Linearity: <0.5% Distortion Typical at $f_{is}$ = 1 kHz, $V_{is}$ = 5 V p-p, $V_{DD} - V_{SS} \geq$ 10 V, $R_L$ = 10 k$\Omega$**
- **Extremely Low Off-State Switch Leakage, Resulting in Very Low Offset Current and High Effective Off-State Resistance: 10 pA Typical at $V_{DD} - V_{SS}$ = 10 V, $T_A$ = 25°C**
- **Extremely High Control Input Impedance (Control Circuit Isolated From Signal Circuit): $10^{12}$ $\Omega$ Typical**
- **Low Crosstalk Between Switches: –50 dB Typical at $f_{is}$ = 8 MHz, $R_L$ = 1 k$\Omega$**

- **Matched Control-Input to Signal-Output Capacitance: Reduces Output Signal Transients**
- **Frequency Response, Switch On = 40 MHz Typical**
- **100% Tested for Quiescent Current at 20 V**
- **5-V, 10-V, and 15-V Parametric Ratings**
- **Meets All Requirements of JEDEC Tentative Standard No. 13-B,** *Standard Specifications for Description of "B" Series CMOS Devices*
- **Applications:**
  - **Analog Signal Switching/Multiplexing: Signal Gating, Modulator, Squelch Control, Demodulator, Chopper, Commutating Switch**
  - **Digital Signal Switching/Multiplexing**
  - **Transmission-Gate Logic Implementation**
  - **Analog-to-Digital and Digital-to-Analog Conversion**
  - **Digital Control of Frequency, Impedance, Phase, and Analog-Signal Gain**

### E, F, M, NS, OR PW PACKAGE
### (TOP VIEW)

| | | | |
|---|---|---|---|
| SIG A IN/OUT | 1 | 14 | $V_{DD}$ |
| SIG A OUT/IN | 2 | 13 | CONTROL A |
| SIG B OUT/IN | 3 | 12 | CONTROL D |
| SIG B IN/OUT | 4 | 11 | SIG D IN/OUT |
| CONTROL B | 5 | 10 | SIG D OUT/IN |
| CONTROL C | 6 | 9 | SIG C OUT/IN |
| $V_{SS}$ | 7 | 8 | SIG C IN/OUT |
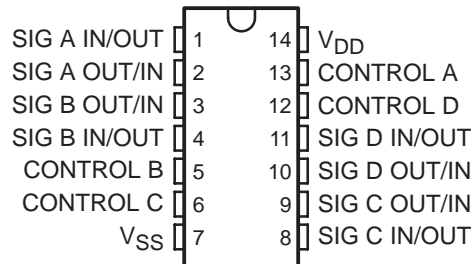
## description/ordering information

The CD4066B is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with the CD4016B, but exhibits a much lower on-state resistance. In addition, the on-state resistance is relatively constant over the full signal-input range.

The CD4066B consists of four bilateral switches, each with independent controls. Both the p and the n devices in a given switch are biased on or off simultaneously by the control signal. As shown in Figure 1, the well of the n-channel device on each switch is tied to either the input (when the switch is on) or to $V_{SS}$ (when the switch is off). This configuration eliminates the variation of the switch-transistor threshold voltage with input signal and, thus, keeps the on-state resistance low over the full operating-signal range.

The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage and more constant on-state impedance over the input-signal range. However, for sample-and-hold applications, the CD4016B is recommended.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## TEXAS INSTRUMENTS

## description/ordering information (continued)

### ORDERING INFORMATION

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –55°C to 125°C | CDIP – F | Tube of 25 | CD4066BF3A | CD4066BF3A |
| | PDIP – E | Tube of 25 | CD4066BE | CD4066BE |
| | SOIC – M | Tube of 50 | CD4066BM | CD4066BM |
| | | Reel of 2500 | CD4066BM96 | |
| | | Reel of 250 | CD4066BMT | |
| | SOP – NS | Reel of 2000 | CD4066BNSR | CD4066B |
| | TSSOP – PW | Tube of 90 | CD4066BPW | CM066B |
| | | Reel of 2000 | CD4066BPWR | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
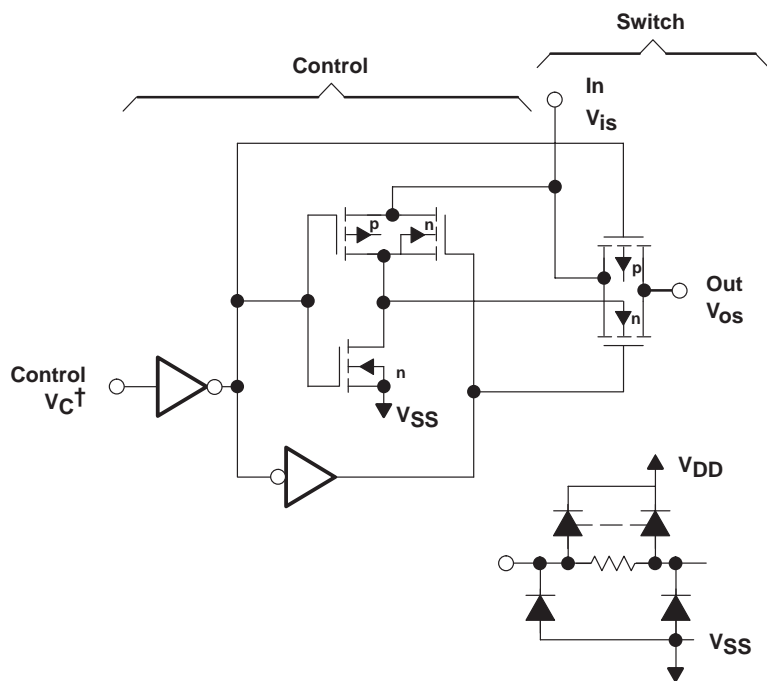


† All control inputs are protected by the CMOS protection network.
NOTES:   A.   All p substrates are connected to $V_{DD}$.
        B.   Normal operation control-line biasing: switch on (logic 1), $V_C = V_{DD}$; switch off (logic 0), $V_C = V_{SS}$
        C.   Signal-level range: $V_{SS} \leq V_{is} \leq V_{DD}$

**92CS-29113**

**Figure 1. Schematic Diagram of One-of-Four Identical Switches and Associated Control Circuitry**

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## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

DC supply-voltage range, $V_{DD}$ (voltages referenced to $V_{SS}$ terminal) . . . . . . . . . . . . . . . . . . . . –0.5 V to 20 V
Input voltage range, $V_{is}$ (all inputs) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . –0.5 V to $V_{DD}$ + 0.5 V
DC input current, $I_{IN}$ (any one input) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . ±10 mA
Package thermal impedance, $\theta_{JA}$ (see Note 1): E package . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 80°C/W
                         M package . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 86°C/W
                         NS package . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 76°C/W
                         PW package . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 113°C/W
Lead temperature (during soldering):
   At distance 1/16 ± 1/32 inch (1,59 ± 0,79 mm) from case for 10 s max . . . . . . . . . . . . . . . . . . . . . . . 265°C
Storage temperature range, $T_{stg}$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
  functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
  implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1:   The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions

|        |                                |  MIN | MAX | UNIT |
|--------|--------------------------------|------|-----|------|
| $V_{DD}$ | Supply voltage               |   3  |  18 |  V   |
| $T_A$  | Operating free-air temperature |  –55 | 125 |  °C  |

# CD4066B
## CMOS QUAD BILATERAL SWITCH

## electrical characteristics

| PARAMETER | | TEST CONDITIONS | $V_{IN}$ (V) | $V_{DD}$ (V) | LIMITS AT INDICATED TEMPERATURES | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | −55°C | −40°C | 85°C | 125°C | 25°C | | |
| | | | | | | | | | TYP | MAX | |
| $I_{DD}$ | Quiescent device current | | 0, 5 | 5 | 0.25 | 0.25 | 7.5 | 7.5 | 0.01 | 0.25 | μA |
| | | | 0, 10 | 10 | 0.5 | 0.5 | 15 | 15 | 0.01 | 0.5 | |
| | | | 0, 15 | 15 | 1 | 1 | 30 | 30 | 0.01 | 1 | |
| | | | 0, 20 | 20 | 5 | 5 | 150 | 150 | 0.02 | 5 | |
| **Signal Inputs ($V_{is}$) and Outputs ($V_{os}$)** | | | | | | | | | | | |
| $r_{on}$ | On-state resistance (max) | $V_C = V_{DD}$, $R_L$ = 10 kΩ returned to $\dfrac{(V_{DD} - V_{SS})}{2}$, $V_{is} = V_{SS}$ to $V_{DD}$ | | 5 | 800 | 850 | 1200 | 1300 | 470 | 1050 | Ω |
| | | | | 10 | 310 | 330 | 500 | 550 | 180 | 400 | |
| | | | | 15 | 200 | 210 | 300 | 320 | 125 | 240 | |
| $\Delta r_{on}$ | On-state resistance difference between any two switches | $R_L$ = 10 kΩ, $V_C = V_{DD}$ | | 5 | | | | | 15 | | Ω |
| | | | | 10 | | | | | 10 | | |
| | | | | 15 | | | | | 5 | | |
| THD | Total harmonic distortion | $V_C = V_{DD}$ = 5 V, $V_{SS}$ = −5 V, $V_{is(p-p)}$ = 5 V (sine wave centered on 0 V), $R_L$ = 10 kΩ, $f_{is}$ = 1-kHz sine wave | | | | | | | 0.4 | | % |
| | −3-dB cutoff frequency (switch on) | $V_C = V_{DD}$ = 5 V, $V_{SS}$ = −5 V, $V_{is(p-p)}$ = 5 V (sine wave centered on 0 V), $R_L$ = 1 kΩ | | | | | | | 40 | | MHz |
| | −50-dB feedthrough frequency (switch off) | $V_C = V_{SS}$ = −5 V, $V_{is(p-p)}$ = 5 V (sine wave centered on 0 V), $R_L$ = 1 kΩ | | | | | | | 1 | | MHz |
| $I_{is}$ | Input/output leakage current (switch off) (max) | $V_C$ = 0 V, $V_{is}$ = 18 V, $V_{os}$ = 0 V; and $V_C$ = 0 V, $V_{is}$ = 0 V, $V_{os}$ = 18 V | 18 | | ±0.1 | ±0.1 | ±1 | ±1 | ±10$^{-5}$ | ±0.1 | μA |
| | −50-dB crosstalk frequency | $V_C(A) = V_{DD}$ = 5 V, $V_C(B) = V_{SS}$ = −5 V, $V_{is}(A)$ = 5 $V_{p-p}$, 50-Ω source, $R_L$ = 1 kΩ | | | | | | | 8 | | MHz |
| $t_{pd}$ | Propagation delay (signal input to signal output) | $R_L$ = 200 kΩ, $V_C = V_{DD}$, $V_{SS}$ = GND, $C_L$ = 50 pF, $V_{is}$ = 10 V (square wave centered on 5 V), $t_r$, $t_f$ = 20 ns | | 5 | | | | | 20 | 40 | ns |
| | | | | 10 | | | | | 10 | 20 | |
| | | | | 15 | | | | | 7 | 15 | |
| $C_{is}$ | Input capacitance | $V_{DD}$ = 5 V, $V_C = V_{SS}$ = −5 V | | | | | | | 8 | | pF |
| $C_{os}$ | Output capacitance | $V_{DD}$ = 5 V, $V_C = V_{SS}$ = −5 V | | | | | | | 8 | | pF |
| $C_{ios}$ | Feedthrough | $V_{DD}$ = 5 V, $V_C = V_{SS}$ = −5 V | | | | | | | 0.5 | | pF |

## electrical characteristics (continued)

| CHARACTERISTIC | | TEST CONDITIONS | $V_{DD}$ (V) | LIMITS AT INDICATED TEMPERATURES | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | −55°C | −40°C | 85°C | 125°C | 25°C | | |
| | | | | | | | | TYP | MAX | |
| **Control ($V_C$)** | | | | | | | | | | |
| $V_{ILC}$ | Control input, low voltage (max) | $\|I_{is}\| < 10\ \mu A$, $V_{is} = V_{SS}$, $V_{OS} = V_{DD}$, and $V_{is} = V_{DD}$, $V_{OS} = V_{SS}$ | 5 | 1 | 1 | 1 | 1 | | 1 | V |
| | | | 10 | 2 | 2 | 2 | 2 | | 2 | |
| | | | 15 | 2 | 2 | 2 | 2 | | 2 | |
| $V_{IHC}$ | Control input, high voltage | See Figure 6 | 5 | 3.5 (MIN) | | | | | | V |
| | | | 10 | 7 (MIN) | | | | | | |
| | | | 15 | 11 (MIN) | | | | | | |
| $I_{IN}$ | Input current (max) | $V_{is} \leq V_{DD}$, $V_{DD} - V_{SS} = 18\ V$, $V_{CC} \leq V_{DD} - V_{SS}$ | 18 | ±0.1 | ±0.1 | ±1 | ±1 | ±$10^{-5}$ | ±0.1 | μA |
| | Crosstalk (control input to signal output) | $V_C = 10\ V$ (square wave), $t_r, t_f = 20\ ns$, $R_L = 10\ k\Omega$ | 10 | | | | | | 50 | mV |
| | Turn-on and turn-off propagation delay | $V_{IN} = V_{DD}$, $t_r, t_f = 20\ ns$, $C_L = 50\ pF$, $R_L = 1\ k\Omega$ | 5 | | | | | 35 | 70 | ns |
| | | | 10 | | | | | 20 | 40 | |
| | | | 15 | | | | | 15 | 30 | |
| | Maximum control input repetition rate | $V_{is} = V_{DD}$, $V_{SS} = GND$, $R_L = 1\ k\Omega$ to GND, $C_L = 50\ pF$, $V_C = 10\ V$ (square wave centered on 5 V), $t_r, t_f = 20\ ns$, $V_{OS} = 1/2\ V_{OS}$ at 1 kHz | 5 | | | | | 6 | | MHz |
| | | | 10 | | | | | 9 | | |
| | | | 15 | | | | | 9.5 | | |
| $C_I$ | Input capacitance | | | | | | | 5 | 7.5 | pF |

## switching characteristics

| $V_{DD}$ (V) | SWITCH INPUT | | | | | | SWITCH OUTPUT, $V_{OS}$ (V) | |
|---|---|---|---|---|---|---|---|---|
| | $V_{is}$ (V) | $I_{is}$ (mA) | | | | | | |
| | | −55°C | −40°C | 25°C | 85°C | 125°C | MIN | MAX |
| 5 | 0 | 0.64 | 0.61 | 0.51 | 0.42 | 0.36 | | 0.4 |
| 5 | 5 | −0.64 | −0.61 | −0.51 | −0.42 | −0.36 | 4.6 | |
| 10 | 0 | 1.6 | 1.5 | 1.3 | 1.1 | 0.9 | | 0.5 |
| 10 | 10 | −1.6 | −1.5 | −1.3 | −1.1 | −0.9 | 9.5 | |
| 15 | 0 | 4.2 | 4 | 3.4 | 2.8 | 2.4 | | 1.5 |
| 15 | 15 | −4.2 | −4 | −3.4 | −2.8 | −2.4 | 13.5 | |

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## TYPICAL CHARACTERISTICS
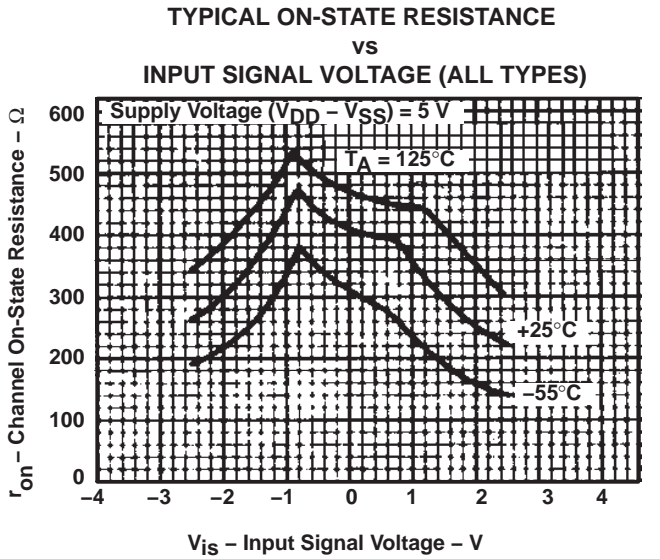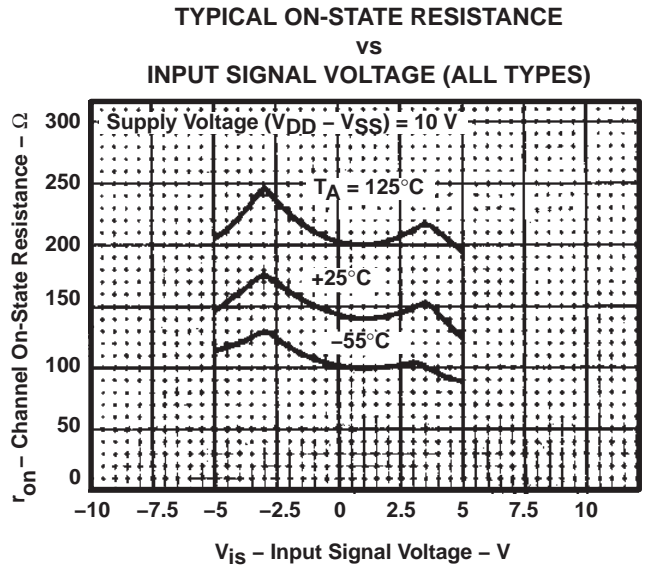
**TYPICAL ON-STATE RESISTANCE
vs
INPUT SIGNAL VOLTAGE (ALL TYPES)**



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**Figure 2**

**TYPICAL ON-STATE RESISTANCE
vs
INPUT SIGNAL VOLTAGE (ALL TYPES)**



92CS-27327RI

**Figure 3**

**TYPICAL ON-STATE RESISTANCE
vs
INPUT SIGNAL VOLTAGE (ALL TYPES)**



92CS-27329RI

**Figure 4**

**TYPICAL ON-STATE RESISTANCE
vs
INPUT SIGNAL VOLTAGE (ALL TYPES)**



92CS-27330RI

**Figure 5**

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6
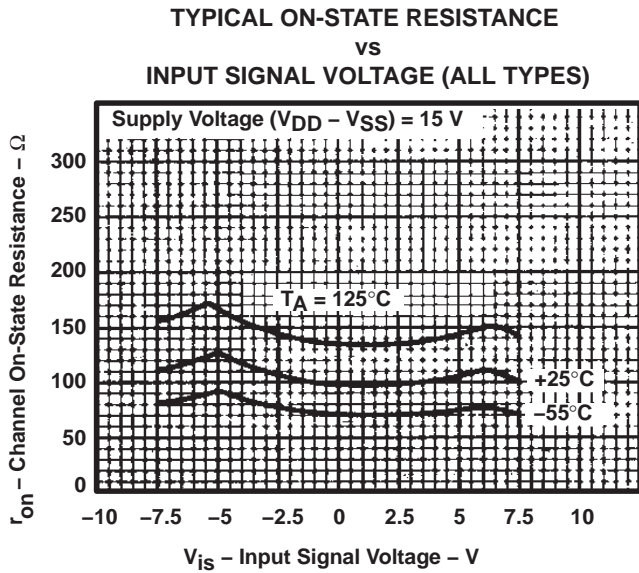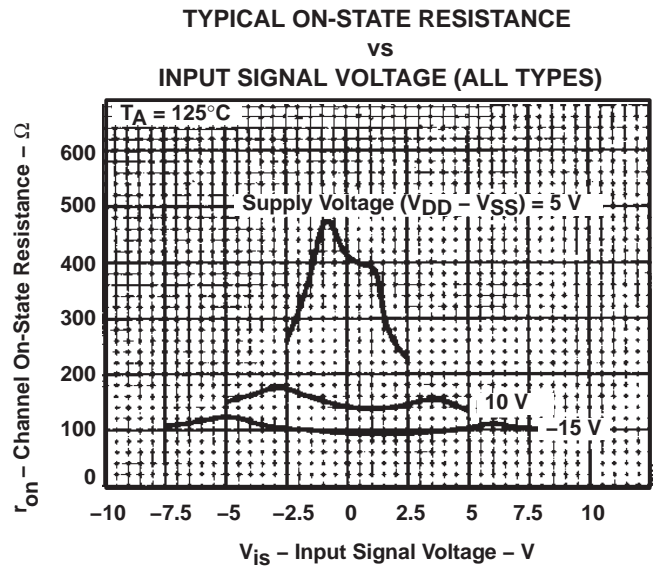
## TYPICAL CHARACTERISTICS



$$r_{on} = \frac{|V_{is} - V_{os}|}{|I_{is}|}$$
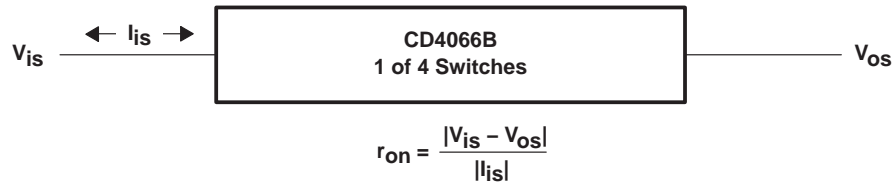
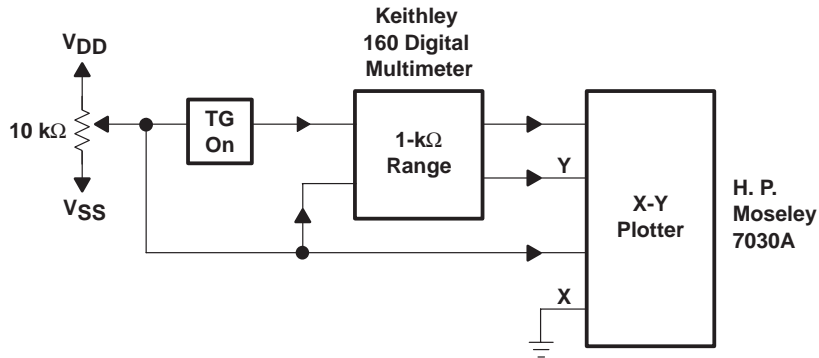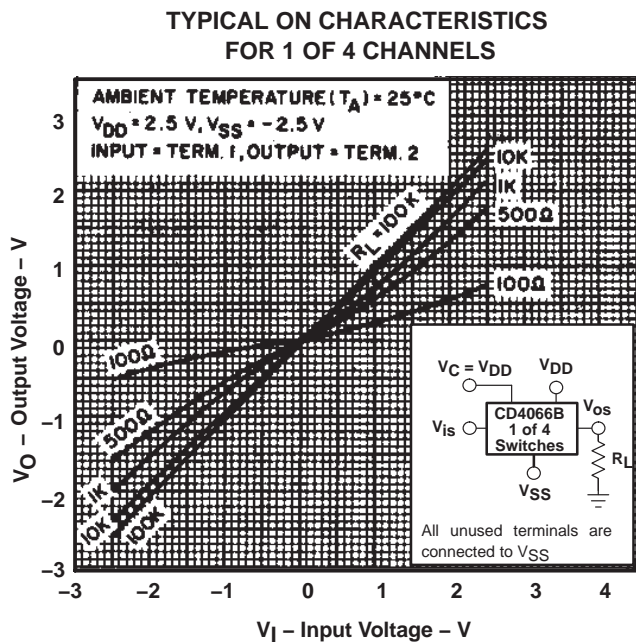**92CS-30966**

**Figure 6. Determination of $r_{on}$ as a Test Condition for Control-Input High-Voltage ($V_{IHC}$) Specification**



**92CS-22716**

**Figure 7. Channel On-State Resistance Measurement Circuit**

**TYPICAL ON CHARACTERISTICS**
**FOR 1 OF 4 CHANNELS**



**92CS-30919**

**Figure 8**

**POWER DISSIPATION PER PACKAGE**
**vs**
**SWITCHING FREQUENCY**



**92C-30920**

**Figure 9**

![Texas Instruments logo] **TEXAS INSTRUMENTS**

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## TYPICAL CHARACTERISTICS



92CS-30921

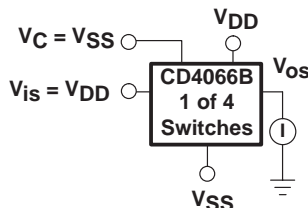Measured on Boonton capacitance bridge, model 75a (1 MHz); test-fixture capacitance nulled out.

**Figure 10. Typical On Characteristics for One of Four Channels**



92CS-30922

All unused terminals are connected to $V_{SS}$.

**Figure 11. Off-Switch Input or Output Leakage**
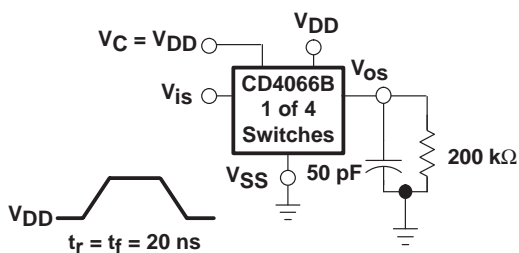


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All unused terminals are connected to $V_{SS}$.

**Figure 12. Propagation Delay Time Signal Input ($V_{is}$) to Signal Output ($V_{os}$)**
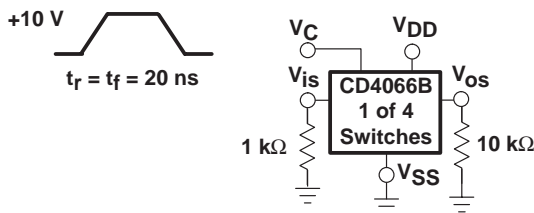


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All unused terminals are connected to $V_{SS}$.

**Figure 13. Crosstalk-Control Input to Signal Output**

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## TYPICAL CHARACTERISTICS
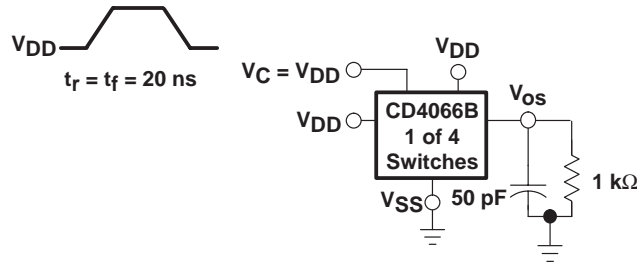


NOTES: A. All unused terminals are connected to $V_{SS}$.
       B. Delay is measured at $V_{OS}$ level of +10% from ground (turn-on) or on-state output level (turn-off).

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**Figure 14. Propagation Delay, $t_{PLH}$, $t_{PHL}$ Control-Signal Output**
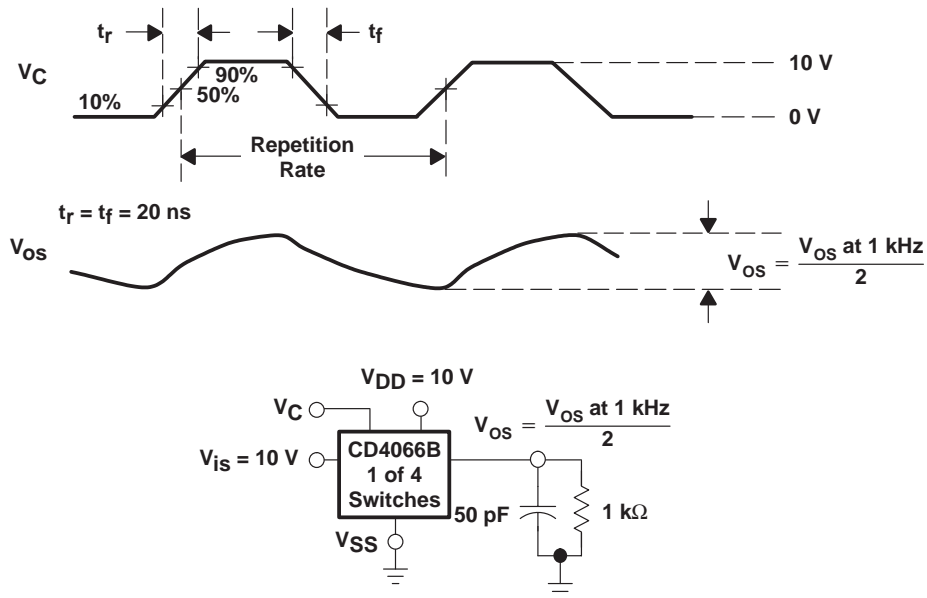


All unused terminals are connected to $V_{SS}$.

**92CS-30925**

**Figure 15. Maximum Allowable Control-Input Repetition Rate**

## TYPICAL CHARACTERISTICS
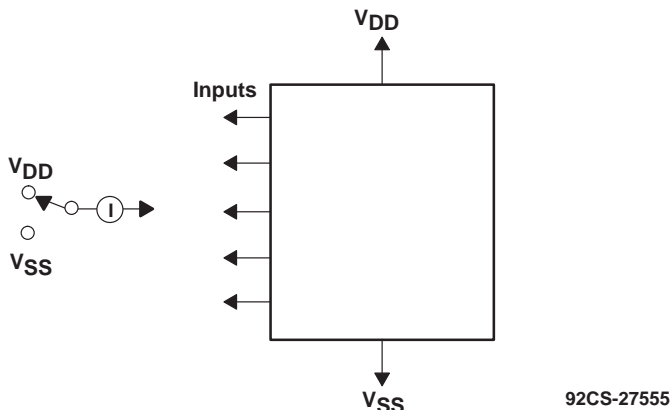


Measure inputs sequentially to both $V_{DD}$ and $V_{SS}$. Connect all unused inputs to either $V_{DD}$ or $V_{SS}$. Measure control inputs only.

**Figure 16. Input Leakage-Current Test Circuit**
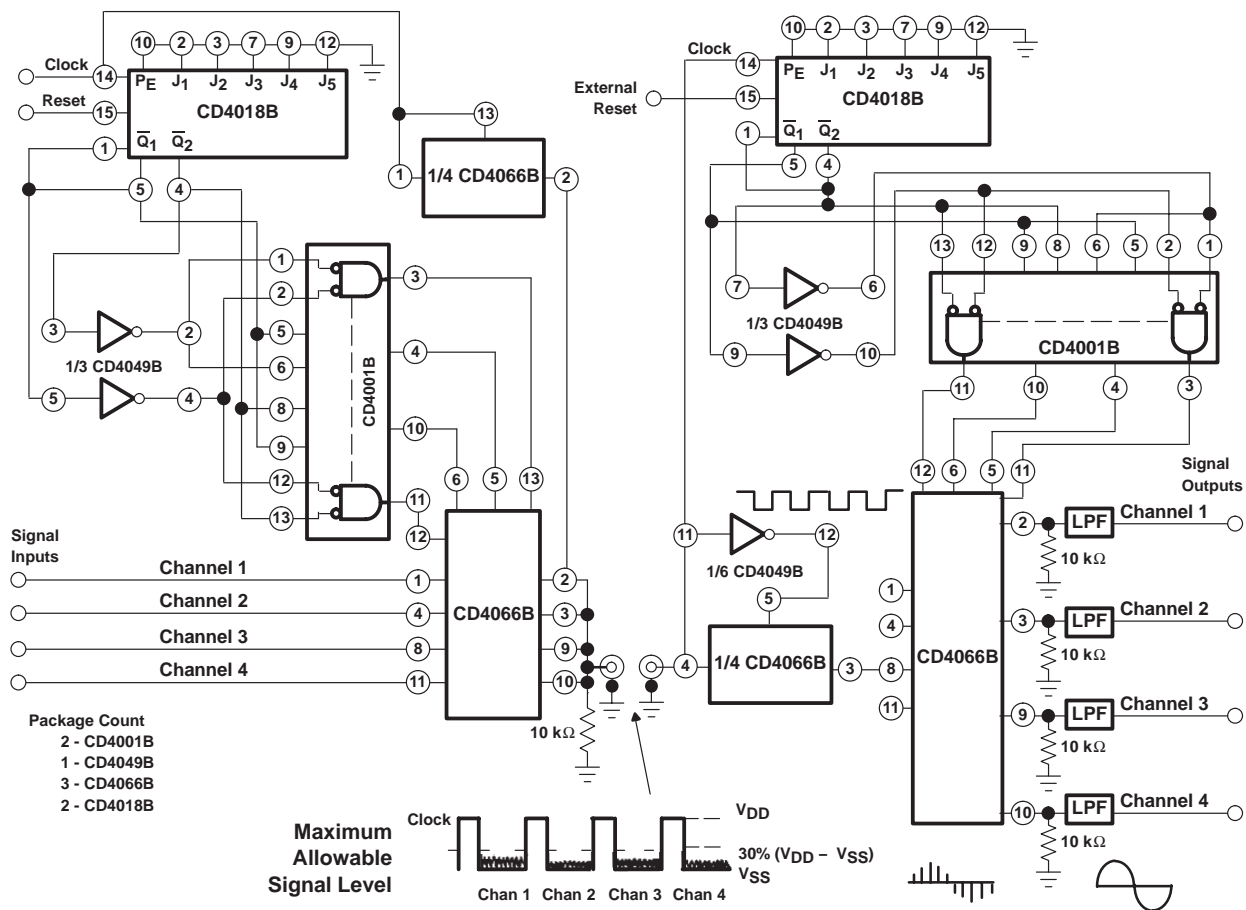


**Figure 17. Four-Channel PAM Multiplex System Diagram**

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**TYPICAL CHARACTERISTICS**
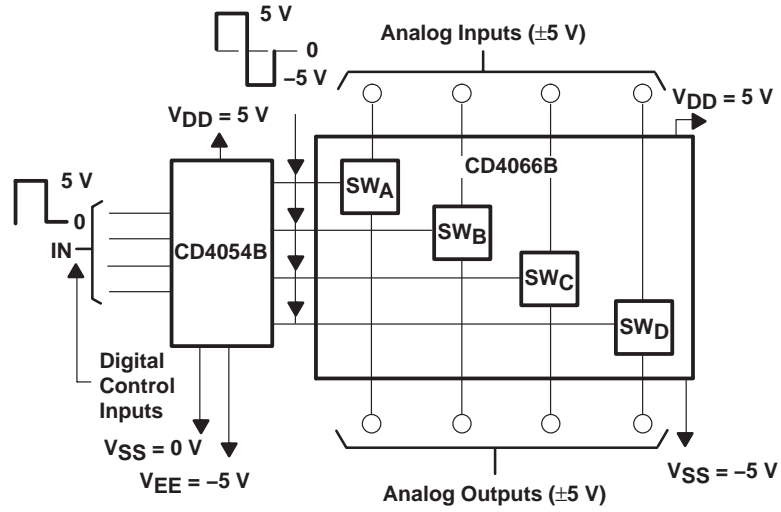


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**Figure 18. Bidirectional Signal Transmission Via Digital Control Logic**

**APPLICATION INFORMATION**

In applications that employ separate power sources to drive $V_{DD}$ and the signal inputs, the $V_{DD}$ current capability should exceed $V_{DD}/R_L$ ($R_L$ = effective external load of the four CD4066B bilateral switches). This provision avoids any permanent current flow or clamp action on the $V_{DD}$ supply when power is applied or removed from the CD4066B.

In certain applications, the external load-resistor current can include both $V_{DD}$ and signal-line components. To avoid drawing $V_{DD}$ current when switch current flows into terminals 1, 4, 8, or 11, the voltage drop across the bidirectional switch must not exceed 0.8 V (calculated from $r_{on}$ values shown).

No $V_{DD}$ current will flow through $R_L$ if the switch current flows into terminals 2, 3, 9, or 10.

# PACKAGE OPTION ADDENDUM

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| CD4066BE | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | Contact TI Distributor or Sales Office |
| CD4066BEE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | Contact TI Distributor or Sales Office |
| CD4066BF | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | Purchase Samples |
| CD4066BF3A | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | Purchase Samples |
| CD4066BF3AS2283 | OBSOLETE | CDIP | J | 14 | | TBD | Call TI | Call TI | Samples Not Available |
| CD4066BF3AS2534 | OBSOLETE | CDIP | J | 14 | | TBD | Call TI | Call TI | Samples Not Available |
| CD4066BM | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| CD4066BM96 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Contact TI Distributor or Sales Office |
| CD4066BM96E4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Contact TI Distributor or Sales Office |
| CD4066BM96G4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Contact TI Distributor or Sales Office |
| CD4066BME4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| CD4066BMG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| CD4066BMT | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| CD4066BMTE4 | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| CD4066BMTG4 | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| CD4066BNSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Contact TI Distributor or Sales Office |
| CD4066BNSRE4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Contact TI Distributor or Sales Office |
| CD4066BNSRG4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Contact TI Distributor or Sales Office |

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/ Ball Finish | MSL Peak Temp [3] | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| CD4066BPW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| CD4066BPWE4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| CD4066BPWG4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| CD4066BPWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Contact TI Distributor or Sales Office |
| CD4066BPWRE4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Contact TI Distributor or Sales Office |
| CD4066BPWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Contact TI Distributor or Sales Office |
| JM38510/05852BCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | Purchase Samples |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF CD4066B, CD4066B-MIL :**

● Catalog: CD4066B

● Military: CD4066B-MIL

NOTE: Qualified Version Definitions:

    ● Catalog - TI's standard catalog product

    ● Military - QML certified for Military and Defense Applications

# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**



Reel Diameter

Reel Width (W1)

**TAPE DIMENSIONS**



| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------|--------------|-----------------|------|-----|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD4066BM96 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| CD4066BM96 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| CD4066BMT | SOIC | D | 14 | 250 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| CD4066BNSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| CD4066BPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD4066BM96 | SOIC | D | 14 | 2500 | 346.0 | 346.0 | 33.0 |
| CD4066BM96 | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| CD4066BMT | SOIC | D | 14 | 250 | 346.0 | 346.0 | 33.0 |
| CD4066BNSR | SO | NS | 14 | 2000 | 346.0 | 346.0 | 33.0 |
| CD4066BPWR | TSSOP | PW | 14 | 2000 | 346.0 | 346.0 | 29.0 |

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| [A] | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | —— | —— | —— | —— |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

B

14                    8

0.065 (1,65)
0.045 (1,14)

1                    7

C

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

[A]

0°–15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES:  A.  All linear dimensions are in inches (millimeters).
B.  This drawing is subject to change without notice.
C.  This package is hermetically sealed with a ceramic lid using glass frit.
D.  Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E.  Falls within MIL STD 1835 GDIP1—T14, GDIP1—T16, GDIP1—T18 and GDIP1—T20.

**N (R−PDIP−T\*\*)**            **PLASTIC DUAL−IN−LINE PACKAGE**

16 PINS SHOWN

| PINS \*\* / DIM | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS−001 VARIATION | AA | BB | AC | AD |

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14)

0.045 (1,14) / 0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

0.010 (0,25) M

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM
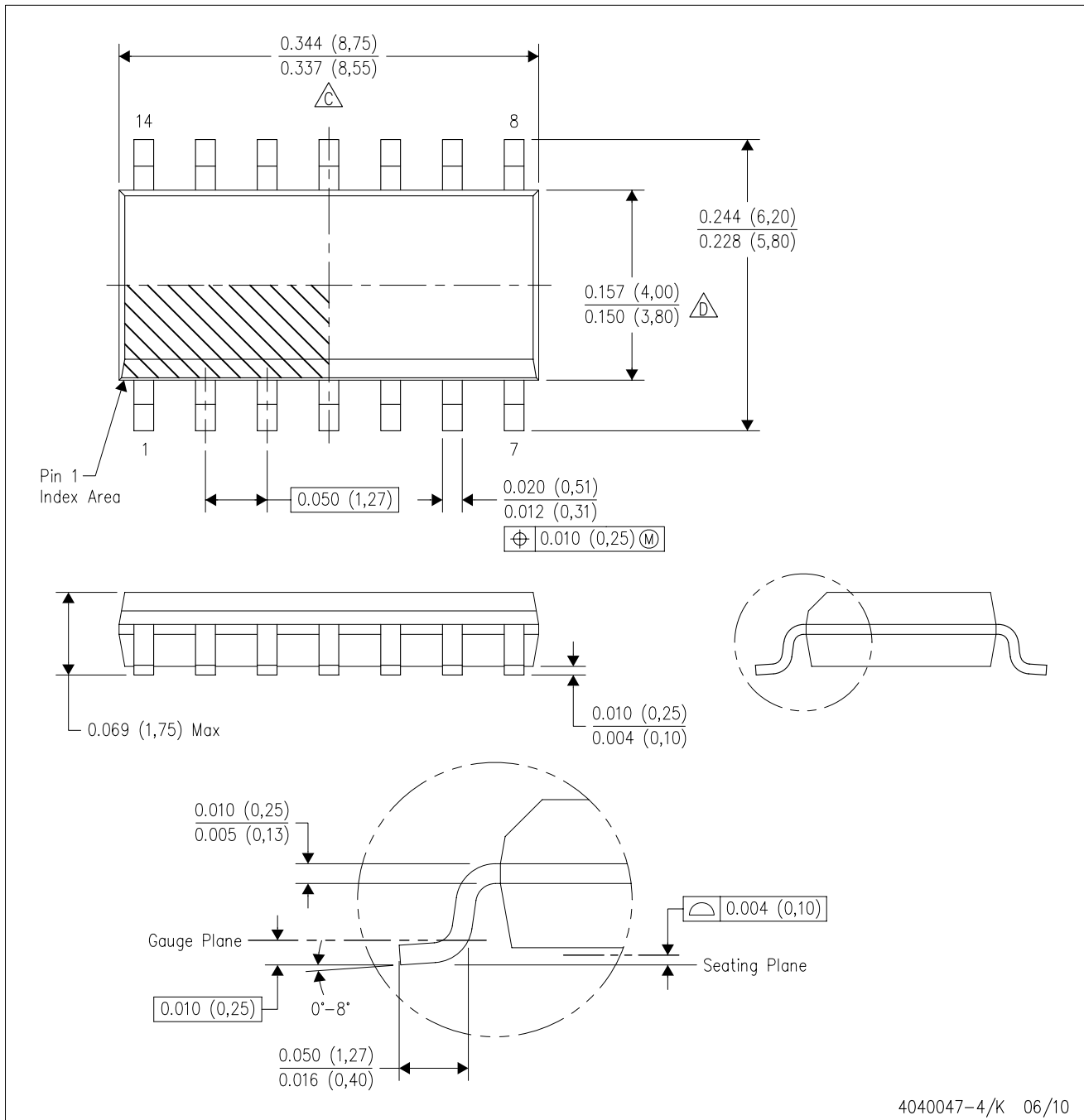
0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option

4040049/E  12/2002

NOTES:  A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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D (R−PDSO−G14)                              PLASTIC SMALL−OUTLINE PACKAGE



0.344 (8,75)
0.337 (8,55)
△C△

14                                    8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)  △D△

1                                    7

Pin 1
Index Area

0.050 (1,27)        0.020 (0,51)
                    0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)        0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−4/K  06/10
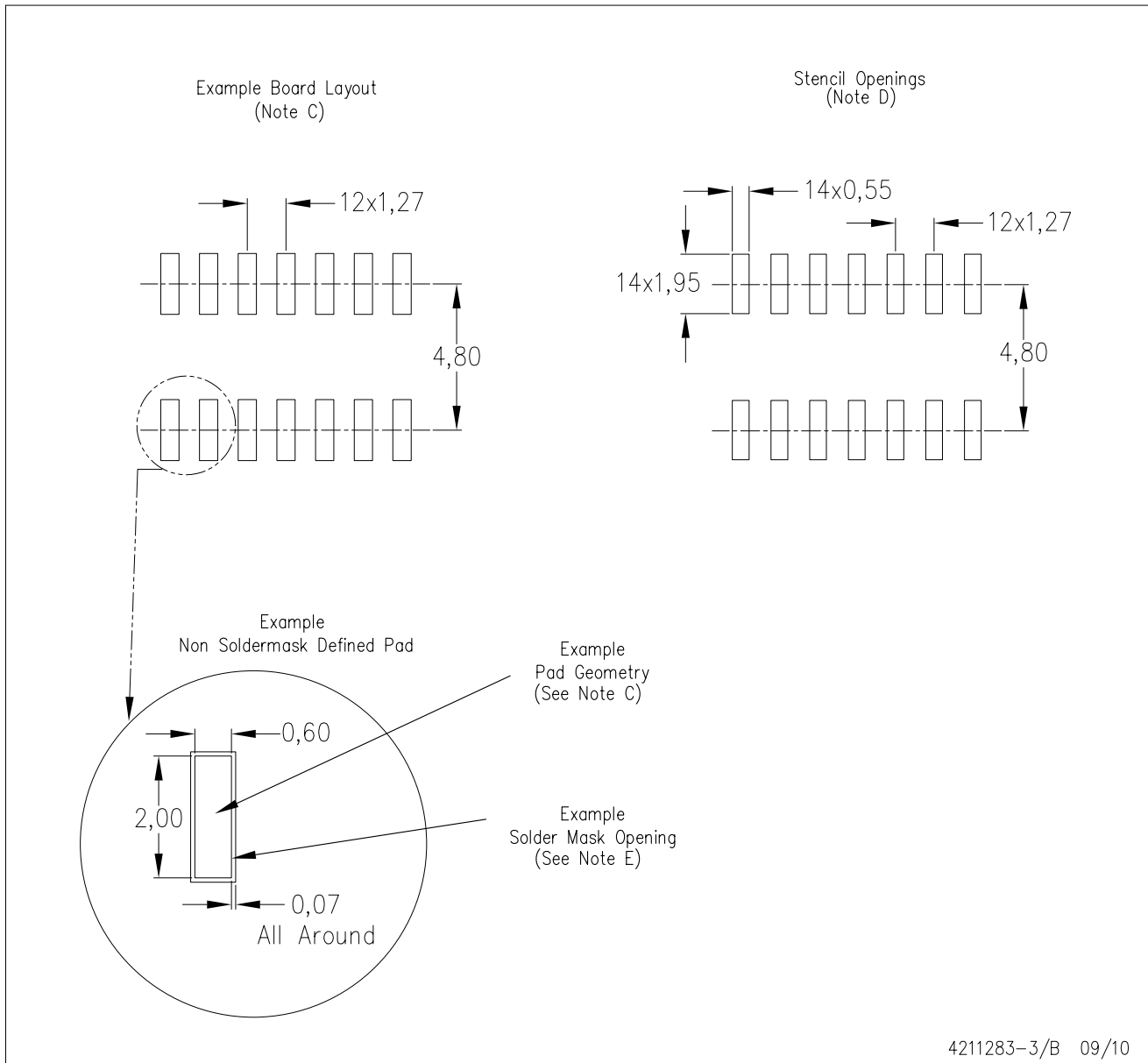
NOTES:  A.  All linear dimensions are in inches (millimeters).
        B.  This drawing is subject to change without notice.
    △C△  Body length does not include mold flash, protrusions, or gate burrs.  Mold flash, protrusions, or gate burrs shall
         not exceed .006 (0,15) per end.
    △D△  Body width does not include interlead flash.  Interlead flash shall not exceed .017 (0,43) per side.
        E.  Reference JEDEC MS−012 variation AB.

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D (R−PDSO−G14)                                    PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

12x1,27

14x0,55

12x1,27

14x1,95

4,80

4,80

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

2,00

Example
Solder Mask Opening
(See Note E)

0,07
All Around

4211283−3/B   09/10

NOTES:    A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Publication IPC−7351 is recommended for alternate designs.
          D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
               contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

**14-PINS SHOWN**



| PINS **<br>DIM | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:  A.  All linear dimensions are in millimeters.
        B.  This drawing is subject to change without notice.
        C.  Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

**PW (R-PDSO-G\*\*)**                                                    **PLASTIC SMALL-OUTLINE PACKAGE**
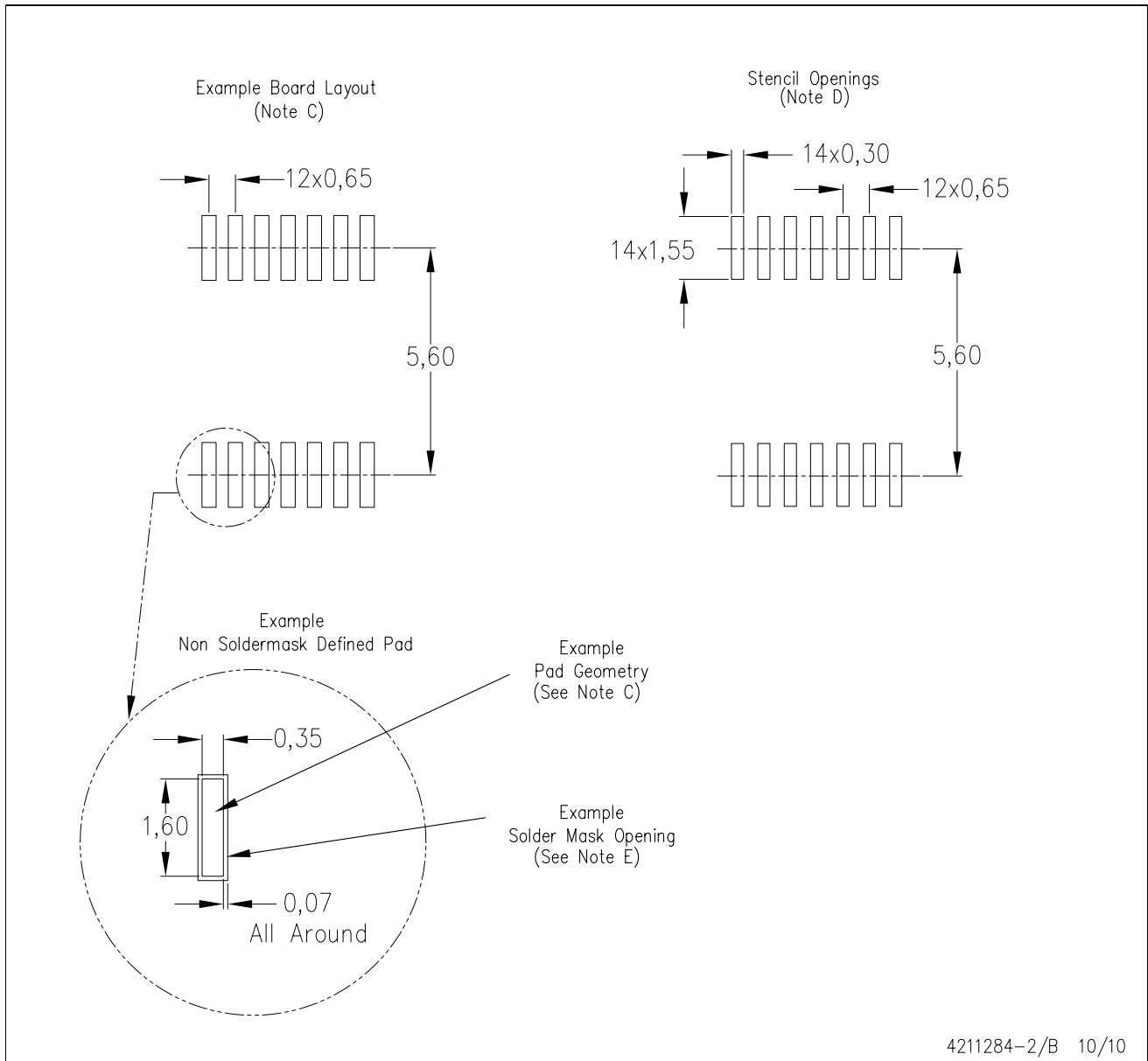
**14 PINS SHOWN**



| PINS \*\* | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

**4040064/F 01/97**

NOTES:  A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
        D. Falls within JEDEC MO-153

PW (R–PDSO–G14)                                                    PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

12x0,65

5,60

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,35

1,60

0,07
All Around

Example
Solder Mask Opening
(See Note E)

Stencil Openings
(Note D)

14x0,30

12x0,65

14x1,55

5,60

4211284–2/B   10/10

NOTES:   A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC–7351 is recommended for alternate designs.
         D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
         E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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