# CD54/74HC192, CD54/74HC193, CD54/74HCT193

Data sheet acquired from Harris Semiconductor
SCHS163F

September 1997 - Revised October 2003

## High-Speed CMOS Logic
## Presettable Synchronous 4-Bit Up/Down Counters

### Features

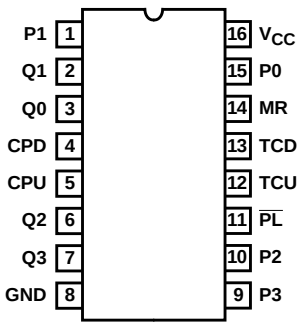
- **Synchronous Counting and Asynchronous Loading**
- **Two Outputs for N-Bit Cascading**
- **Look-Ahead Carry for High-Speed Counting**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55$^{O}$C to 125$^{O}$C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: $N_{IL}$ = 30%, $N_{IH}$ = 30% of $V_{CC}$ at $V_{CC}$ = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, $V_{IL}$= 0.8V (Max), $V_{IH}$ = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at $V_{OL}$, $V_{OH}$**

### Description

The ’HC192, ’HC193 and ’HCT193 are asynchronously presettable BCD Decade and Binary Up/Down synchronous counters, respectively.

### Pinout

**CD54HC192, CD54HC193, CD54HCT193 (CERDIP)**
**CD74HC192 (PDIP, SOP, TSSOP)**
**CD74HC193 (PDIP, SOIC)**
**CD74HCT193 (PDIP)**
TOP VIEW




Presetting the counter to the number on the preset data inputs (P0-P3) is accomplished by a LOW asynchronous parallel load input ($\overline{PL}$). The counter is incremented on the low-to-high transition of the Clock-Up input (and a high level on the Clock-Down input) and decremented on the low to high transition of the Clock-Down input (and a high level on the Clock-up input). A high level on the MR input overrides any other input to clear the counter to its zero state. The Terminal Count up (carry) goes low half a clock period before the zero count is reached and returns to a high level at the zero count. The Terminal Count Down (borrow) in the count down mode likewise goes low half a clock period before the maximum count (9 in the 192 and 15 in the 193) and returns to high at the maximum count. Cascading is effected by connecting the carry and borrow outputs of a less significant counter to the Clock-Up and Clock-Down inputs, respectively, of the next most significant counter.

If a decade counter is preset to an illegal state or assumes an illegal state when power is applied, it will return to the normal sequence in one count as shown in state diagram.

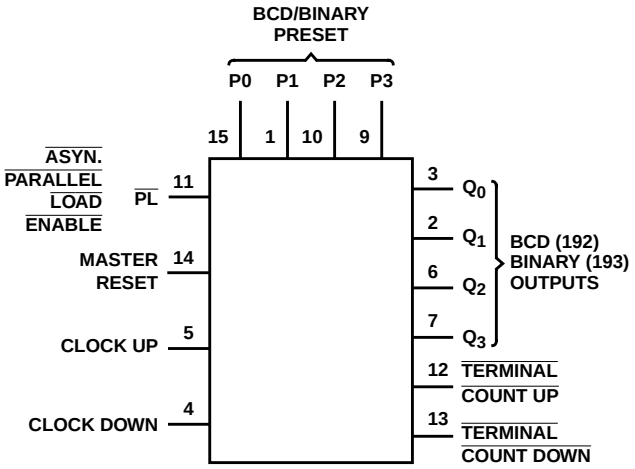
### Ordering Information

| PART NUMBER | TEMP. RANGE ($^{O}$C) | PACKAGE |
|---|---|---|
| CD54HC192F3A | -55 to 125 | 16 Ld CERDIP |
| CD54HC193F3A | -55 to 125 | 16 Ld CERDIP |
| CD54HCT193F3A | -55 to 125 | 16 Ld CERDIP |
| CD74HC192E | -55 to 125 | 16 Ld PDIP |
| CD74HC192NSR | -55 to 125 | 16 Ld SOP |
| CD74HC192PW | -55 to 125 | 16 Ld TSSOP |
| CD74HC192PWR | -55 to 125 | 16 Ld TSSOP |
| CD74HC192PWT | -55 to 125 | 16 Ld TSSOP |
| CD74HC193E | -55 to 125 | 16 Ld PDIP |
| CD74HC193M | -55 to 125 | 16 Ld SOIC |
| CD74HC193MT | -55 to 125 | 16 Ld SOIC |
| CD74HC193M96 | -55 to 125 | 16 Ld SOIC |
| CD74HCT193E | -55 to 125 | 16 Ld PDIP |

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

## Functional Diagram




**TRUTH TABLE**

| CLOCK UP | CLOCK DOWN | RESET | PARALLEL LOAD | FUNCTION |
|---|---|---|---|---|
| ↑ | H | L | H | Count Up |
| H | ↑ | L | H | Count Down |
| X | X | H | X | Reset |
| X | X | L | L | Load Preset Inputs |

H = High Voltage Level, L = Low Voltage Level, X = Don't Care, ↑ = Transition from Low to High Level

## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ . . . . . -0.5V to 7V
DC Input Diode Current, $I_{IK}$
For $V_I$ < -0.5V or $V_I$ > $V_{CC}$ + 0.5V . . . . . ±20mA
DC Output Diode Current, $I_{OK}$
For $V_O$ < -0.5V or $V_O$ > $V_{CC}$ + 0.5V . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, $I_O$
For $V_O$ > -0.5V or $V_O$ < $V_{CC}$ + 0.5V . . . . . ±25mA
DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$ . . . . . ±50mA

## Operating Conditions

Temperature Range ($T_A$) . . . . . -55°C to 125°C
Supply Voltage Range, $V_{CC}$
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, $V_I$, $V_O$ . . . . . 0V to $V_{CC}$
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)

## Thermal Information

Package Thermal Impedance, $\theta_{JA}$ (see Note 1):
E (PDIP) Package . . . . . 67°C/W
M (SOIC) Package. . . . . 73°C/W
NS (SOP) Package . . . . . 64°C/W
PW (TSSOP) Package . . . . . 108°C/W
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $I_O$ (mA) | $V_{CC}$ (V) | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 2 | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | | | 4.5 | 3.15 | - | - | 3.15 | - | 3.15 | - | V |
| | | | | 6 | 4.2 | - | - | 4.2 | - | 4.2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 2 | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | | | 4.5 | - | - | 1.35 | - | 1.35 | - | 1.35 | V |
| | | | | 6 | - | - | 1.8 | - | 1.8 | - | 1.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 2 | 1.9 | - | - | 1.9 | - | 1.9 | - | V |
| | | | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| | | | -0.02 | 6 | 5.9 | - | - | 5.9 | - | 5.9 | - | V |
| High Level Output Voltage TTL Loads | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| | | | -5.2 | 6 | 5.48 | - | - | 5.34 | - | 5.2 | - | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 2 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 6 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| | | | 5.2 | 6 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ or GND | - | 6 | - | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 6 | - | - | 8 | - | 80 | - | 160 | µA |

## DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | | | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $I_O$ (mA) | $V_{CC}$ (V) | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HCT TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 4.5 to 5.5 | 2 | - | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 4.5 to 5.5 | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| High Level Output Voltage TTL Loads | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ to GND | - | 5.5 | - | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | - | 5.5 | - | - | 8 | - | 80 | - | 160 | µA |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | $\Delta I_{CC}$ (Note 2) | $V_{CC}$ - 2.1 | - | 4.5 to 5.5 | - | 100 | 360 | - | 450 | - | 490 | µA |

NOTE:

2. For dual-supply systems theoretical worst case ($V_I$ = 2.4V, $V_{CC}$ = 5.5V) specification is 1.8mA.

## HCT Input Loading Table

| INPUT | UNIT LOADS |
|---|---|
| P0-P3 | 0.4 |
| MR | 1.45 |
| $\overline{PL}$ | 0.85 |
| CPU, CPD | 1.45 |

NOTE: Unit Load is $\Delta I_{CC}$ limit specified in DC Electrical Specifications table, e.g. 360µA max at 25°C.

**Prerequisite For Switching Specifications**

| PARAMETER | SYMBOL | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | |
| Pulse Width | $t_W$ | 2 | 115 | - | - | 145 | - | 175 | - | ns |
| CPU, CPD | | 4.5 | 23 | - | - | 29 | - | 35 | - | ns |
| 192 | | 6 | 20 | - | - | 25 | - | 30 | - | ns |
| | $t_W$ | 2 | 100 | - | - | 125 | - | 150 | - | ns |
| CPU, CPD | | 4.5 | 20 | - | - | 25 | - | 30 | - | ns |
| 193 | | 6 | 17 | - | - | 21 | - | 26 | - | ns |
| $\overline{PL}$ | $t_W$ | 2 | 80 | - | - | 100 | - | 120 | - | ns |
| | | 4.5 | 16 | - | - | 20 | - | 24 | - | ns |
| | | 6 | 14 | - | - | 17 | - | 20 | - | ns |
| MR | $t_W$ | 2 | 100 | - | - | 125 | - | 150 | - | ns |
| | | 4.5 | 20 | - | - | 25 | - | 30 | - | ns |
| | | 6 | 17 | - | - | 21 | - | 26 | - | ns |
| Set-up Time | $t_{SU}$ | 2 | 80 | - | - | 100 | - | 120 | - | ns |
| Pn to $\overline{PL}$ | | 4.5 | 16 | - | - | 20 | - | 24 | - | ns |
| | | 6 | 14 | - | - | 17 | - | 20 | - | ns |
| Hold Time | $t_H$ | 2 | 0 | - | - | 0 | - | 0 | - | ns |
| Pn to $\overline{PL}$ | | 4.5 | 0 | - | - | 0 | - | 0 | - | ns |
| | | 6 | 0 | - | - | 0 | - | 0 | - | ns |
| Hold Time | $t_H$ | 2 | 80 | - | - | 100 | - | 120 | - | ns |
| CPD to CPU or | | 4.5 | 16 | - | - | 20 | - | 24 | - | ns |
| CPU to CPD | | 6 | 14 | - | - | 17 | - | 20 | - | ns |
| Recovery Time | $t_{REC}$ | 2 | 80 | - | - | 100 | - | 120 | - | ns |
| $\overline{PL}$ to CPU, CPD | | 4.5 | 16 | - | - | 20 | - | 24 | - | ns |
| | | 6 | 14 | - | - | 17 | - | 20 | - | ns |
| MR to CPU, CPD | $t_{REC}$ | 2 | 5 | - | - | 5 | - | 5 | - | ns |
| | | 4.5 | 5 | - | - | 5 | - | 5 | - | ns |
| | | 6 | 5 | - | - | 5 | - | 5 | - | ns |
| Maximum Frequency | $f_{MAX}$ | 2 | 5 | - | - | 4 | - | 3 | - | MHz |
| CPU, CPD | | 4.5 | 22 | - | - | 18 | - | 15 | - | MHz |
| 192 | | 6 | 24 | - | - | 21 | - | 18 | - | MHz |
| | $f_{MAX}$ | 2 | 5 | - | - | 4 | - | 3 | - | MHz |
| CPU, CPD | | 4.5 | 25 | - | - | 20 | - | 17 | - | MHz |
| 193 | | 6 | 29 | - | - | 24 | - | 20 | - | MHz |
| **HCT TYPES** | | | | | | | | | | |
| Pulse Width | $t_W$ | 2 | - | - | - | - | - | - | - | ns |
| CPU, CPD | | 4.5 | 23 | - | - | 29 | - | 35 | - | ns |
| 192 | | 6 | - | - | - | - | - | - | - | ns |
| CPU, CPD | $t_W$ | 2 | - | - | - | - | - | - | - | ns |
| 193 | | 4.5 | 23 | - | - | 29 | - | 35 | - | ns |
| | | 6 | - | - | - | - | - | - | - | ns |

## Prerequisite For Switching Specifications (Continued)

| PARAMETER | SYMBOL | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $\overline{PL}$ | $t_W$ | 2 | - | - | - | - | - | - | - | ns |
| | | 4.5 | 16 | - | - | 20 | - | 24 | - | ns |
| | | 6 | - | - | - | - | - | - | - | ns |
| MR | $t_W$ | 2 | - | - | - | - | - | - | - | ns |
| | | 4.5 | 20 | - | - | 25 | - | 30 | - | ns |
| | | 6 | - | - | - | - | - | - | - | ns |
| Set-up Time | $t_{SU}$ | 2 | - | - | - | - | - | - | - | ns |
| Pn to $\overline{PL}$ | | 4.5 | 15 | - | - | 19 | - | 22 | - | ns |
| | | 6 | - | - | - | - | - | - | - | ns |
| Hold Time | $t_H$ | 2 | - | - | - | - | - | - | - | ns |
| Pn to $\overline{PL}$ | | 4.5 | 0 | - | - | 0 | - | 0 | - | ns |
| | | 6 | - | - | - | - | - | - | - | ns |
| Hold Time | $t_H$ | 2 | - | - | - | - | - | - | - | ns |
| CPD to CPU or | | 4.5 | 16 | - | - | 20 | - | 24 | - | ns |
| CPU to CPD | | 6 | - | - | - | - | - | - | - | ns |
| Recovery Time | $t_{REC}$ | 2 | - | - | - | - | - | - | - | ns |
| $\overline{PL}$ to CPU, CPD | | 4.5 | 15 | - | - | 19 | - | 22 | - | ns |
| | | 6 | - | - | - | - | - | - | - | ns |
| MR to CPU, CPD | $t_{REC}$ | 2 | - | - | - | - | - | - | - | ns |
| | | 4.5 | 5 | - | - | 5 | - | 5 | - | ns |
| | | 6 | - | - | - | - | - | - | - | ns |
| Maximum Frequency | $f_{MAX}$ | 2 | - | - | - | - | - | - | - | MHz |
| CPU, CPD | | 4.5 | 22 | - | - | 18 | - | 15 | - | MHz |
| 192 | | 6 | - | - | - | - | - | - | - | MHz |
| CPU, CPD | $f_{MAX}$ | 2 | - | - | - | - | - | - | - | MHz |
| 193 | | 4.5 | 22 | - | - | 18 | - | 15 | - | MHz |
| | | 6 | - | - | - | - | - | - | - | MHz |

## Switching Specifications Input $t_r$, $t_f$ = 6ns

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | | |
| Propagation Delay | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 125 | - | 155 | - | 190 | ns |
| CPU to $\overline{TCU}$ | | $C_L$ = 50pF | 4.5 | - | - | 25 | - | 31 | - | 38 | ns |
| | | $C_L$ = 15pF | 5 | - | 10 | - | - | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | | 21 | - | 26 | - | 32 | ns |
| CPD to $\overline{TCD}$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 125 | - | 155 | - | 190 | ns |
| | | $C_L$ = 50pF | 4.5 | - | - | 25 | - | 31 | - | 38 | ns |
| | | $C_L$ = 15pF | 5 | - | 10 | - | - | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | - | 21 | - | 26 | - | 32 | ns |
| CPU to $Q_n$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 220 | - | 270 | - | 325 | ns |
| | | $C_L$ = 50pF | 4.5 | - | - | 43 | - | 54 | - | 65 | ns |
| | | $C_L$ = 15pF | 5 | - | 18 | - | - | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | - | 37 | - | 46 | - | 55 | ns |

**Switching Specifications** Input $t_r$, $t_f$ = 6ns **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| CPD to $Q_n$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 220 | - | 270 | - | 325 | ns |
| | | $C_L$ = 50pF | 4.5 | - | - | 43 | - | 54 | - | 65 | ns |
| | | $C_L$ = 15pF | 5 | - | 18 | - | - | - | - | | ns |
| | | $C_L$ = 50pF | 6 | - | - | 37 | - | 46 | - | 55 | ns |
| $\overline{PL}$ to $Q_n$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 220 | - | 275 | - | 330 | ns |
| | | $C_L$ = 50pF | 4.5 | - | - | 44 | - | 55 | - | 66 | ns |
| | | $C_L$ = 15pF | 5 | - | 18 | - | - | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | - | 37 | - | 47 | - | 56 | ns |
| MR to $Q_n$ | $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 200 | - | 250 | - | 300 | ns |
| | | $C_L$ = 50pF | 4.5 | - | - | 40 | - | 50 | - | 60 | ns |
| | | $C_L$ = 15pF | 5 | - | 17 | - | - | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | - | 34 | - | 43 | - | 51 | ns |
| Transition Time | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 2 | - | - | 75 | - | 95 | - | 110 | ns |
| Q, TCU, TCD | | | 4.5 | - | - | 15 | - | 19 | - | 22 | ns |
| | | | 6 | - | - | 13 | - | 16 | - | 19 | ns |
| Input Capacitance | $C_{IN}$ | $C_L$ = 50pF | - | - | - | 10 | - | 10 | - | 10 | pF |
| Power Dissipation Capacitance (Notes 3, 4) | $C_{PD}$ | $C_L$ = 15pF | 5 | - | 40 | - | - | - | - | - | pF |
| **HCT TYPES** | | | | | | | | | | | |
| Propagation Delay | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 27 | - | 34 | - | 41 | ns |
| CPU to $\overline{TCU}$ | | $C_L$ = 15pF | 5 | - | 11 | - | - | - | - | - | ns |
| CPU to $\overline{TCD}$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 27 | - | 34 | - | 41 | ns |
| | | $C_L$ = 15pF | 5 | - | 11 | - | - | - | - | - | ns |
| CPU to $Q_n$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 40 | - | 50 | - | 60 | ns |
| | | $C_L$ = 15pF | 5 | - | 17 | - | - | - | - | - | ns |
| CPD to $Q_n$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 40 | - | 50 | - | 60 | ns |
| | | $C_L$ = 15pF | 5 | - | 17 | - | - | - | - | - | ns |
| $\overline{PL}$ to $Q_n$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 46 | - | 58 | - | 69 | ns |
| | | $C_L$ = 15pF | 5 | - | 21 | - | - | - | - | - | ns |
| MR to $Q_n$ | $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 43 | - | 54 | - | 65 | ns |
| | | $C_L$ = 15pF | 5 | - | 18 | - | - | - | - | - | ns |
| Transition Time | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | | | | | | | | | |
| Q, TCU, TCD | | | 4.5 | - | - | 15 | - | 19 | - | 22 | ns |
| Input Capacitance | $C_{IN}$ | $C_L$ = 50pF | - | - | - | 10 | - | 10 | - | 10 | pF |
| Power Dissipation Capacitance (Notes 3, 4) | $C_{PD}$ | $C_L$ = 15pF | 5 | - | 50 | - | - | - | - | - | pF |

NOTES:

3. $C_{PD}$ is used to determine the dynamic power consumption, per gate.
4. $P_D = V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2)$ where $f_i$ = Input Frequency, $C_L$ = Output Load Capacitance, $V_{CC}$ = Supply Voltage.

## Test Circuits and Waveforms

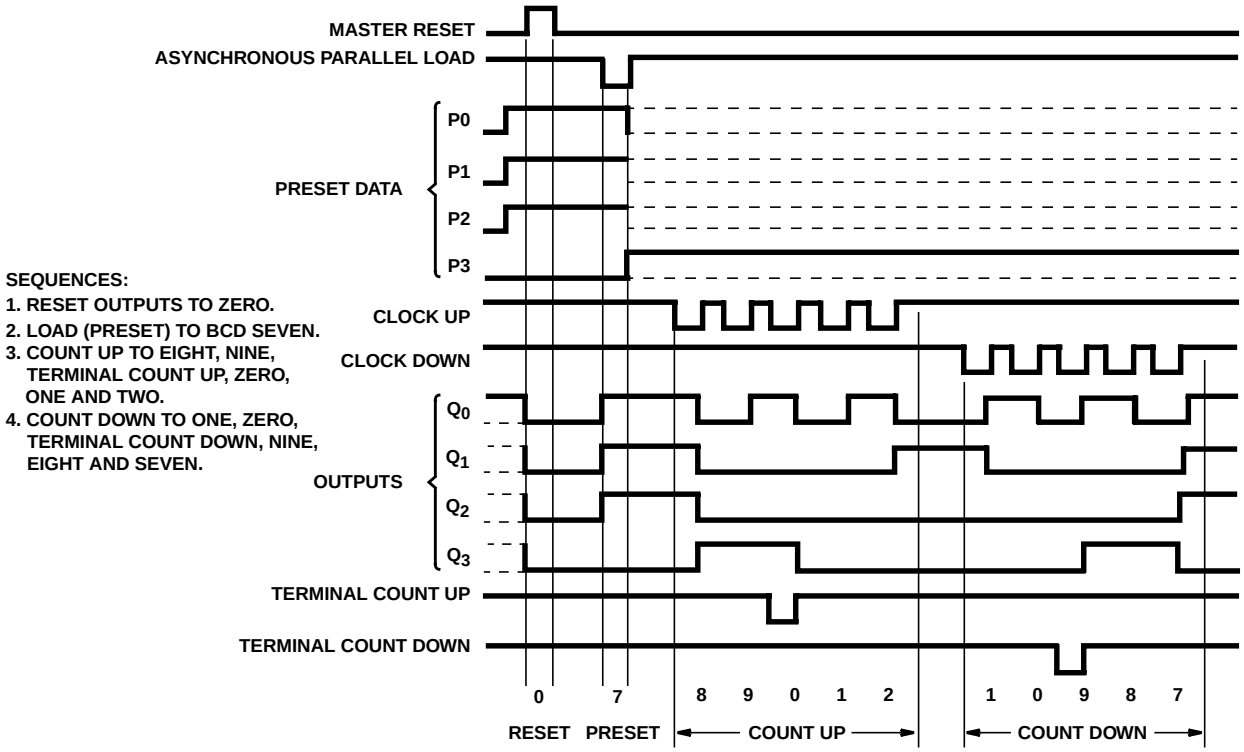
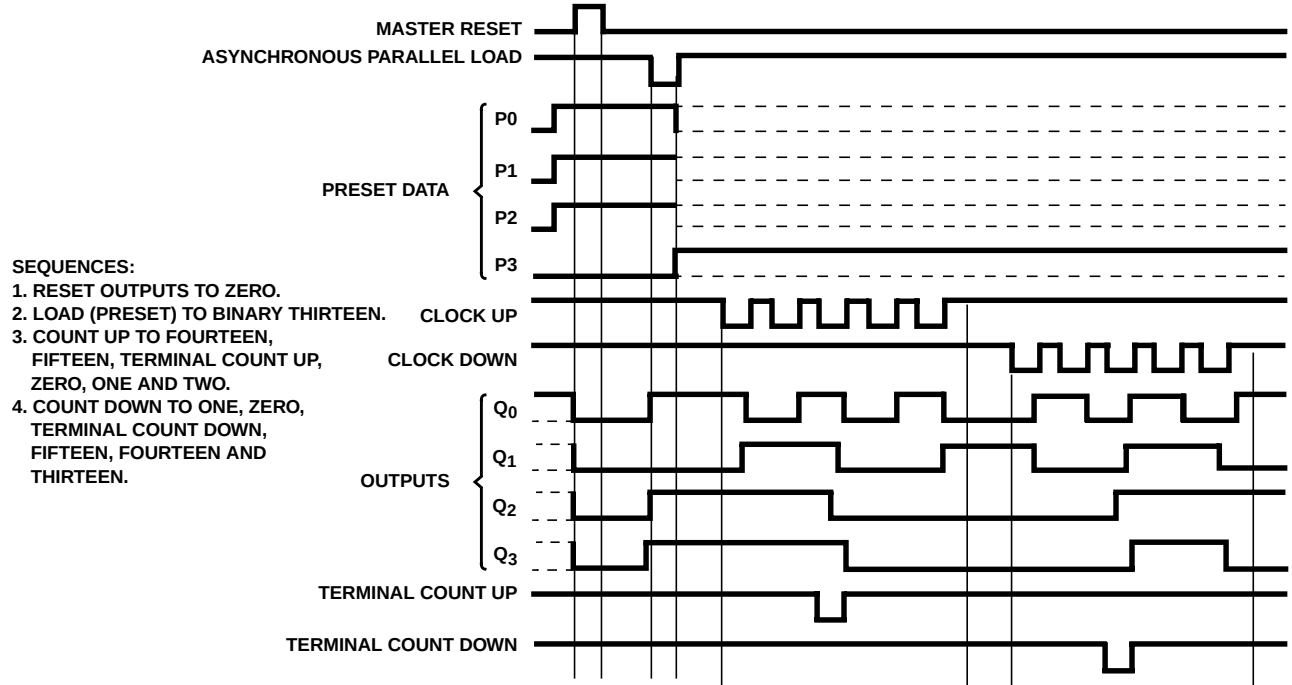



**FIGURE 1. ’HC192 SYNCHRONOUS DECADE COUNTERS, TYPICAL RESET, PRESET AND COUNT SEQUENCES**

## Test Circuits and Waveforms (Continued)




NOTES:

1. Master reset overrides load data and clock inputs.
2. When counting up, clock-down input must be high. When counting down, clock-up input must be high.

**FIGURE 2. ’HC193 SYNCHRONOUS BINARY COUNTERS, TYPICAL RESET, PRESET AND COUNT SEQUENCES**

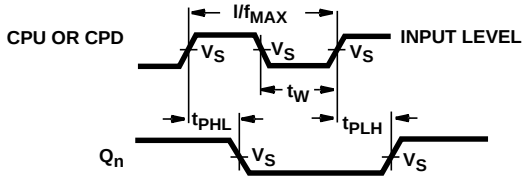



**FIGURE 3. CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH**

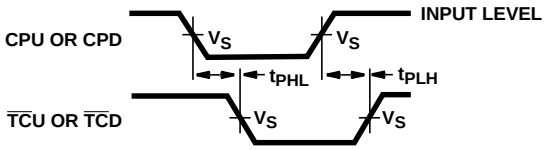



**FIGURE 4. CLOCK TO TERMINAL COUNT DELAYS**

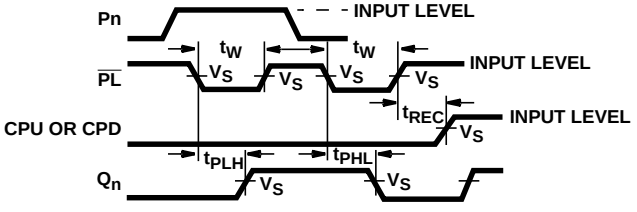



**FIGURE 5. PARALLEL LOAD PULSE WIDTH, PARALLEL LOAD TO OUTPUT DELAYS, AND PARALLEL LOAD TO CLOCK RECOVERY TIME**

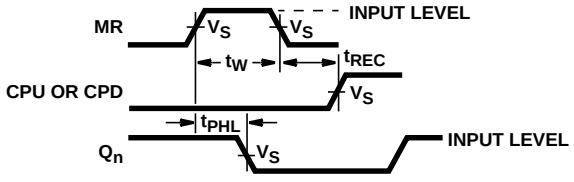



**FIGURE 6. MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME**

## *Test Circuits and Waveforms* (Continued)

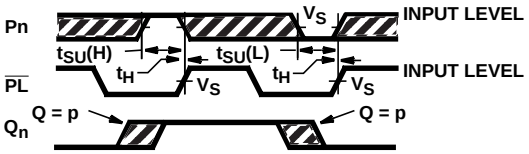



**FIGURE 7. SET-UP AND HOLD TIMES DATA TO PARALLEL LOAD (PL)**

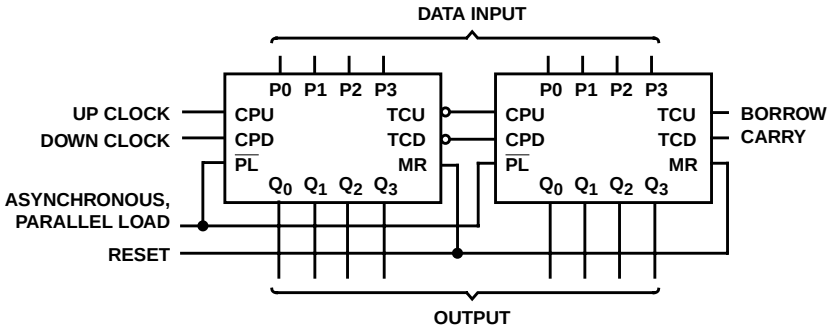
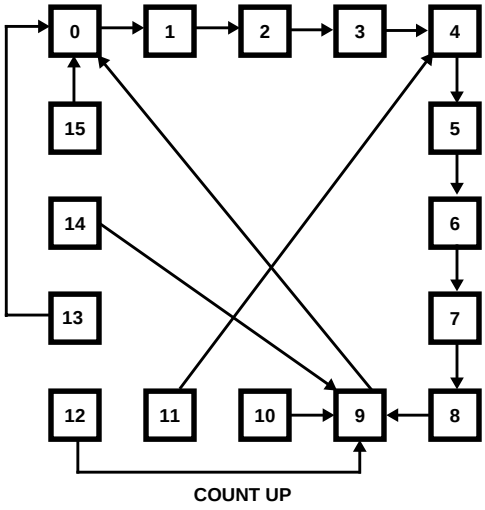
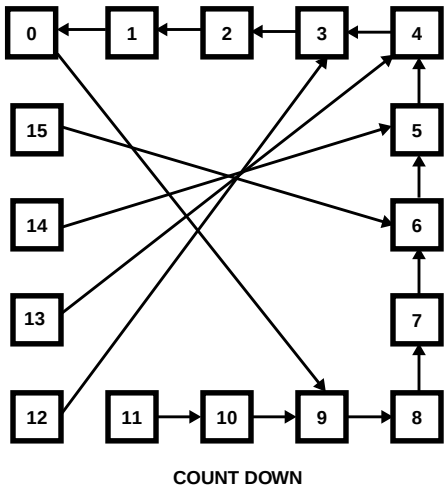



**FIGURE 8. CASCADED UP/DOWN COUNTER WITH PARALLEL LOAD**




NOTE: Illegal states in BCD counters corrected in one count.

NOTE: Illegal states in BCD counters corrected in one or two counts.

**FIGURE 9. 'HC192, 'HCT193 STATE DIAGRAMS**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| 5962-8780801EA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type |
| 5962-9084801MEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type |
| 9084801MEAS2035 | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI |
| CD54HC192F3A | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type |
| CD54HC193F3A | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type |
| CD54HCT193F3A | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type |
| CD74HC192E | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74HC192EE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74HC192NSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC192NSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC192NSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC192PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC192PWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC192PWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC192PWT | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC192PWTE4 | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC192PWTG4 | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC193E | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74HC193EE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74HC193M | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC193M96 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC193M96E4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC193M96G4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC193ME4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC193MG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC193MT | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC193MTE4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| CD74HC193MTG4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HCT193E | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74HCT193EE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |

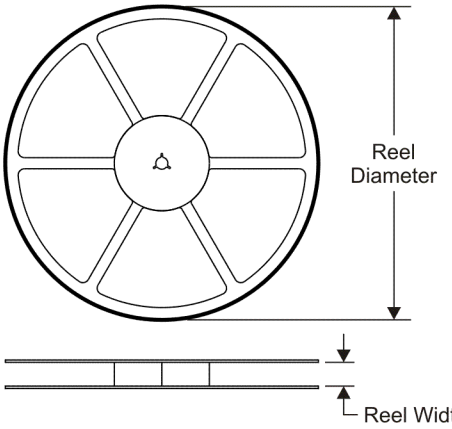
(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

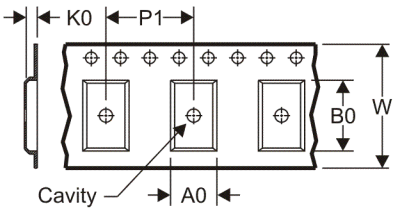
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

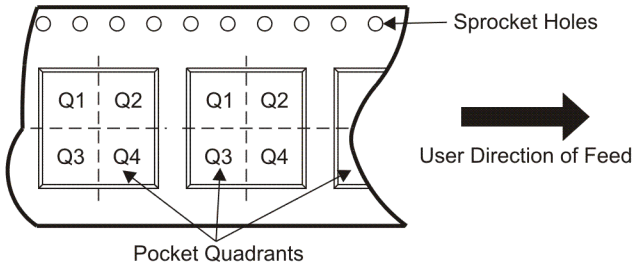



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

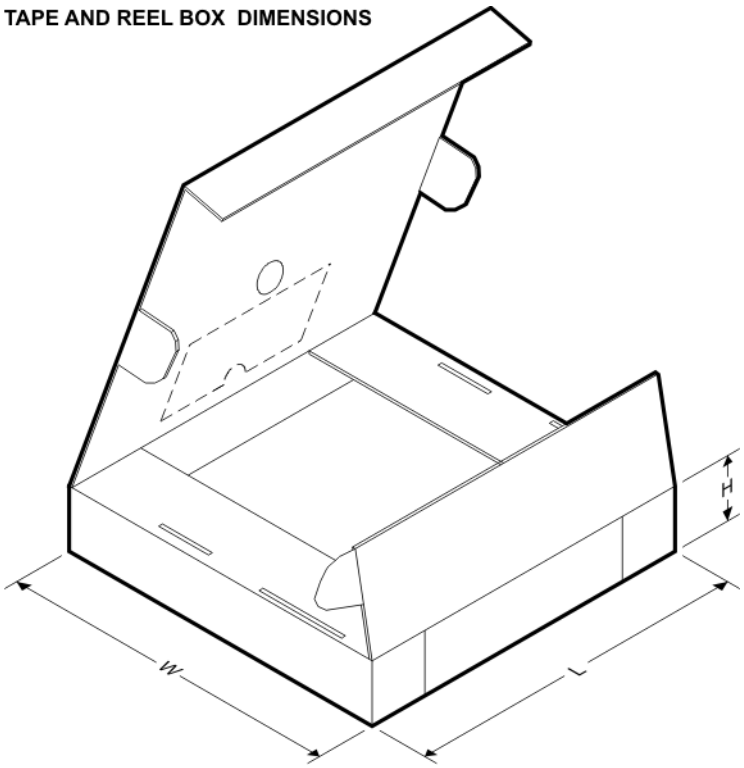
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74HC192NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| CD74HC192PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| CD74HC192PWT | TSSOP | PW | 16 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| CD74HC193M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



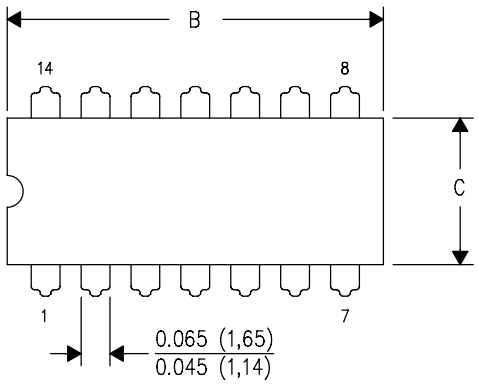

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD74HC192NSR | SO | NS | 16 | 2000 | 346.0 | 346.0 | 33.0 |
| CD74HC192PWR | TSSOP | PW | 16 | 2000 | 346.0 | 346.0 | 29.0 |
| CD74HC192PWT | TSSOP | PW | 16 | 250 | 346.0 | 346.0 | 29.0 |
| CD74HC193M96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |

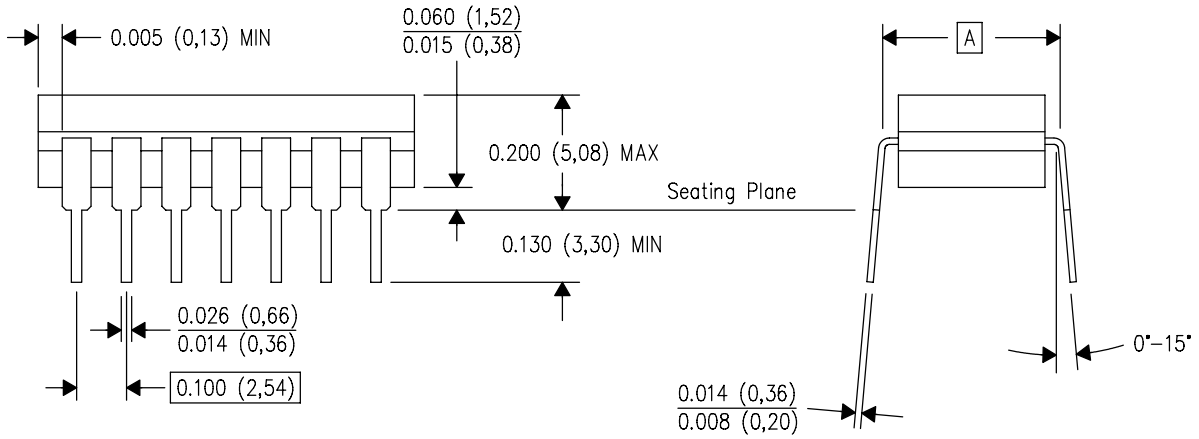
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



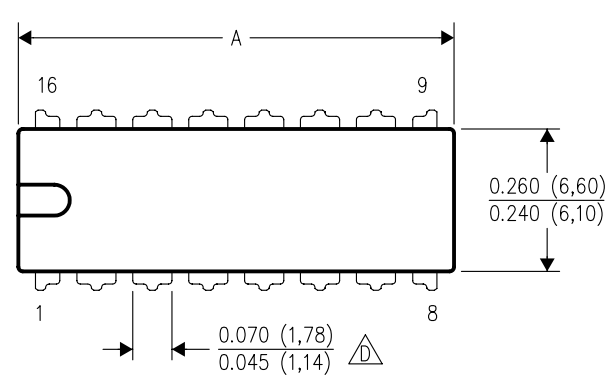

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

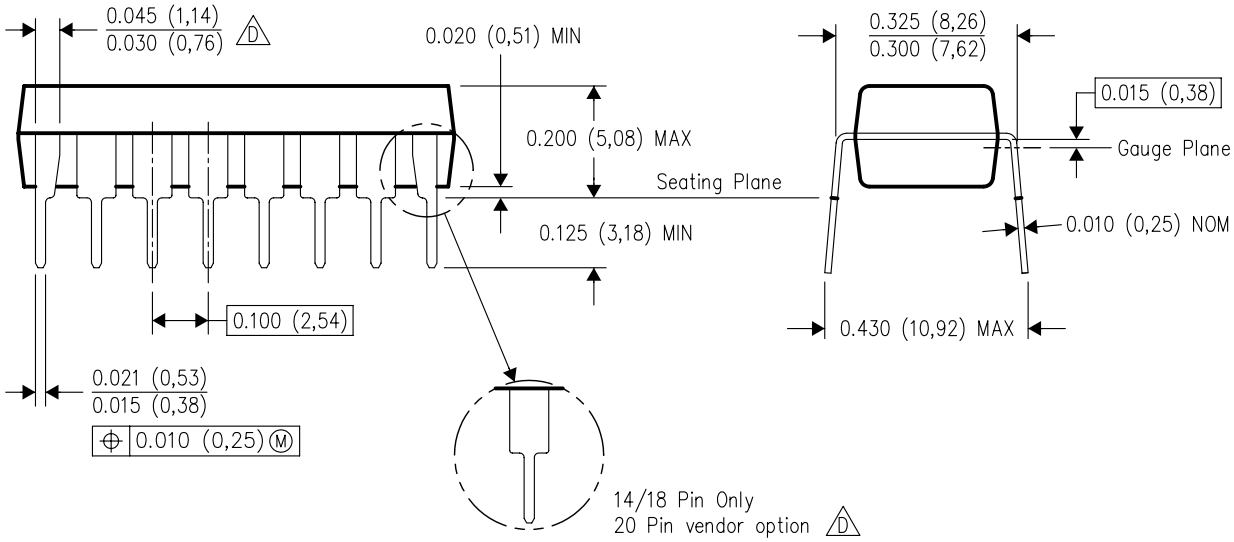
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



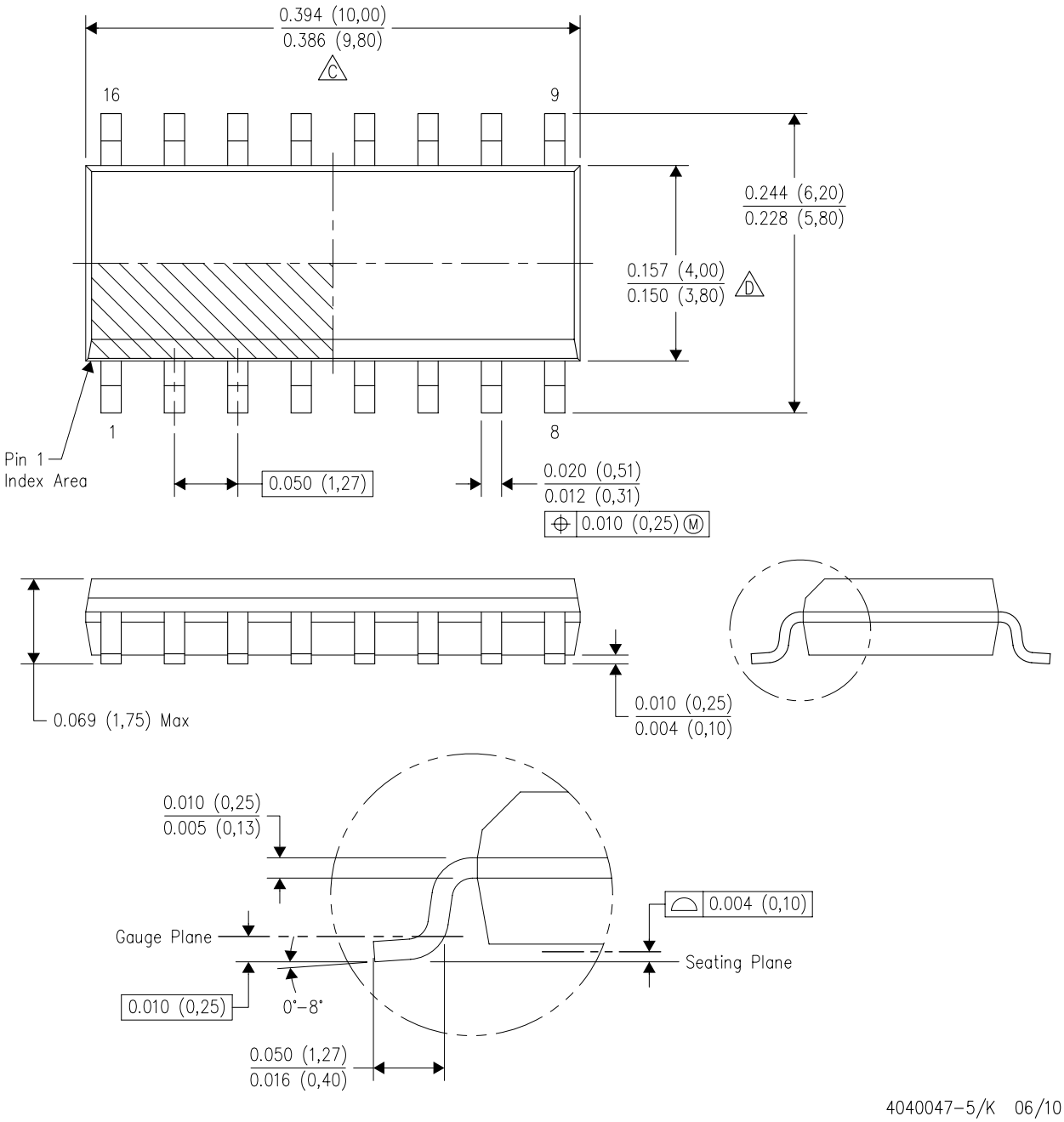

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

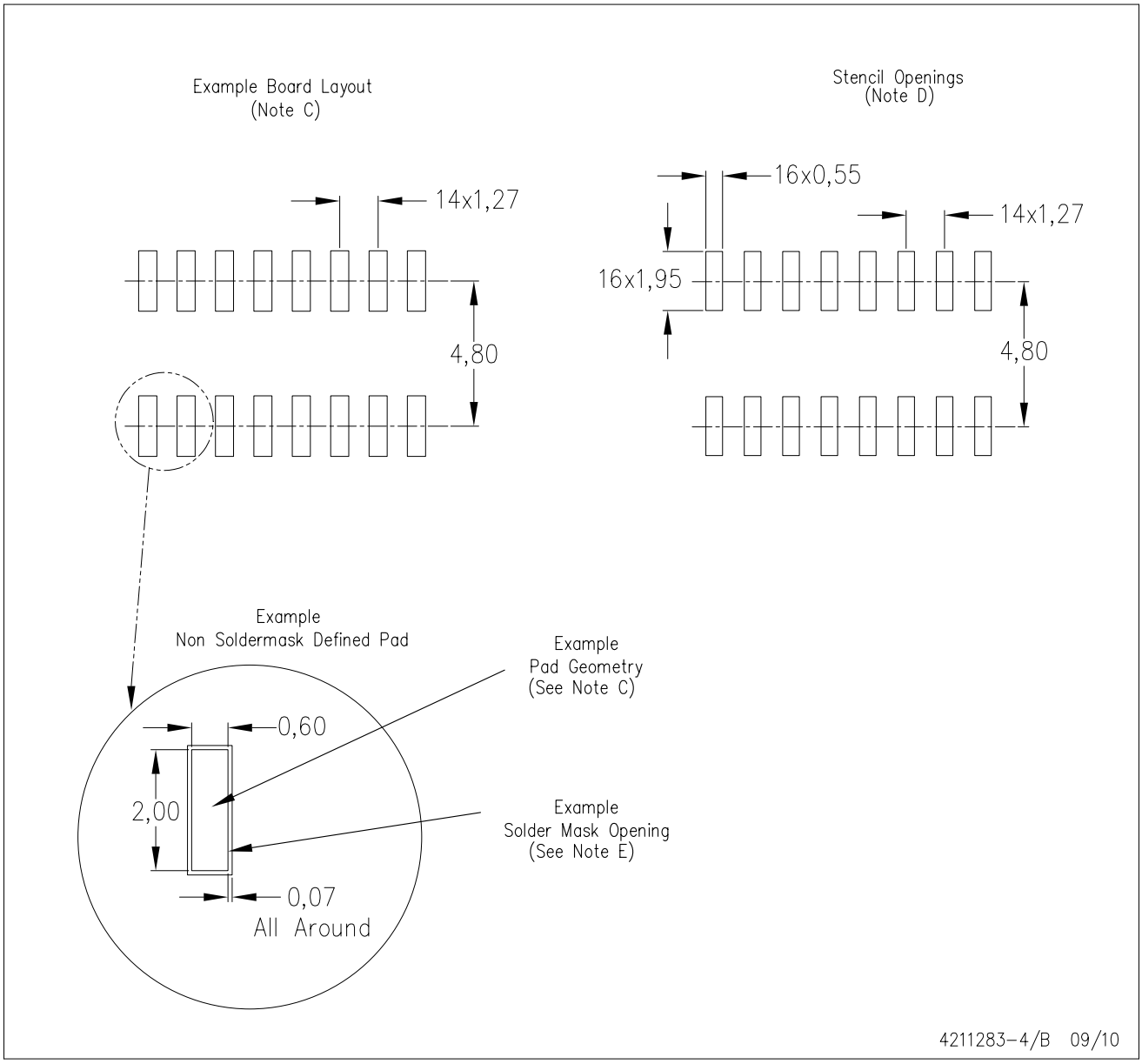
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

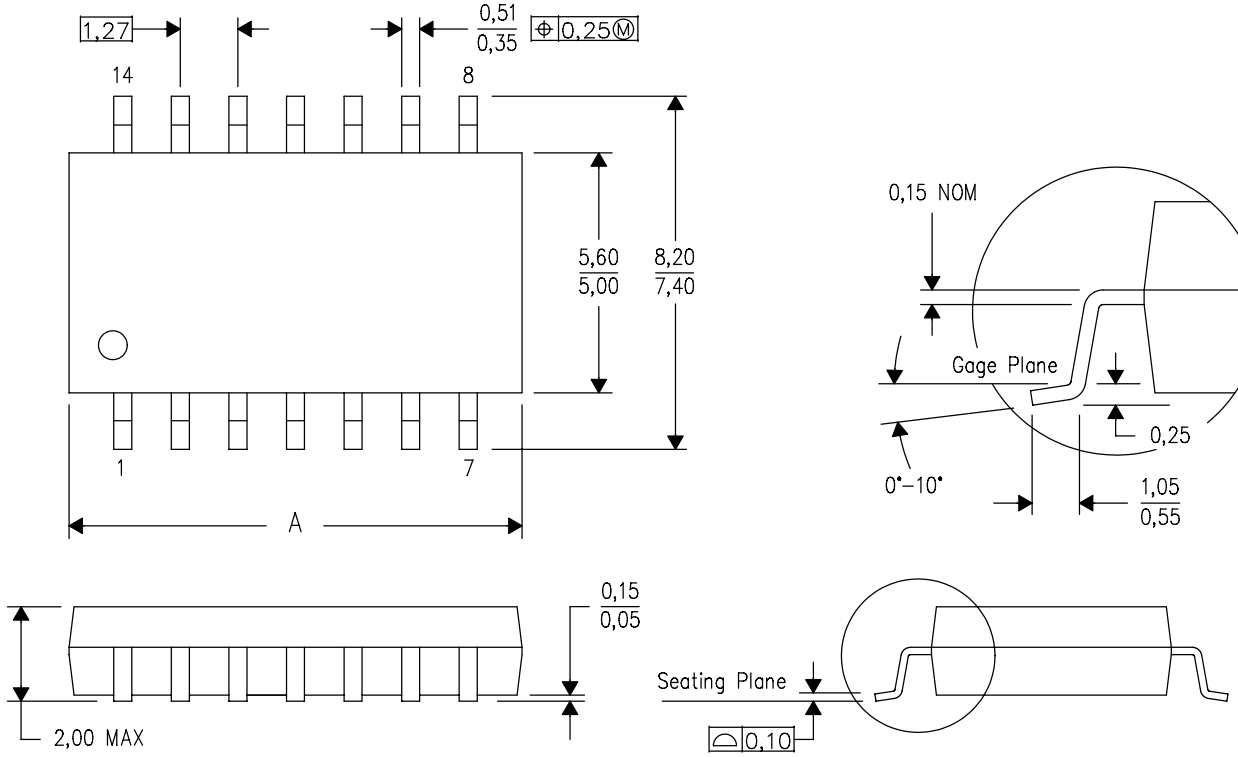



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



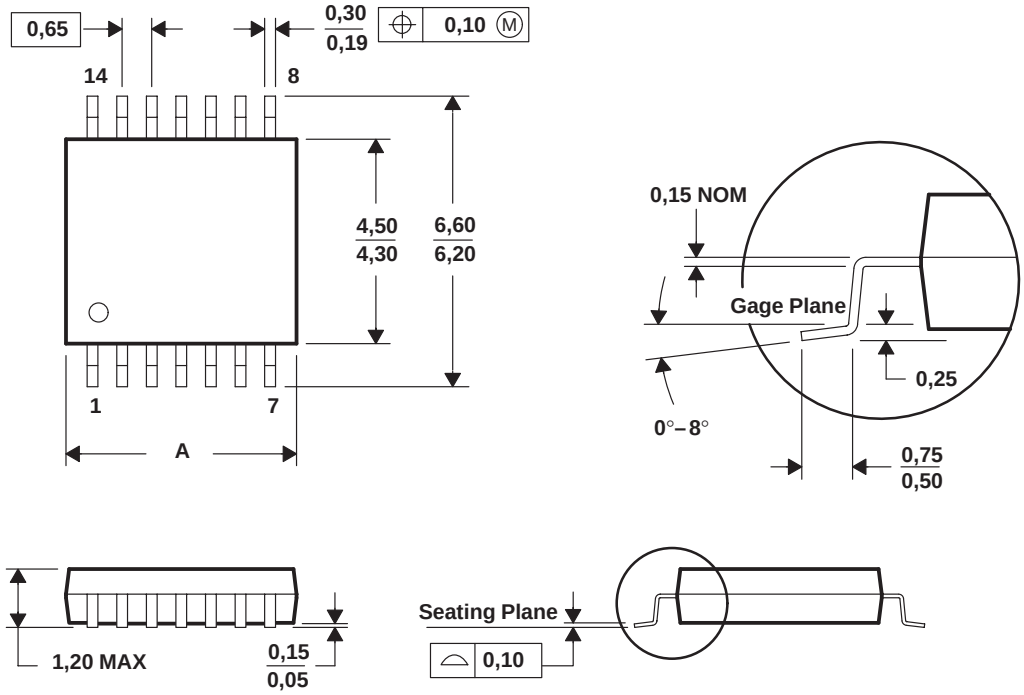

| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

**PW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PINS SHOWN**

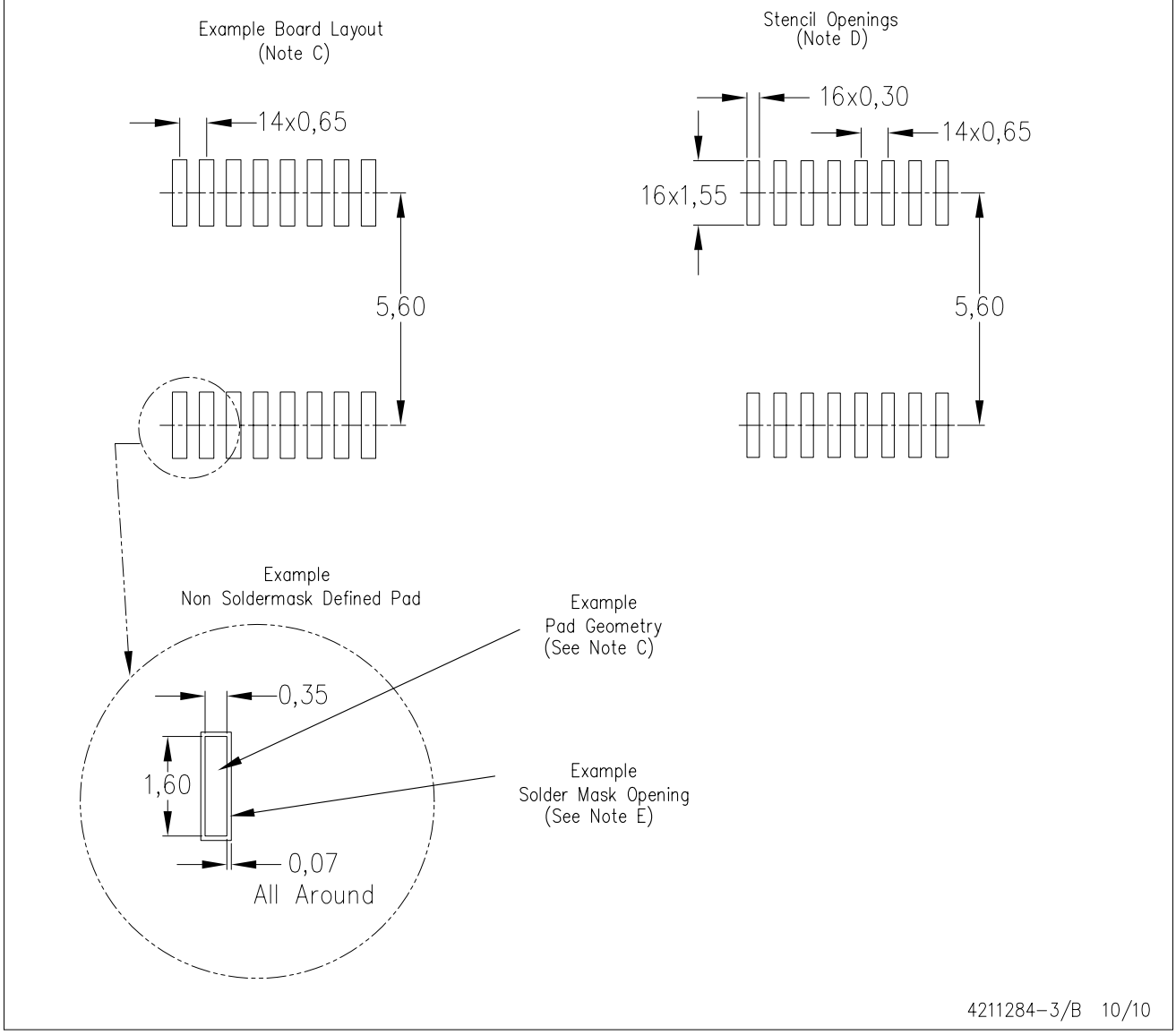



| DIM \ PINS ** | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

**4040064/F 01/97**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

| **Products** | | **Applications** | |
|---|---|---|---|
| Amplifiers | amplifier.ti.com | Audio | www.ti.com/audio |
| Data Converters | dataconverter.ti.com | Automotive | www.ti.com/automotive |
| DLP® Products | www.dlp.com | Communications and Telecom | www.ti.com/communications |
| DSP | dsp.ti.com | Computers and Peripherals | www.ti.com/computers |
| Clocks and Timers | www.ti.com/clocks | Consumer Electronics | www.ti.com/consumer-apps |
| Interface | interface.ti.com | Energy | www.ti.com/energy |
| Logic | logic.ti.com | Industrial | www.ti.com/industrial |
| Power Mgmt | power.ti.com | Medical | www.ti.com/medical |
| Microcontrollers | microcontroller.ti.com | Security | www.ti.com/security |
| RFID | www.ti-rfid.com | Space, Avionics & Defense | www.ti.com/space-avionics-defense |
| RF/IF and ZigBee® Solutions | www.ti.com/lprf | Video and Imaging | www.ti.com/video |
| | | Wireless | www.ti.com/wireless-apps |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265