PD - 95390

# IRFIB5N50LPbF

International
IOR Rectifier

## SMPS MOSFET

HEXFET® Power MOSFET

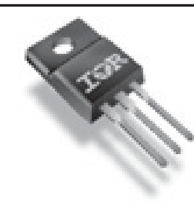
### Applications

- Zero Voltage Switching SMPS
- Telecom and Server Power Supplies
- Uninterruptible Power Supplies
- Motor Control applications
- Lead-Free

| $V_{DSS}$ | $R_{DS(on)}$ typ. | Trr typ. | $I_D$ |
|---|---|---|---|
| 500V | 0.67Ω | 73ns | 4.7A |

### Features and Benefits

- SuperFast body diode eliminates the need for external diodes in ZVS applications.
- Lower Gate charge results in simpler drive requirements.
- Enhanced dv/dt capabilities offer improved ruggedness.
- Higher Gate voltage threshold offers improved noise immunity.

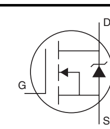


TO-220 Full-Pak

### Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---|---|---|---|
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V | 4.7 | A |
| $I_D$ @ $T_C$ = 100°C | Continuous Drain Current, $V_{GS}$ @ 10V | 3.0 | |
| $I_{DM}$ | Pulsed Drain Current ① | 16 | |
| $P_D$ @$T_C$ = 25°C | Power Dissipation | 42 | W |
| | Linear Derating Factor | 0.33 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ±30 | V |
| dv/dt | Peak Diode Recovery dv/dt ② | 13 | V/ns |
| $T_J$<br>$T_{STG}$ | Operating Junction and<br>Storage Temperature Range | -55 to + 150 | °C |
| | Soldering Temperature, for 10 seconds | 300 (1.6mm from case ) | |
| | Mounting torque, 6-32 or M3 screw | 10lb·in (1.1N·m) | |

### Diode Characteristics

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current<br>(Body Diode) | —— | —— | 4.7 | A | MOSFET symbol<br>showing the |
| $I_{SM}$ | Pulsed Source Current<br>(Body Diode) ① | —— | —— | 16 | | integral reverse<br>p-n junction diode.  |
| $V_{SD}$ | Diode Forward Voltage | —— | —— | 1.5 | V | $T_J$ = 25°C, $I_S$ = 4.0A, $V_{GS}$ = 0V ④ |
| $t_{rr}$ | Reverse Recovery Time | —— | 73 | 110 | ns | $T_J$ = 25°C, $I_F$ = 4.0A |
| | | —— | 99 | 150 | | $T_J$ = 125°C, di/dt = 100A/µs ④ |
| $Q_{rr}$ | Reverse Recovery Charge | —— | 200 | 310 | nC | $T_J$ = 25°C, $I_S$ = 4.0A, $V_{GS}$ = 0V ④ |
| | | —— | 360 | 540 | | $T_J$ = 125°C, di/dt = 100A/µs ④ |
| $I_{RRM}$ | Reverse Recovery Current | —— | 6.7 | 10 | A | $T_J$ = 25°C |
| $t_{on}$ | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD) | | | | |

## Static @ $T_J$ = 25°C (unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 500 | — | — | V | $V_{GS}$ = 0V, $I_D$ = 250μA |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.43 | — | V/°C | Reference to 25°C, $I_D$ = 1mA |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | 0.67 | 0.80 | Ω | $V_{GS}$ = 10V, $I_D$ = 2.4A ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 3.0 | — | 5.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 250μA |
| $I_{DSS}$ | Drain-to-Source Leakage Current | — | — | 50 | μA | $V_{DS}$ = 500V, $V_{GS}$ = 0V |
| | | — | — | 2.0 | mA | $V_{DS}$ = 400V, $V_{GS}$ = 0V, $T_J$ = 125°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | — | — | 100 | nA | $V_{GS}$ = 30V |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | $V_{GS}$ = -30V |
| $R_G$ | Internal Gate Resistance | — | 2.0 | — | Ω | f = 1MHz, open drain |

## Dynamic @ $T_J$ = 25°C (unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| gfs | Forward Transconductance | 2.8 | — | — | S | $V_{DS}$ = 50V, $I_D$ = 2.4A |
| $Q_g$ | Total Gate Charge | — | — | 45 | nC | $I_D$ = 4.0A |
| $Q_{gs}$ | Gate-to-Source Charge | — | — | 13 | | $V_{DS}$ = 400V |
| $Q_{gd}$ | Gate-to-Drain ("Miller") Charge | — | — | 23 | | $V_{GS}$ = 10V, See Fig. 7 & 16 ④ |
| $t_{d(on)}$ | Turn-On Delay Time | — | 13 | — | ns | $V_{DD}$ = 250V |
| $t_r$ | Rise Time | — | 17 | — | | $I_D$ = 4.0A |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 26 | — | | $R_G$ = 9.0Ω |
| $t_f$ | Fall Time | — | 10 | — | | $V_{GS}$ = 10V, See Fig. 11a & 11b ④ |
| $C_{iss}$ | Input Capacitance | — | 1000 | — | pF | $V_{GS}$ = 0V |
| $C_{oss}$ | Output Capacitance | — | 110 | — | | $V_{DS}$ = 25V |
| $C_{rss}$ | Reverse Transfer Capacitance | — | 12 | — | | ƒ = 1.0MHz, See Fig. 5 |
| $C_{oss}$ | Output Capacitance | — | 1360 | — | | $V_{GS}$ = 0V, $V_{DS}$ = 1.0V, ƒ = 1.0MHz |
| $C_{oss}$ | Output Capacitance | — | 31 | — | | $V_{GS}$ = 0V, $V_{DS}$ = 400V, ƒ = 1.0MHz |
| $C_{oss}$ eff. | Effective Output Capacitance | — | 75 | — | | $V_{GS}$ = 0V,$V_{DS}$ = 0V to 400V ⑤ |
| $C_{oss}$ eff. (ER) | Effective Output Capacitance (Energy Related) | — | 55 | — | | |

## Avalanche Characteristics

| Symbol | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $E_{AS}$ | Single Pulse Avalanche Energy② | — | 140 | mJ |
| $I_{AR}$ | Avalanche Current ① | — | 4.0 | A |
| $E_{AR}$ | Repetitive Avalanche Energy ① | — | 3.0 | mJ |

## Thermal Resistance

| Symbol | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case | — | 3.0 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient | — | 65 | |

**Notes:**

① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11).

② Starting $T_J$ = 25°C, L = 18mH, $R_G$ = 25Ω, $I_{AS}$ = 4.0A, dv/dt = 13V/ns. (See Figure 12a).

③ $I_{SD} \leq$ 4.0, di/dt ≤ 280A/μs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 150°C.

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

⑤ $C_{oss}$ eff. is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.
$C_{oss}$ eff.(ER) is a fixed capacitance that stores the same energy as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.

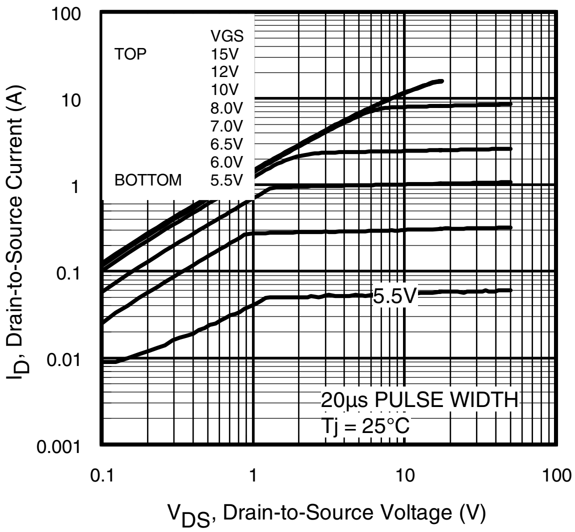



**Fig 1.** Typical Output Characteristics

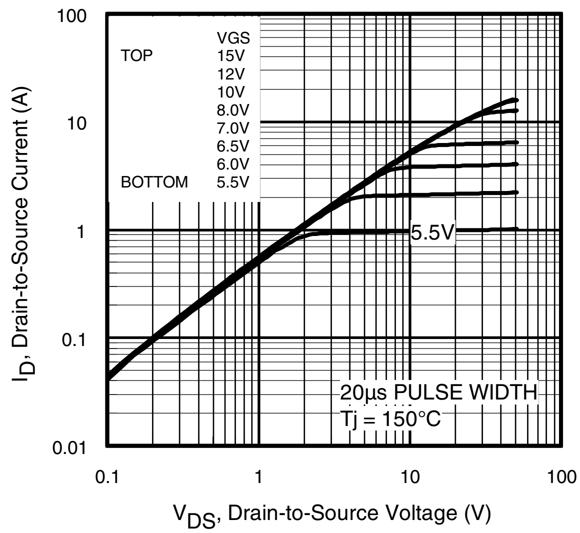



**Fig 2.** Typical Output Characteristics

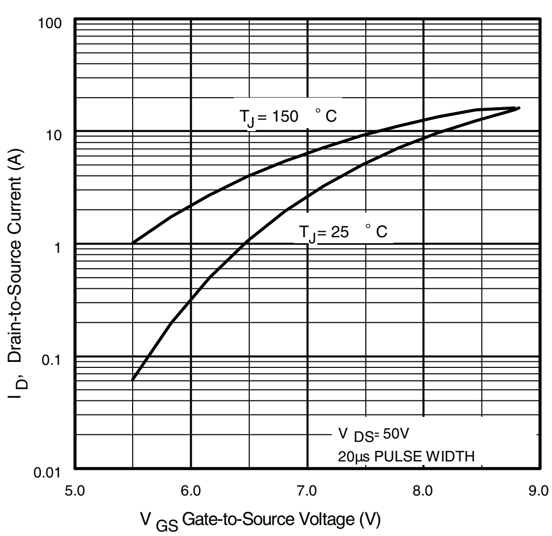



**Fig 3.** Typical Transfer Characteristics

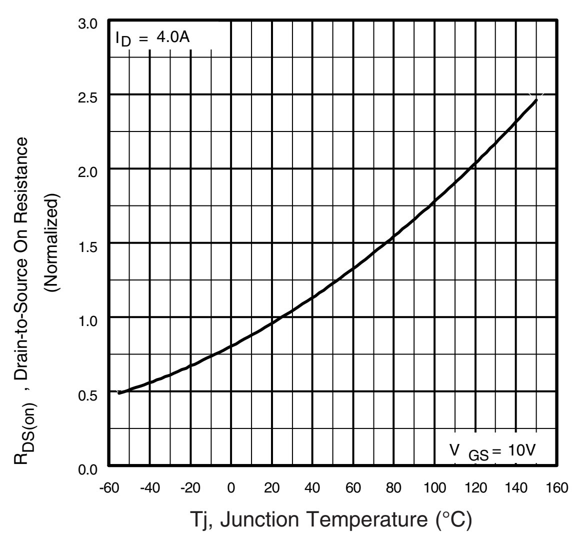



**Fig 4.** Normalized On-Resistance vs. Temperature

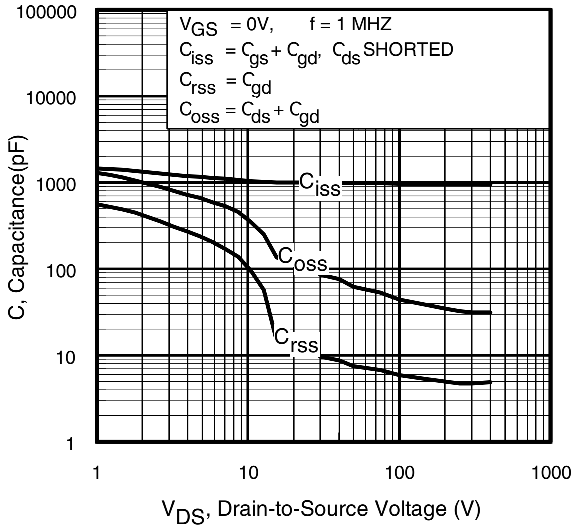



**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage

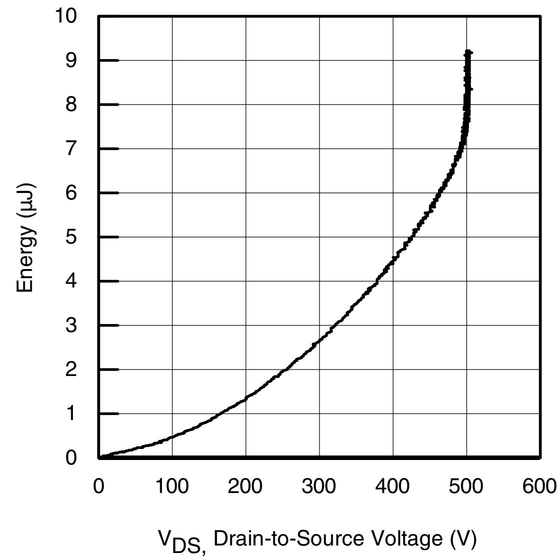



**Fig 6.** Typ. Output Capacitance Stored Energy vs. $V_{DS}$

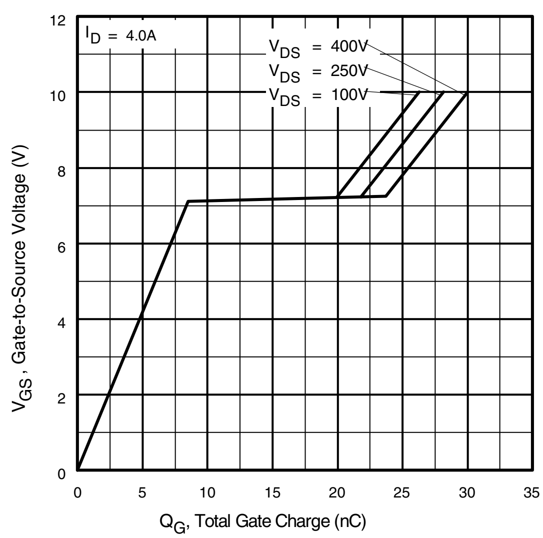



**Fig 7.** Typical Gate Charge vs. Gate-to-Source Voltage

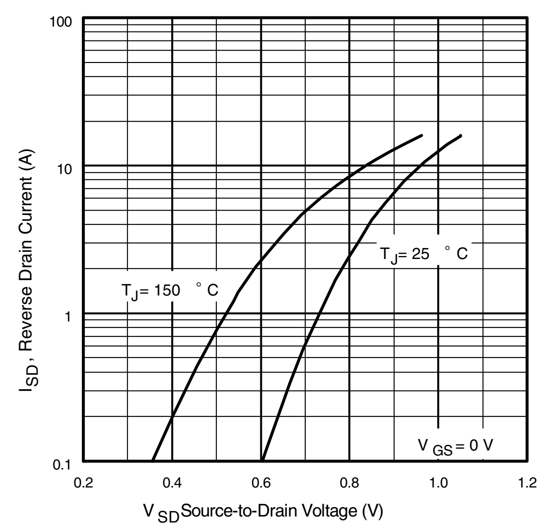



**Fig 8.** Typical Source-Drain Diode Forward Voltage

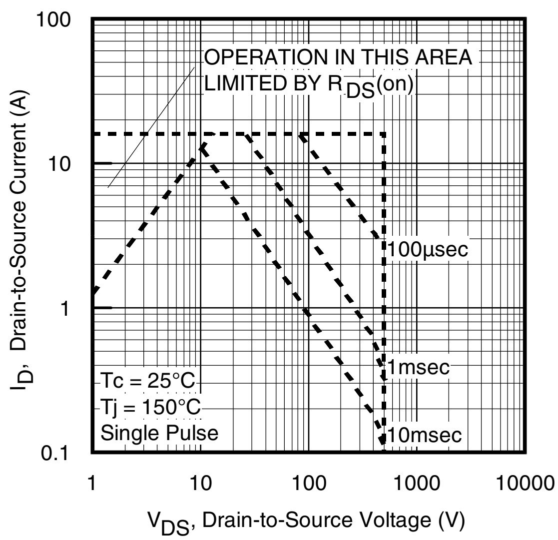



**Fig 9.** Maximum Safe Operating Area

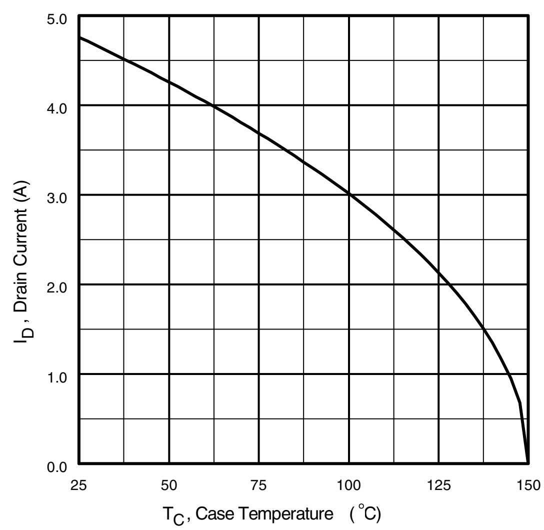



**Fig 10.** Maximum Drain Current vs. Case Temperature

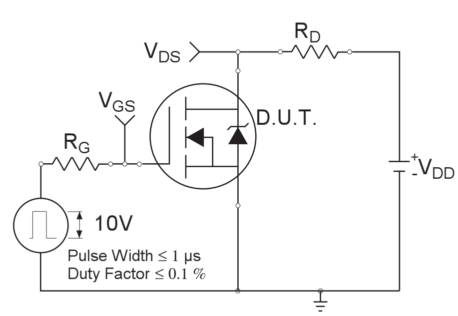



**Fig 11a.** Switching Time Test Circuit

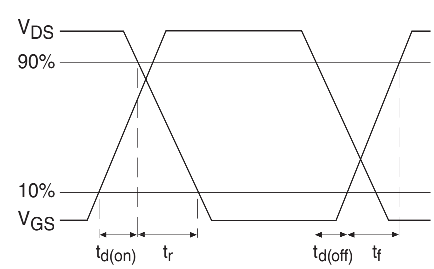



**Fig 11b.** Switching Time Waveforms

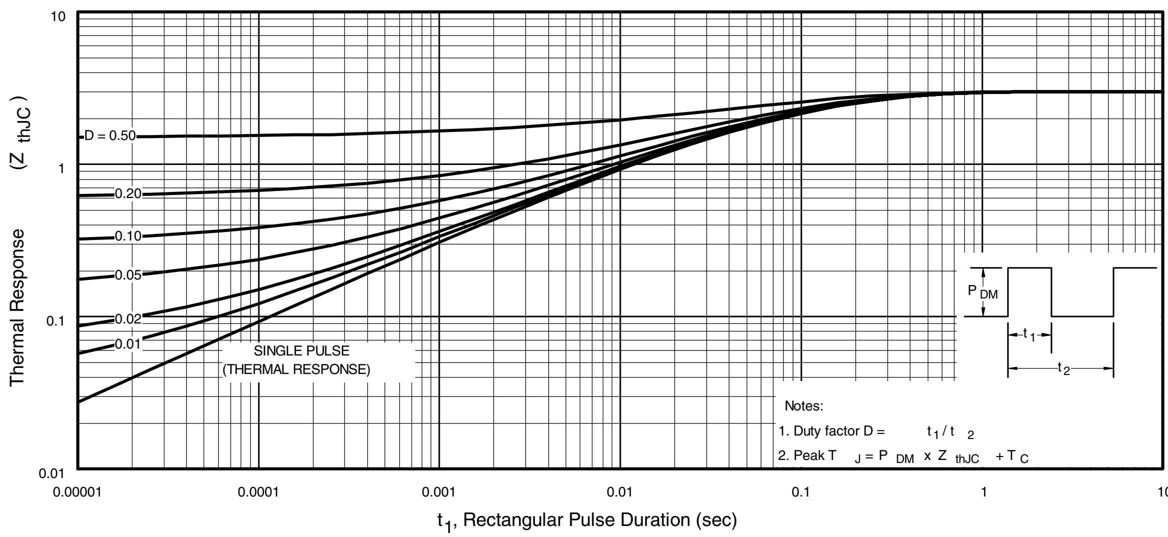



**Fig 12.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

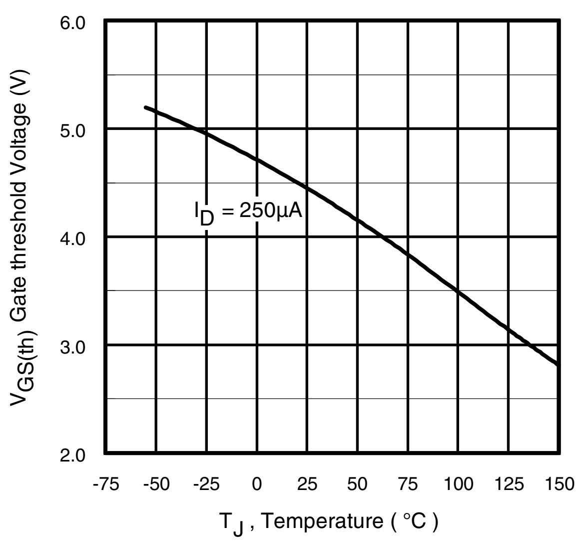



**Fig 13.** Threshold Voltage vs.Temperature

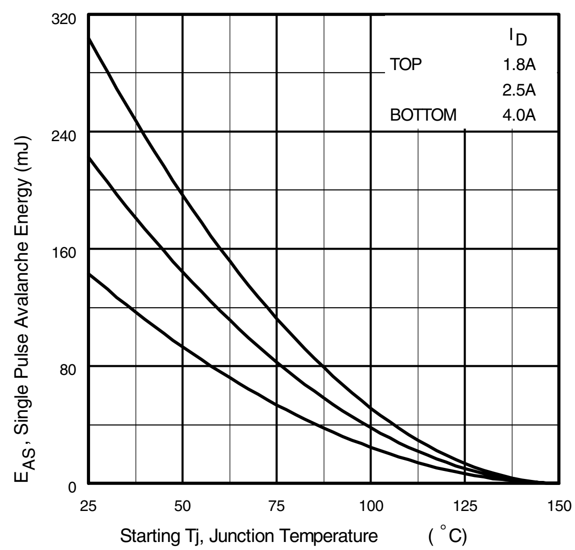



**Fig 14.** Maximum Avalanche Energy vs. Drain Current

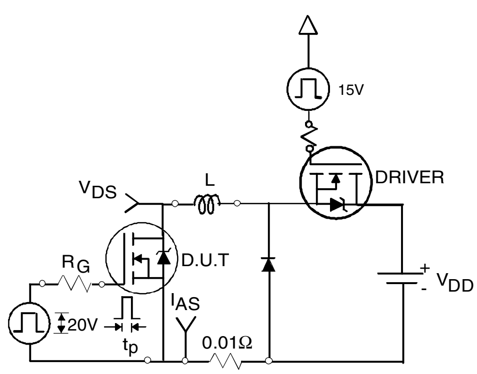



**Fig 15a.** Unclamped Inductive Test Circuit

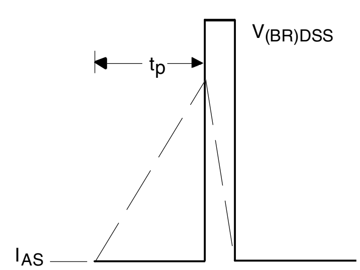



**Fig 15b.** Unclamped Inductive Waveforms

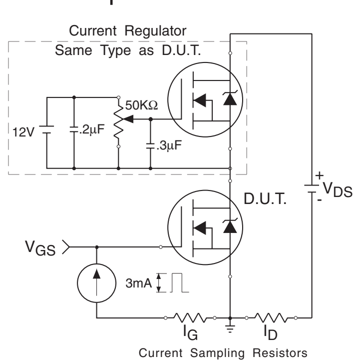



**Fig 16a.** Gate Charge Test Circuit

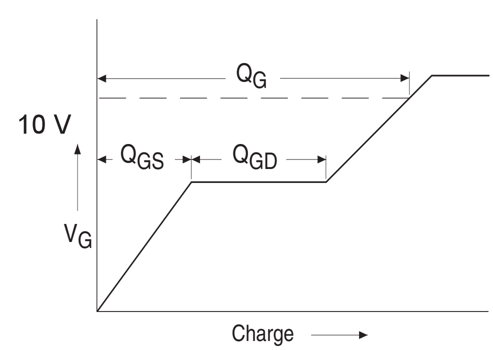
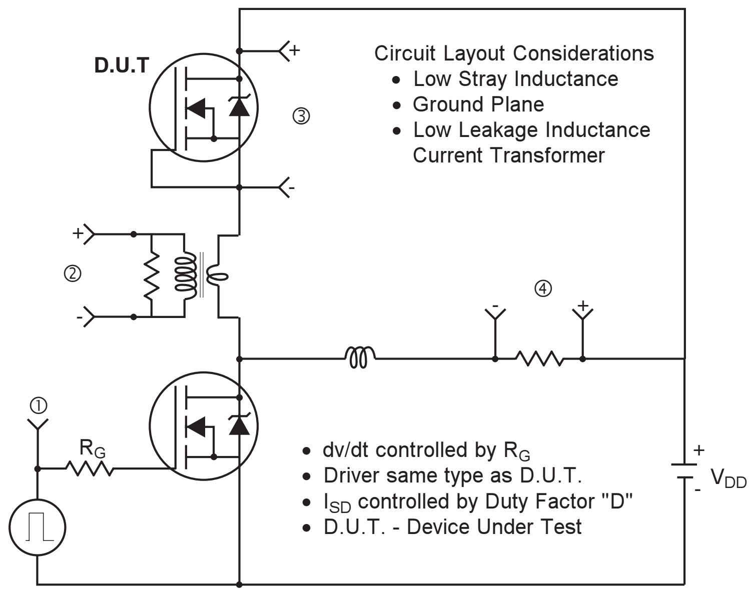
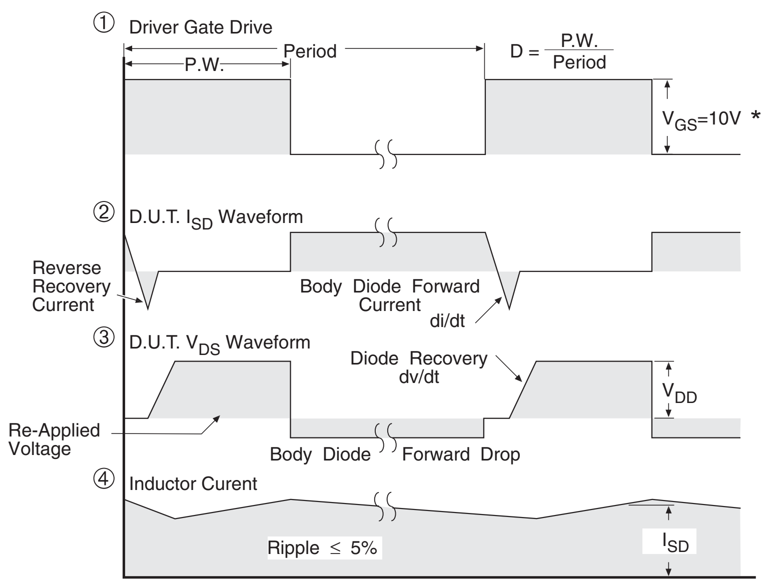



**Fig 16b.** Basic Gate Charge Waveform

## Peak Diode Recovery dv/dt Test Circuit



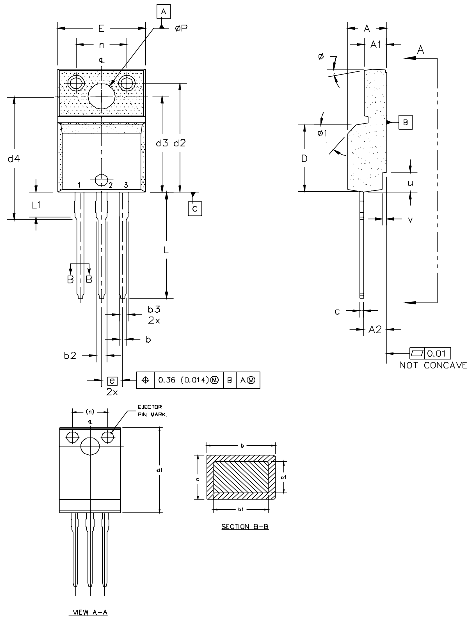




* $V_{GS}$ = 5V for Logic Level Devices

**Fig 17.** For N-Channel HEXFET® Power MOSFETs

## TO-220 Full-Pak Package Outline

Dimensions are shown in millimeters (inches)



NOTES:
1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3.0 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
4.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5.0 DIMENSION b1 APPLY TO BASE METAL ONLY.
6.0 STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.
7.0 CONTROLLING DIMENSION : INCHES.

| SYMBOL | DIMENSIONS | | | | NOTES |
|---|---|---|---|---|---|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 4 57 | 4.83 | 0.180 | 0.190 | |
| A1 | 2.57 | 2.83 | 0.101 | 0.114 | |
| A2 | 2.51 | 2.85 | 0.099 | 0.112 | |
| b | 0.622 | 0.89 | 0.024 | 0.035 | |
| b1 | 0.622 | 0.838 | 0.024 | 0.033 | 5 |
| b2 | 1.229 | 1.400 | 0.048 | 0.055 | |
| b3 | 1.229 | 1.400 | 0.048 | 0.055 | |
| c | 0 440 | 0.629 | 0.017 | 0.025 | |
| c1 | 0 440 | 0.584 | 0.017 | 0.023 | |
| D | 8.65 | 9.80 | 0.341 | 0.386 | 4 |
| d1 | 15.80 | 16.12 | 0.622 | 0.635 | |
| d2 | 13.97 | 14.22 | 0.550 | 0.560 | |
| d3 | 12.30 | 12.92 | 0.484 | 0.509 | |
| d4 | 8.64 | 9.91 | 0.340 | 0.390 | |
| E | 10.36 | 10.63 | 0.408 | 0.419 | 4 |
| e | 2.54 BSC | | 0.100 BSC | | |
| L | 13 20 | 13.73 | 0.520 | 0 541 | |
| L1 | 3.10 | 3.50 | 0.122 | 0.138 | 3 |
| n | 6.05 | 6.15 | 0.238 | 0.242 | |
| øP | 3.05 | 3.45 | 0.120 | 0.136 | |
| u | 2.40 | 2.50 | 0.094 | 0.098 | 6 |
| v | 0.40 | 0.50 | 0.016 | 0.020 | 6 |
| ø | 3° | 7° | 3° | 7° | |
| ø1 | | 45° | | 45° | |

LEAD ASSIGNMENTS

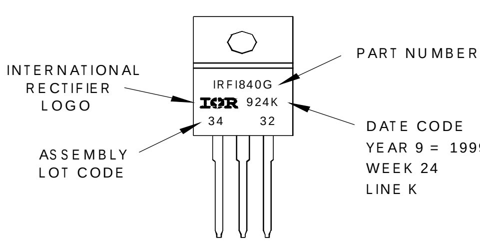
HEXFET
1.- GATE
2.- DRAIN
3.- SOURCE

IGBTs, CoPACK
1.- GATE
2.- COLLECTOR
3.- EMITTER

## TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRFI840G
WITH ASSEMBLY
LOT CODE 3432
ASSEMBLED ON WW 24 1999
IN THE ASSEMBLY LINE "K"

**Note:** "P" in assembly line position indicates "Lead-Free"




**TO-220AB FullPak package is not recommended for Surface Mount Application.**

Data and specifications subject to change without notice.
This product has been designed and qualified for the Automotive [Q101] market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

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06/04

# Notice

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