

## 3.3 V Dual LVTTTL/LVCMOS to Differential LVPECL Buffer

### FEATURES

- Dual 3.3V LVTTTL to LVPECL Buffer
- Operating Range
  - LVPECL  $V_{CC} = 3.0\text{ V to }3.6\text{ V}$  With  $GND = 0\text{ V}$
- Support for Clock Frequencies to 2.0 GHz (typ)
- 420 ps Typical Propagation Delay
- Deterministic HIGH Output Value for Open Input Conditions
- Built-in Temperature Compensation
- Drop in Compatible to MC100ELT23
- PNP Single Ended Inputs for Minimal Loading

### PINOUT ASSIGNMENT

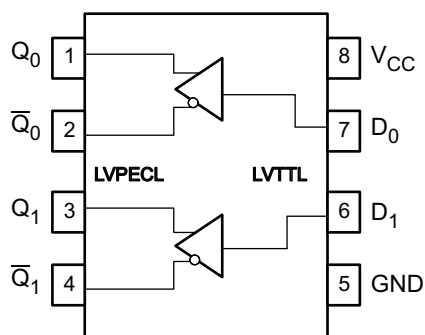


Table 1. Pin Description

PIN	FUNCTION
$D_0, D_1$	LVTTTL data inputs
$Q_0, \bar{Q}_0, Q_1, \bar{Q}_1$	LVPECL outputs
$V_{CC}$	Positive supply
GND	Ground

### ORDERING INFORMATION<sup>(1)</sup>

PART NUMBER	PART MARKING	PACKAGE	LEAD FINISH
SN65EPT22D	SN65EPT22	SOIC	NiPdAu
SN65EPT22DGK	SN65EPT22	SOIC-TSSOP	NiPdAu

(1) Leaded device options not initially available. Contact sales representative for further details.



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

PARAMETER	CONDITION	VALUE	UNIT
Absolute supply voltage, $V_{CC}$		6	V
Absolute input voltage, $V_I$	$GND = 0$ and $V_I \leq V_{CC}$	0 to 6	V
Supply voltage LVPEL		3.3	V
Output current	Continuous	50	mA
	Surge	100	
Operating temperature range		–40 to 85	°C
Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## POWER DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	POWER RATING $T_A < 25^\circ\text{C}$ (mW)	THERMAL RESISTANCE, JUNCTION TO AMBIENT NO AIRFLOW	DERATING FACTOR $T_A > 25^\circ\text{C}$ (mW/°C)	POWER RATING $T_A = 85^\circ\text{C}$ (mW)
SOIC	Low-K	719	139	7	288
	High-K	840	119	8	336
SOIC-TSSOP	Low-K	469	213	5	188
	High-K	527	189	5	211

## THERMAL CHARACTERISTICS

PARAMETER		PACKAGE	VALUE	UNIT
$\theta_{JB}$	Junction-to Board Thermal Resistance	SOIC	79	°C/W
		SOIC-TSSOP	120	
$\theta_{JC}$	Junction-to Case Thermal Resistance	SOIC	98	°C/W
		SOIC-TSSOP	74	

## KEY ATTRIBUTES

CHARACTERISTICS	VALUE
Moisture sensitivity level	Lead free package
	SOIC-8
	TSSOP-8
Flammability rating (Oxygen Index: 28 to 34)	UL 94 V-0 at 0.125 in
ESD-HBM	4 kV
ESD-machine model	200 V
ESD-charge device model	2 kV
Meets or exceeds JEDEC Spec EIA/JESD78 latchup test	

**TTL INPUT DC CHARACTERISTICS<sup>(1)</sup> ( $V_{CC} = 3.3\text{ V}$ ,  $GND = 0$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ )**

CHARACTERISTIC		CONDITION	MIN	TYP	MAX	UNIT
$I_{IH}$	Input HIGH current	$V_{IN} = 2.7\text{ V}$			20	$\mu\text{A}$
$I_{IHH}$	Input HIGH current max	$V_{IN} = V_{CC}$			100	$\mu\text{A}$
$I_{IL}$	Input LOW current	$V_{IN} = 0.5\text{ V}$			-0.6	$\text{mA}$
$V_{IK}$	Input clamp voltage	$I_{IN} = -18\text{ mA}$			-1	$\text{V}$
$V_{IH}$	Input high voltage		2.0			$\text{V}$
$V_{IL}$	Input low voltage				0.8	$\text{V}$

- (1) Device will meet the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

**PECL OUTPUT DC CHARACTERISTICS<sup>(1)</sup> ( $V_{CC} = 3.3\text{ V}$ ;  $GND = 0.0\text{V}$ )<sup>(2)</sup>**

CHARACTERISTIC	$-40^\circ\text{C}$			$25^\circ\text{C}$			$85^\circ\text{C}$			UNIT	
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
$I_{CC}$	Power supply current	39	45	42	47	45	50			$\text{mA}$	
$V_{OH}$	Output HIGH voltage <sup>(3)</sup>	2155	2224	2405	2155	2224	2405	2155	2224	2405	$\text{mV}$
$V_{OL}$	Output LOW voltage <sup>(3)</sup>	1355	1441	1605	1355	1438	1605	1355	1435	1605	$\text{mV}$

- (1) Device will meet the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
- (2) Output parameters vary 1:1 with  $V_{CC}$
- (3) All loading with  $50\Omega$  to  $V_{CC} - 2.0\text{V}$

**AC CHARACTERISTICS<sup>(1)</sup> ( $V_{CC} = 3.0\text{ V}$  to  $3.6\text{ V}$ ;  $GND = 0\text{ V}$ )<sup>(2)</sup>**

CHARACTERISTIC	$-40^\circ\text{C}$			$25^\circ\text{C}$			$85^\circ\text{C}$			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$f_{MAX}$	Max switching frequency <sup>(3)</sup> , see <a href="#">Figure 5</a>	2.1		2.0		2.0				$\text{GHz}$
$t_{PLH} / t_{PHL}$	Propagation delay to differential output	230	550	230	550	230	550			$\text{ps}$
$t_{SKEW}$	Within device skew <sup>(4)</sup>	25	50	25	50	25	50			$\text{ps}$
	Device to device skew <sup>(5)</sup>	100	200	100	200	100	200			$\text{ps}$
$t_{JITTER}$	Random clock jitter (RMS)	0.2	0.8	0.2	0.8	0.2	0.8			$\text{ps}$
$t_r / t_f$	Output rise/fall times (20%–80%)	150	300	150	300	150	300			$\text{ps}$

- (1) Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
- (2) Measured using a 2.4 V source, 50% duty cycle clock source. All loading with  $50\Omega$  to  $V_{CC} - 2.0\text{ V}$ .
- (3) Maximum switching frequency measured at output amplitude of  $300\text{ mV}_{pp}$ .
- (4) Skew is measured between outputs under identical transitions and conditions on any one device.
- (5) Device-to-Device Skew for identical transitions at identical VCC levels.

Typical Termination for Output Driver

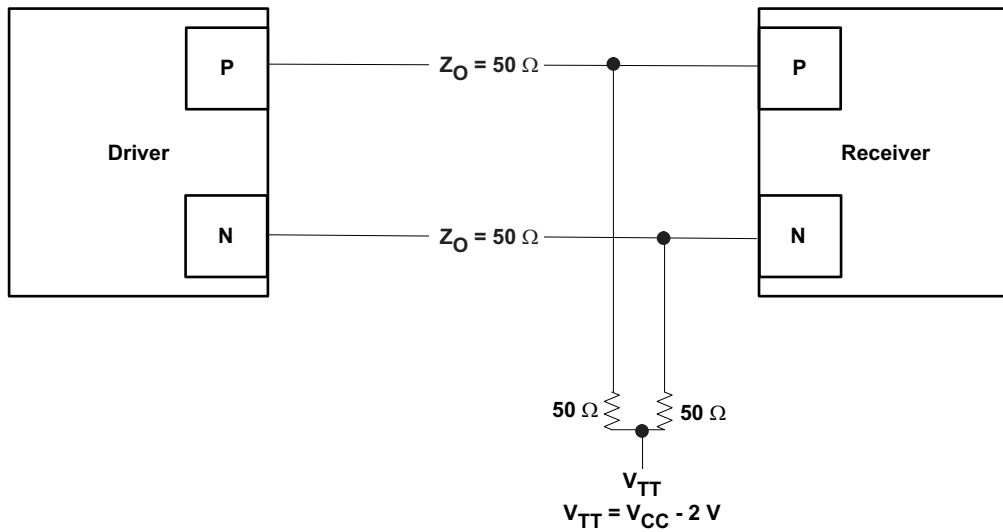


Figure 1. Termination for Output Driver

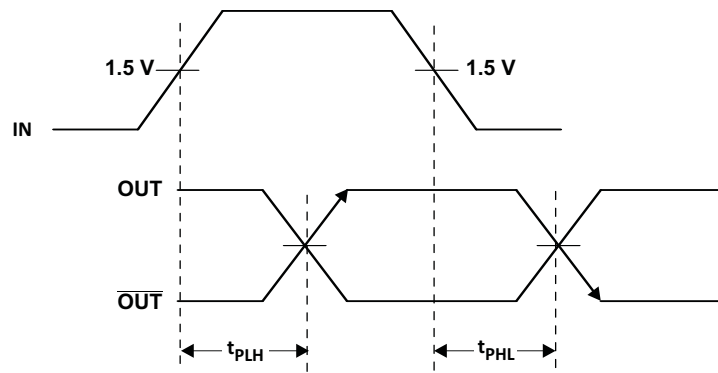


Figure 2. Output Propagation Delay

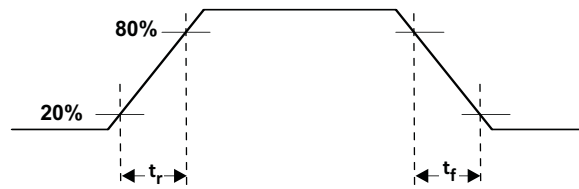


Figure 3. Output Rise and Fall Times

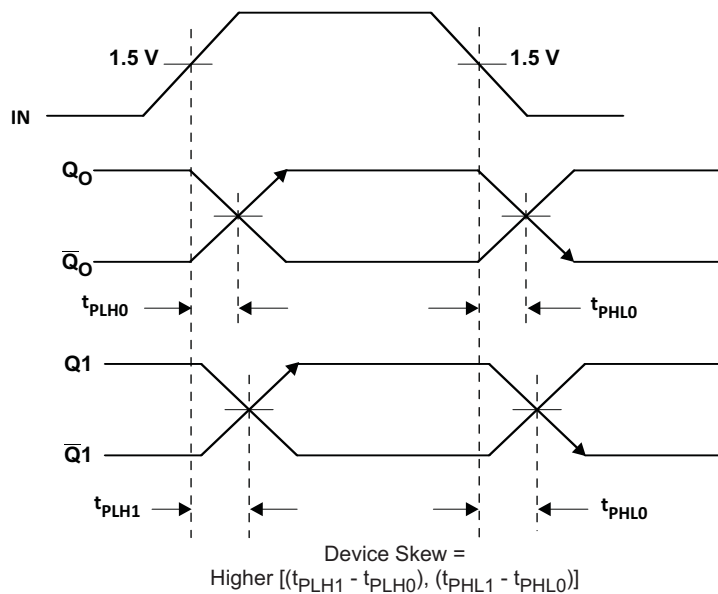


Figure 4. Device Skew

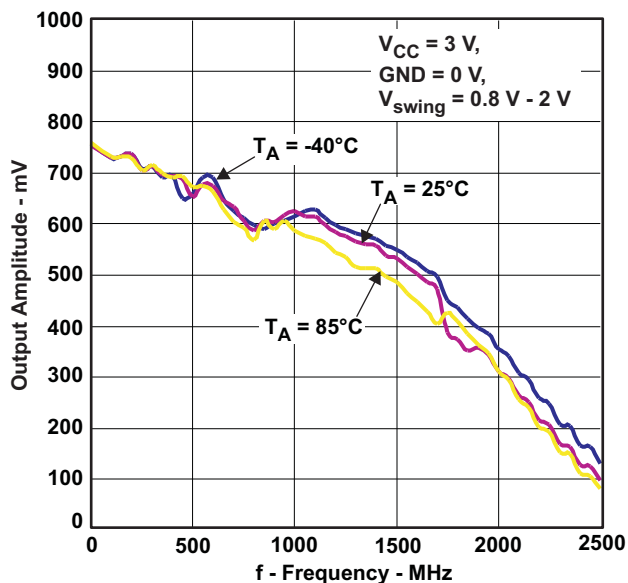


Figure 5. Output Amplitude versus Frequency

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65EPT22DGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65EPT22DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65EPT22DGKR	MSOP	DGK	8	2500	346.0	346.0	29.0
SN65EPT22DR	SOIC	D	8	2500	346.0	346.0	29.0

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

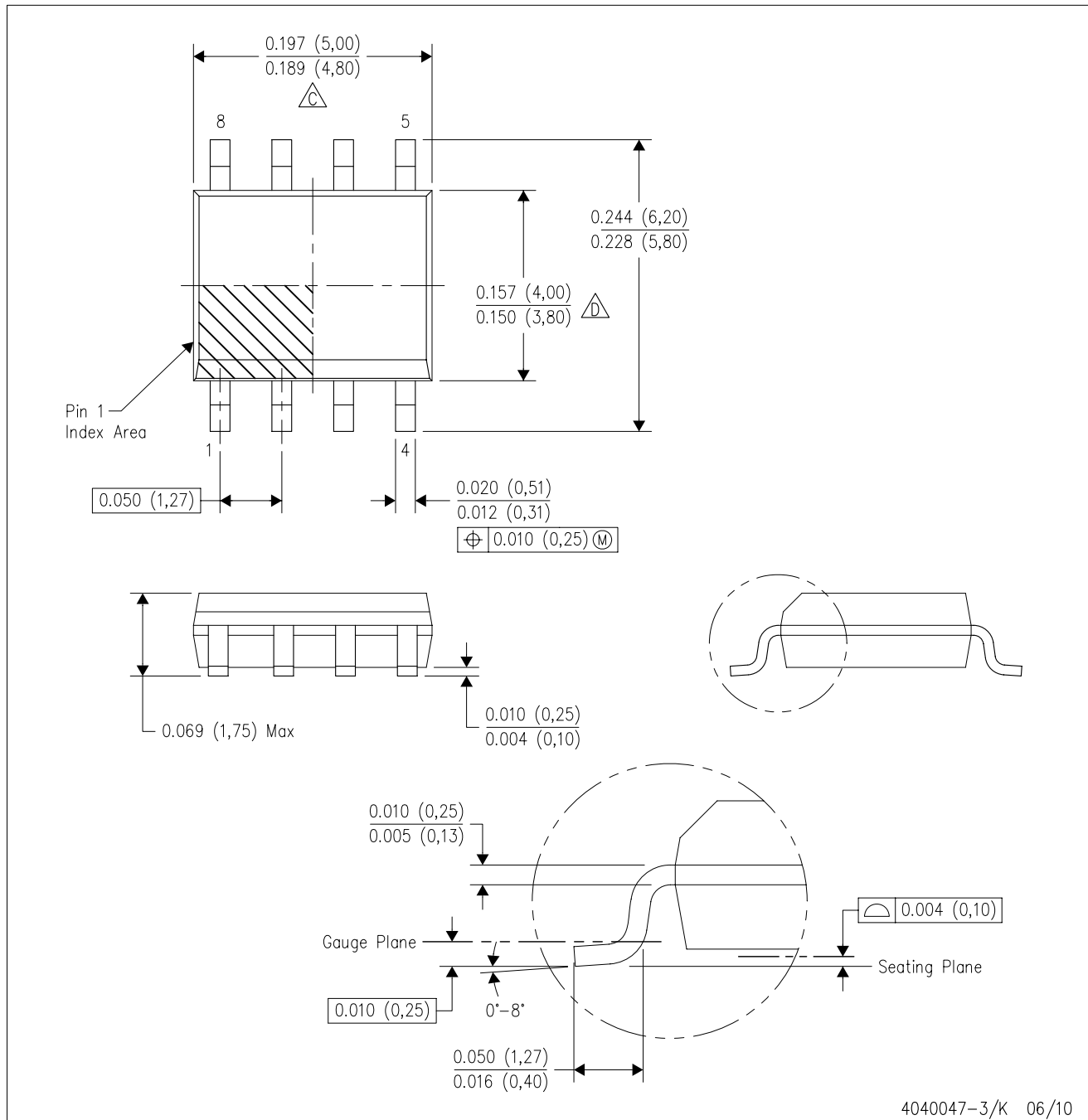


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



D (R-PDSO-G8)

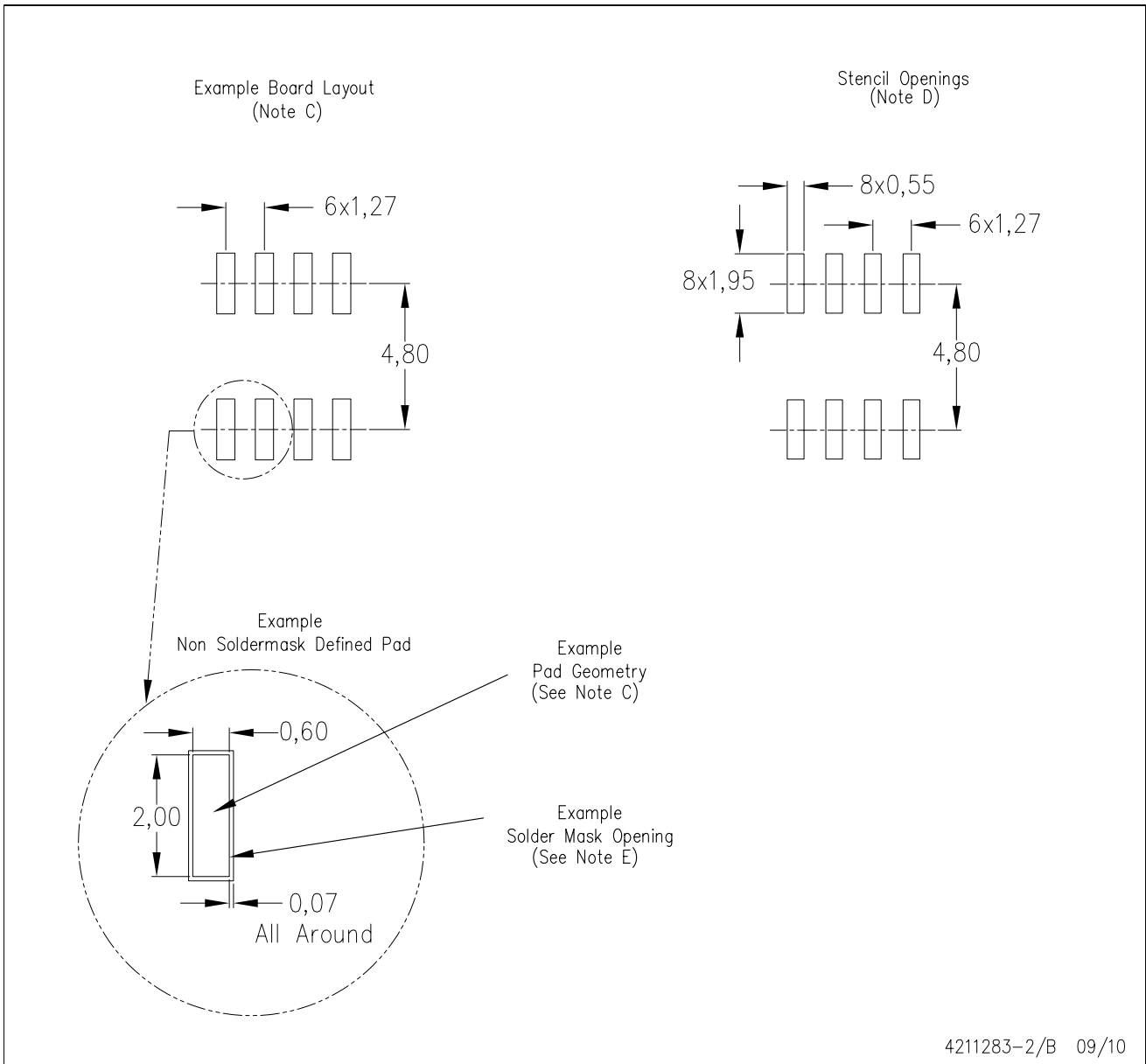
PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.  
 D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.  
 E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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