

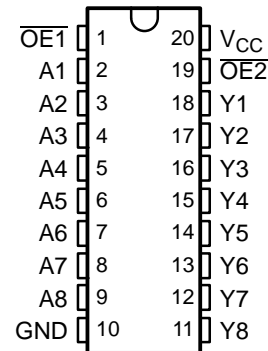
FEATURES

- Controlled Baseline
 - One Assembly/Test Site, One Fabrication Site
- Extended Temperature Performance of -40°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree ⁽¹⁾
- Operates From 2 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 5.1 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at $V_{CC} = 3.3$ V, $T_A = 25^{\circ}\text{C}$

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- I_{off} Supports Partial-Power-Down Mode Operation

DW OR PW PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The SN74LVC541A-EP octal buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The device is ideal for driving bus lines or buffering memory address registers.

This device features inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that, if either output enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all eight outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

| T_A | PACKAGE ⁽¹⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|--|------------------------|--------------|-----------------------|------------------|
| -40°C to 125°C | SOIC – DW | Reel of 2000 | SN74LVC541AQDWREP | C541AEP |
| | TSSOP – PW | Reel of 2000 | SN74LVC541AQPWREP | C541AEP |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

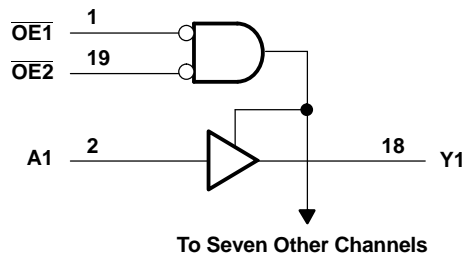
SN74LVC541A-EP OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS748A–DECEMBER 2003–REVISED AUGUST 2005

FUNCTION TABLE

| INPUTS | | | OUTPUT Y |
|------------------|------------------|---|-------------|
| $\overline{OE1}$ | $\overline{OE2}$ | A | |
| L | L | L | L |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---------------|---|------------|----------------|---------|
| V_{CC} | Supply voltage range | -0.5 | 6.5 | V |
| V_I | Input voltage range ⁽²⁾ | -0.5 | 6.5 | V |
| V_O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | -0.5 | 6.5 | V |
| V_O | Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾ | -0.5 | $V_{CC} + 0.5$ | V |
| I_{IK} | Input clamp current | $V_I < 0$ | | -50 mA |
| I_{OK} | Output clamp current | $V_O < 0$ | | -50 mA |
| I_O | Continuous output current | | | ±50 mA |
| | Continuous current through V_{CC} or GND | | | ±100 mA |
| θ_{JA} | Package thermal impedance ⁽⁴⁾ | DW package | | 58 °C/W |
| | | PW package | | 83 °C/W |
| T_{stg} | Storage temperature range ⁽⁵⁾ | -65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

Recommended Operating Conditions⁽¹⁾

| | | | MIN | MAX | UNIT |
|-----------------|--------------------------------|----------------------------------|-----|-----------------|------|
| V _{CC} | Supply voltage | Operating | 2 | 3.6 | V |
| | | Data retention only | 1.5 | | |
| V _{IH} | High-level input voltage | V _{CC} = 2.7 V to 3.6 V | 2 | | V |
| V _{IL} | Low-level input voltage | V _{CC} = 2.7 V to 3.6 V | | 0.8 | V |
| V _I | Input voltage | | 0 | 5.5 | V |
| V _O | Output voltage | High or low state | 0 | V _{CC} | V |
| | | 3-state | 0 | 5.5 | |
| I _{OH} | High-level output current | V _{CC} = 2.7 V | | -12 | mA |
| | | V _{CC} = 3 V | | -24 | |
| I _{OL} | Low-level output current | V _{CC} = 2.7 V | | 12 | mA |
| | | V _{CC} = 3 V | | 24 | |
| T _A | Operating free-air temperature | | -40 | 125 | °C |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V _{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|------------------|--|--|-----------------|-----------------------|--------------------|-----|------|
| V _{OH} | I _{OH} = -100 μA | | 2.7 V to 3.6 V | V _{CC} - 0.2 | | V | |
| | I _{OH} = -12 mA | | 2.7 V | 2.2 | | | |
| | | | 3 V | 2.4 | | | |
| | I _{OH} = -24 mA | | 3 V | 2.2 | | | |
| V _{OL} | I _{OL} = 100 μA | | 2.7 V to 3.6 V | 0.2 | | V | |
| | I _{OL} = 12 mA | | 2.7 V | 0.4 | | | |
| | I _{OL} = 24 mA | | 3 V | 0.55 | | | |
| I _I | V _I = 0 to 5.5 V | | 3.6 V | ±5 | | μA | |
| I _{OZ} | V _O = 0 to 5.5 V | | 3.6 V | ±15 | | μA | |
| I _{CC} | V _I = V _{CC} or GND | | 3.6 V | 10 | | μA | |
| | 3.6 V ≤ V _I ≤ 5.5 V ⁽²⁾ | | | 10 | | | |
| ΔI _{CC} | One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND | | 2.7 V to 3.6 V | 500 | | μA | |
| C _i | V _I = V _{CC} or GND | | 3.3 V | 4 | | pF | |
| C _o | V _O = V _{CC} or GND | | 3.3 V | 5.5 | | pF | |

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(2) This applies in the disabled state only.

SN74LVC541A-EP
OCTAL BUFFER/DRIVER
WITH 3-STATE OUTPUTS

SCAS748A–DECEMBER 2003–REVISED AUGUST 2005

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

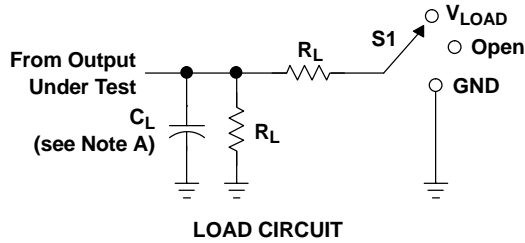
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 2.7 V | | V _{CC} = 3.3 V ± 0.3 V | | UNIT |
|------------------|------------------------|----------------|-------------------------|-----|------------------------------------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| t _{pd} | A | Y | | 5.6 | 1 | 5.1 | ns |
| t _{en} | $\overline{\text{OE}}$ | Y | | 7.5 | 1 | 7 | ns |
| t _{dis} | $\overline{\text{OE}}$ | Y | | 7.7 | 1 | 7 | ns |

Operating Characteristics

T_A = 25°C

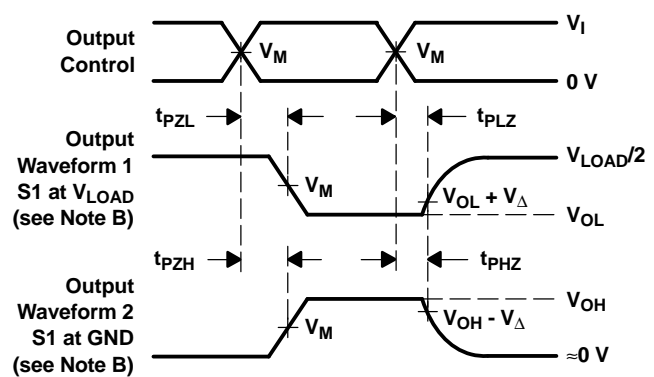
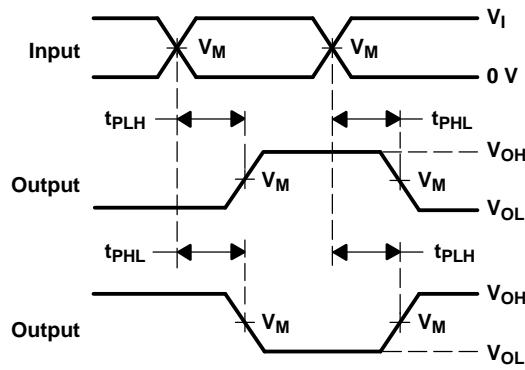
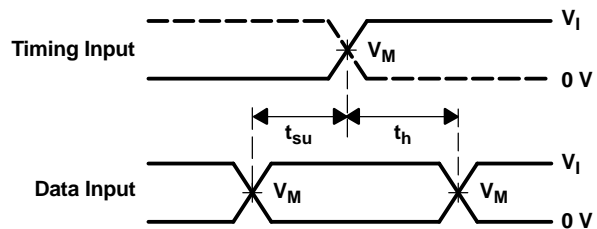
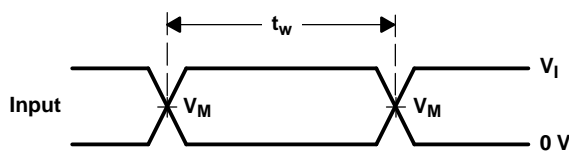
| PARAMETER | | TEST CONDITIONS | V _{CC} = 2.5 V | V _{CC} = 3.3 V | UNIT |
|-----------------|---|--------------------|-------------------------|-------------------------|------|
| | | | TYP | TYP | |
| C _{pd} | Power dissipation capacitance per buffer/driver | Outputs enabled | 58 | 33 | pF |
| | | Outputs disabled | 2 | 2 | |

PARAMETER MEASUREMENT INFORMATION



| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|-------------------|--------|---------------|-------|------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| 2.7 V | 2.7 V | ≤ 2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| 3.3 V \pm 0.3 V | 2.7 V | ≤ 2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|-------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74LVC541AQDWREP | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC541AQPWREP | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| V62/04666-01XE | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| V62/04666-01YE | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LVC541A-EP :

- Catalog: [SN74LVC541A](#)
- Automotive: [SN74LVC541A-Q1](#)
- Military: [SN54LVC541A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC541AQDWREP | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.0 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LVC541AQPWREP | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC541AQDWREP | SOIC | DW | 20 | 2000 | 346.0 | 346.0 | 41.0 |
| SN74LVC541AQPWREP | TSSOP | PW | 20 | 2000 | 346.0 | 346.0 | 33.0 |

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

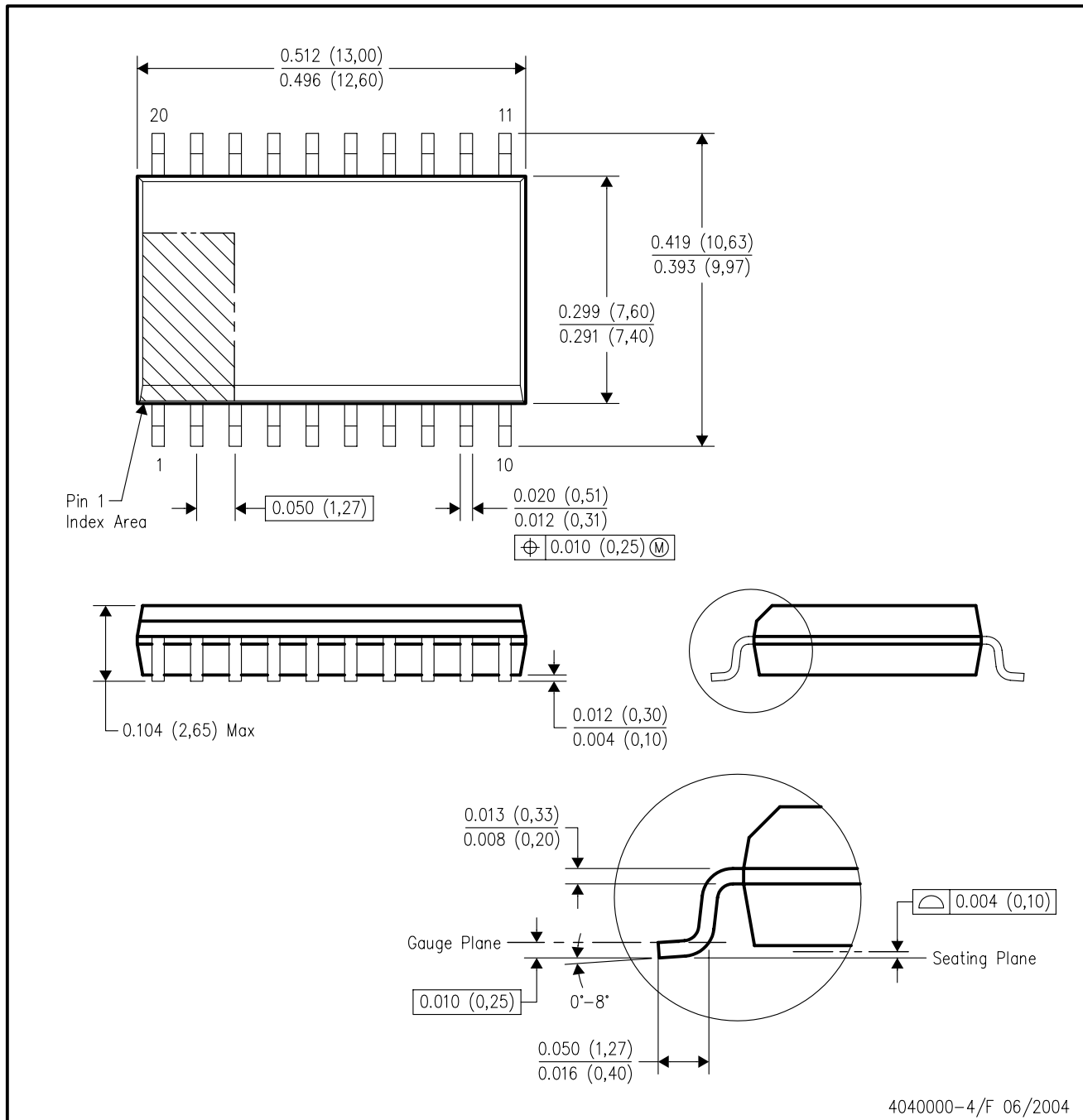


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- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

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