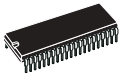
TDA7429L

3 BAND EQUALIZER AUDIO PROCESSOR WITH SUBWOOFER CONTR

1 FEATURES

- 3 STEREO INPUTS
- AUXILIARY MONO INPUT
- INPUT ATTENUATION CONTROL IN 0.5dB STEP
- TREBLE MIDDLE AND BASS CONTROL
  - FOUR SPEAKERS ATTENUATORS:
    - 4 INDEPENDENT SPEAKERS CONTROL IN 1dB STEPS FOR BALANCE FACILITY
    - INDEPENDENT MUTE FUNCTION
- SUBWOOFER OUTPUT (L+R) CONTROLLED IN 1dB STEP INPUTS
- ALL FUNCTIONS PROGRAMMABLE VIA SERIAL BUS

Figure 1. Package



SDIP42

Table 1. Order Codes

Part Number	Package
TDA7429L	SDIP42

2 DESCRIPTION

The TDA7429L is volume tone (bass middle and treble) balance (Left/Right) processors for quality audio applications in TV and Hi-Fi systems, providing also an additional subwoofer control.
The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers.
Thanks to the used BIPOLAR/CMOS Technology, Low Distortion, Low Noise and DC stepping are obtained.

Figure 2. Test Circuit

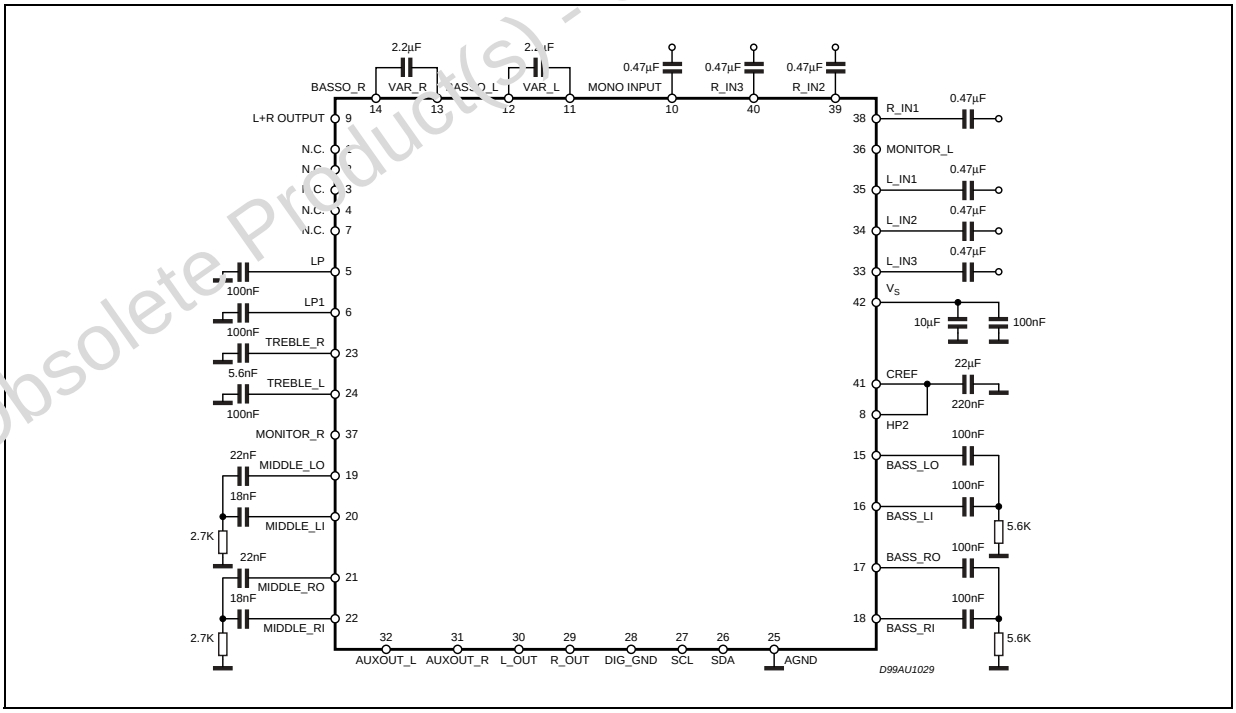


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_S	Operating Supply Voltage	5.5	V
T_{amb}	Operating Ambient Temperature	0 to 70	°C
T_{stg}	Storage Temperature Range	-55 to 150	°C

Figure 3. Pin Description

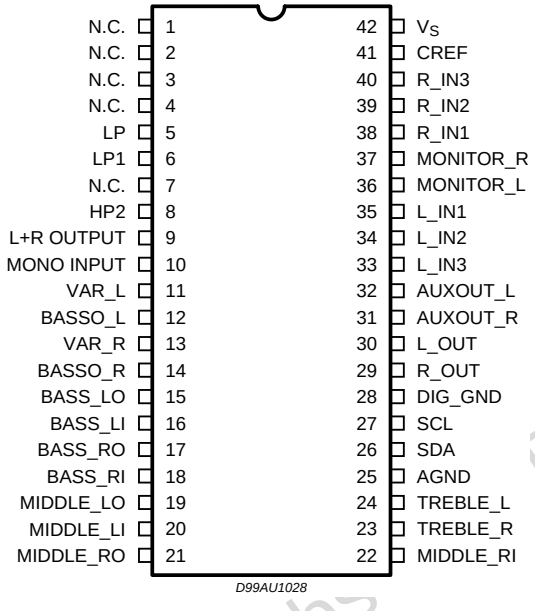


Table 3. Quick Reference Data

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_S	Supply Voltage	7	9	10.2	V
V_{CL}	Max Input Signal Handling	2			V_{RMS}
THD	Total Harmonic Distortion V = 0.1Vrms f = 1KHz		0.01	0.1	%
S/N	Signal to Noise Ratio V_{out} = 1Vrms (mode = OFF)		106		dB
S_C	Channel Separation f = 1KHz		90		dB
	Treble Control (2dB step)	-14		14	dB
	Middle Control (2dB step)	-14		14	dB
	Bass Control (2dB step)	-14		14	dB
	Balance Control 1dB step (LCH, RCH)	-79		0	dB
	Mute Attenuation		100		dB

Table 4. Thermal Data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}pin}$	Thermal Resistance Junction-pins	85	°C/W

Figure 4. Block Diagram

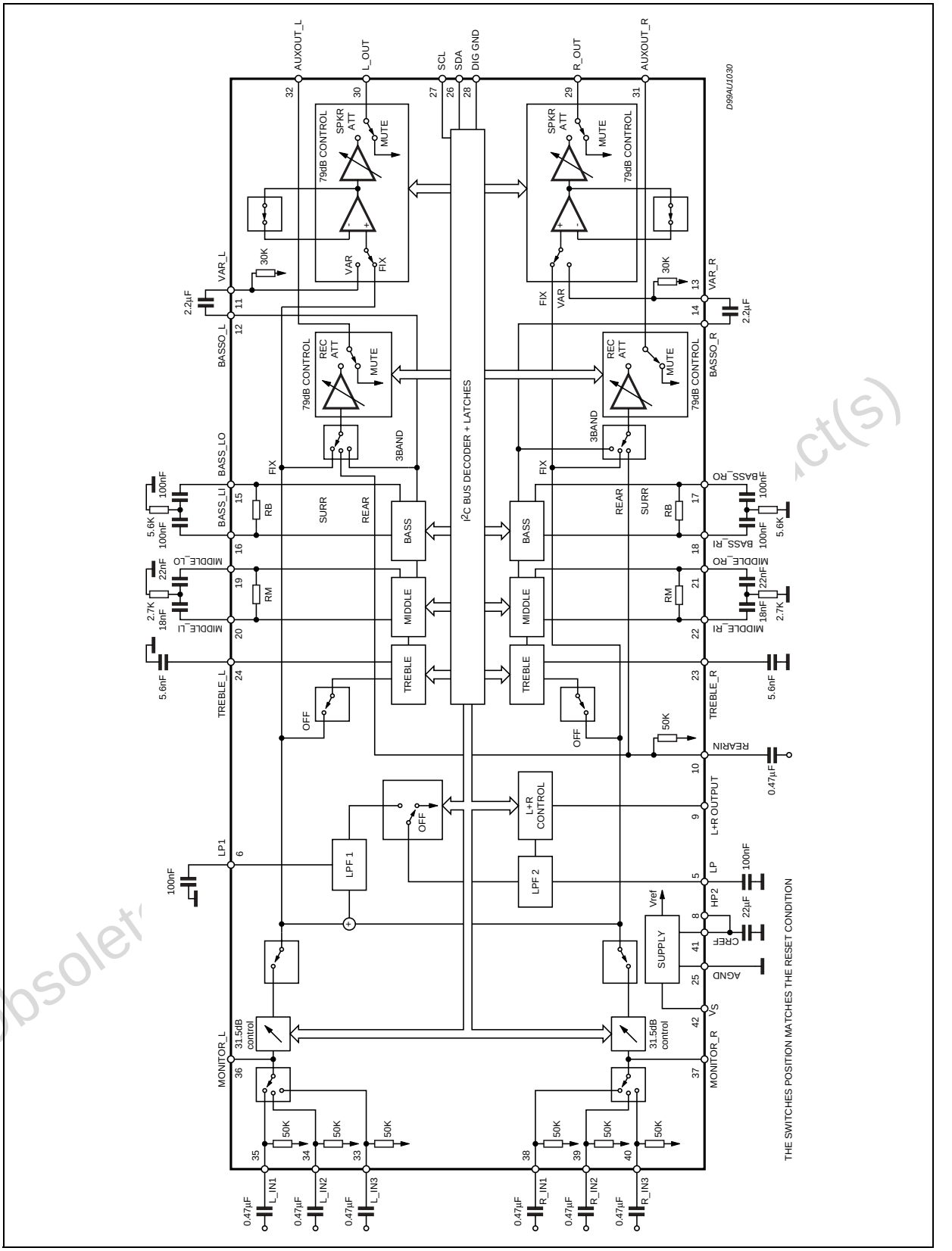


Table 5. Electrical Characteristcs (refer to the test circuit T_{amb} = 25°C, V_S = 9V, R_L = 10KΩ,Vin = 1Vrms; RG = 600Ω, all controls flat (G = 0dB), L+R CTRL = +4dB, MODE = OFF; f = 1KHz unless otherwise specified).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		7	9	10.2	V
I_S	Supply Current		10	18	26	mA
SVR	Ripple Rejection	L_{CH} / $R_{CH\ out}$, Mode = OFF	60	80		dB
INPUT STAGE						
R_{IN}	Input Resistance		35	50	65	KΩ
V_{CL}	Clipping Level	THD = 0.3%	2	2.5		V_{rms}
C_{RANGE}	Control Range			31.5		dB
A_{VMIN}	Min. Attenuation		-1	0	1	dB
A_{VMAX}	Max. Attenuation		31	31.5	32	dB
A_{STEP}	Step Resolution			0.5	1	dB
BASS CONTROL						
G_b	Control Range	Max. Boost/cut	±11.5	±14.0	±16.0	dB
B_{STEP}	Step Resolution		1	2	3	dB
R_B	Internal Feedback Resistance		32	44	56	KΩ
MIDDLE CONTROL						
G_m	Control Range	Max. Boost/cut	±11.5	±14.0	±16.0	dB
M_{STEP}	Step Resolution		1	2	3	dB
R_M	Internal Feedback Resistance		17.5	25	32.5	KΩ
TREBLE CONTROL						
G_t	Control Range	Max. Boost/cut	±13.0	±14.0	±15.0	dB
T_{STEP}	Step Resolution		1	2	3	dB
CONTROL L+R						
C_{RANGE}	Control Range		±11.5		±4	dB
S_{STEP}	Step Resolution		0.5	1	1.5	dB
SPEAKER & AUX ATTENUATORS						
C_{RANGE}	Control Range			79		dB
S_{STEP}	Step Resolution		-0.5	1	1.5	dB
E_A	Attenuation set error	A_v = 0 to -20dB	-1.5	0	1.5	dB
		A_v = -20 to -79dB	-3	0	2	dB

Table 5. Electrical Characteristcs (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DC}	DC Steps	adjacent att. steps	-3	0	3	mV
A_{MUTE}	Output Mute Condition		+70	100		dB
R_{VEA}	Input Impedance		21	30	39	KΩ
AUDIO OUTPUTS						
$N_{O(OFF)}$	Output Noise (OFF)	Output Mute, Flat BW = 20Hz to 20KHz		4 5		μV_{rms} μV_{rms}
d	Distorsion	A_v = 0 ; V_{in} = 1V_{rms}		0.01	0.1	%
S_C	Channel Separation		70	90		dB
V_{OCL}	Clipping Level	d = 0.3%	2	2.5		Vrms
R_{OUT}	Output Resistance		20	40	70	Ω
V_{OUT}	DC Voltage Level			3.8		V
MONITOR OUTPUTS						
d	Distorsion	A_v = 0 ; V_{in} = 1V_{rms}		0.01	0.1	%
S_C	Channel Separation		70	90		dB
V_{OCL}	Clipping Level	d = 0.3%	2	2.5		Vrms
R_{OUT}	Output Resistance		20	50	85	Ω
V_{OUT}	DC Voltage Level			4.5		V
BUS INPUTS						
V_{IL}	Input Low Voltage				1	V
V_{IH}	Input High Voltage		3			V
I_{IN}	Input Current		-5		+5	mA
V_O	Output Voltage SDA Acknowledge	I_O = 1.6mA			0.4	V

3 I²C BUS INTERFACE

Data transmission from microprocessor to the TDA7429L and viceversa takes place through the 2 wires I²C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

3.1 Data Validity

As shown in fig. 5, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

3.2 Start and Stop Conditions

As shown in fig.6 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

3.3 Byte Format

Every byte transferred on the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

3.4 Acknowledge

The master (mP) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 7). The peripheral (audioprocessor) that acknowledges has to pull-down (LOW) the SDA line during this clock pulse.

The audioprocessor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

3.5 Transmission without Acknowledge

Avoiding to detect the acknowledge of the audioprocessor, the µP can use a simpler transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.

This approach of course is less protected from misworking.

Figure 5. Data validity on the I²C bus

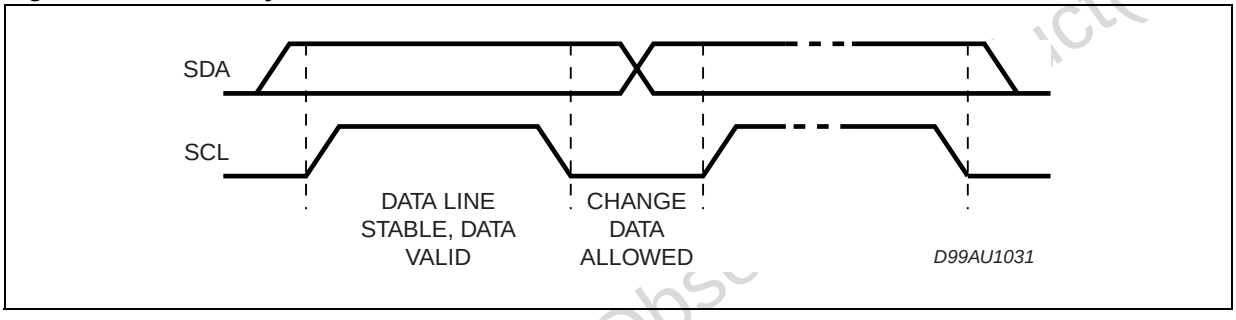


Figure 6. Timing Diagram of I²C bus

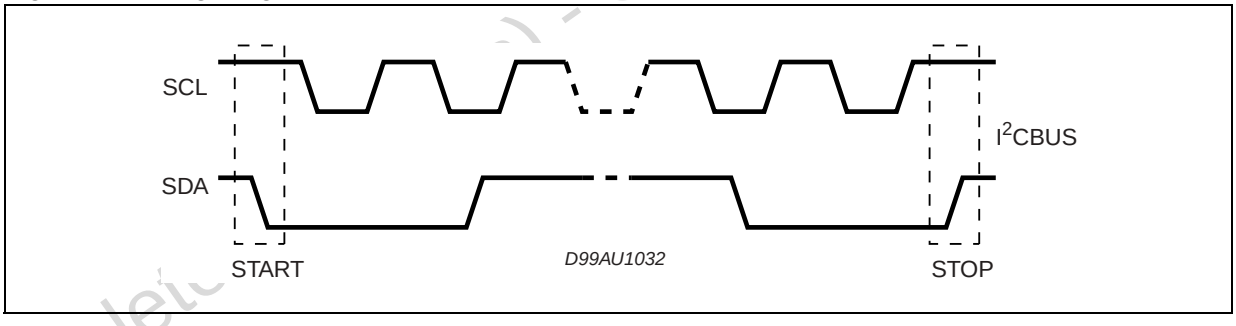
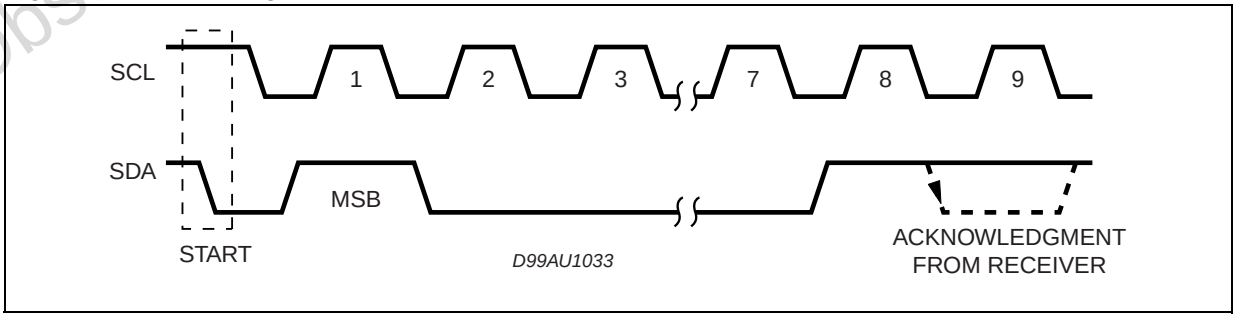


Figure 7. Acknowledge on the I²C bus



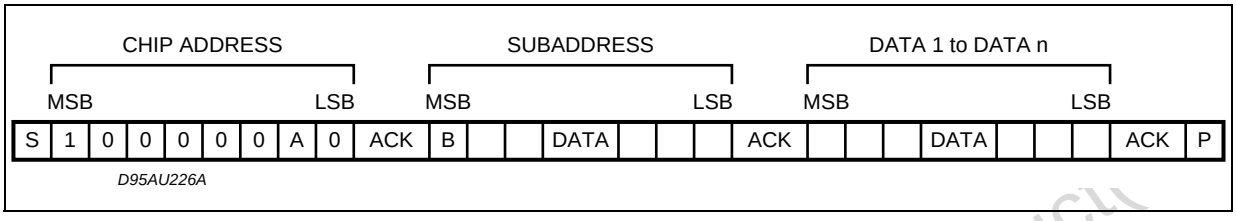
4 SOFTWARE SPECIFICATION

4.1 Interface Protocol

The interface protocol comprises:

- A start condition (S)
- A chip address byte, containing the TDA7429L address
- A subaddress bytes
- A sequence of data (N byte + achnowledge)
- A stop condition (P)

Figure 8.

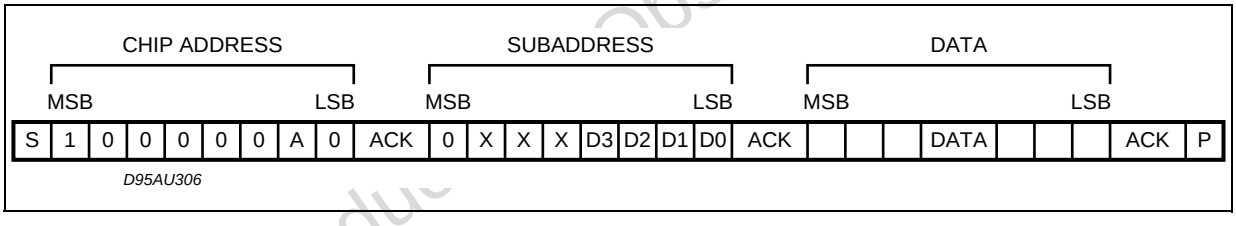


5 EXAMPLES

5.1 No Incremental Bus

The TDA7429L receives a start condition, the correct chip address, a subaddress with the MSB = 0 (no incremental bus), N-datas (all these datas concern the subaddress selected), a stop condition.

Figure 9.



5.2 Incremental Bus

The TDA7429L receives a start condition, the correct chip address, a subaddress with the MSB = 1 (incremental bus): now it is in a loop condition with an autoincrease of the subaddress whereas SUBADDRESS from "1XXX1010" to "1XXX1111" of DATA are ignored.The DATA 1 concern thesubaddress sent, and the DATA 2 concern the subaddress sent plus one in the loop etc, and at the end it receivers the stop condition.

Figure 10.

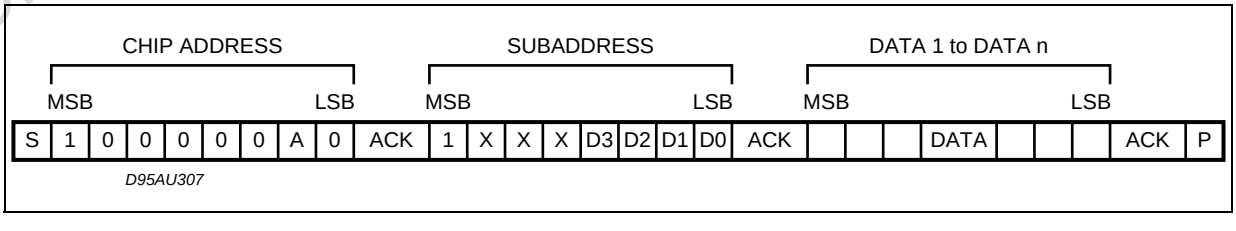


Table 6. Function Selection

The first byte (subaddress)

MSB							LSB	SUBADDRESS
D7	D6	D5	D4	D3	D2	D1	D0	
B[1]	X[2]	X	X	0	0	0	0	INPUT ATTENUATION
B	X	X	X	0	0	0	1	CONTROL OUT L+R & SUBWOOFER
B	X	X	X	0	0	1	0	NOT USED
B	X	X	X	0	0	1	1	BASS & NATURAL BASE
B	X	X	X	0	1	0	0	MIDDLE & TREBLE
B	X	X	X	0	1	0	1	SPEAKER ATTENUATION "L“
B	X	X	X	0	1	1	1	AUX ATTENUATION "L”
B	X	X	X	1	0	0	0	AUX ATTENUATION"R”
B	X	X	X	1	0	0	1	INPUT MULTIPLEXER, & AUX OUT

<1> B = 1 incremental bus; active
B = 0 no incremental bus;
<2> X = indifferent 0,1

Table 7. Input Attenuation Selection

MSB							LSB	INPUT ATTENUATION
D7	D6	D5	D4	D3	D2	D1	D0	0.5 dB STEPS
X					0	0	0	0
X					0	0	1	-0.5
X					0	1	0	-1
X					0	1	1	-1.5
X					1	0	0	-2
X					1	0	1	-2.5
X					1	1	0	-3
X					1	1	1	-3.5
								4 dB STEPS
X		0	0	0				0
X		0	0	1				-4
X		0	1	0				-8
X		0	1	1				-12
X		1	0	0				-16
X		1	0	1				-20
X		1	1	0				-24
X		1	1	1				-28
INPUT ATTENUATION = 0 ~ -31.5dB								
D7	D6	D5	D4	D3	D2	D1	D0	L+R OUTPUT SWITCH
X	0							(L+R) OUTPUT PIN ACTIVE

Table 8. Out & (L+R) & Subwoofer Selection

MSB							LSB	
D7	D6	D5	D4	D3	D2	D1	D0	SUBWOOFER CONTROL
X						0	0	SUBWOOFER ON
X						0	1	NOT ALLOWED
X						1	0	SUBWOOFER OFF
X						1	1	NOT ALLOWED
								OUT
X					0			VAR
X					1			FIX
								L+R CONTROL
X	0	0	0	0				+4
X	0	0	0	1				+3
X	0	0	1	0				+2
X	0	0	1	1				+1
X	0	1	0	0				0
X	0	1	0	1				-1
X	0	1	1	0				-2
X	0	1	1	1				-3
X	1	0	0	0				-4
X	1	0	0	1				-5
X	1	0	1	0				-6
X	1	0	1	1				-7
X	1	1	0	0				-8
X	1	1	0	1				--9
X	1	1	1	0				-10
X	1	1	1	1				-11

Table 9. Bass Selection

MSB							LSB	BASS
D7	D6	D5	D4	D3	D2	D1	D0	2 dB STEPS
X	X	X	1	0	0	0	0	-14
X	X	X	1	0	0	0	1	-12
X	X	X	1	0	0	1	0	-10
X	X	X	1	0	0	1	1	-8
X	X	X	1	0	1	0	0	-6
X	X	X	1	0	1	0	1	-4
X	X	X	1	0	1	1	0	-2
X	X	X	1	0	1	1	1	0
X	X	X	1	1	1	1	1	0
X	X	X	1	1	1	1	0	2
X	X	X	1	1	1	0	1	4
X	X	X	1	1	1	0	0	6
X	X	X	1	1	0	1	1	8
X	X	X	1	1	0	1	0	10
X	X	X	1	1	0	0	1	12
X	X	X	1	1	0	0	0	14

Table 10. Speaker/Aux Att. R & L Selection

MSB							LSB	SPEAKER/AUX ATT
D7	D6	D5	D4	D3	D2	D1	D0	1 dB STEPS
X					0	0	0	0
X					0	0	1	-1
X					0	1	0	-2
X					0	1	1	-3
X					1	0	0	-4
X					1	0	1	-5
X					1	1	0	-6
X					1	1	1	-7
								8 dB STEPS
X	0	0	0	0				0
X	0	0	0	1				-8
X	0	0	1	0				-16
X	0	0	1	1				-24
X	0	1	0	0				-32
X	0	1	0	1				-40
X	0	1	1	0				-48
X	0	1	1	1				-56
X	1	0	0	0				-64
X	1	0	0	1				-72
								MUTE
X	1	0	1	X				
X	1	1	X	X				

Notes: 1. X = INDIFFERENT 0.1
2. SPAEAKER/AUX ATTENUATION = 0dB to 79dB

Table 11. Middle & Treble Selection

MSB							LSB	MIDDLE
D7	D6	D5	D4	D3	D2	D1	D0	2 dB STEPS
				0	0	0	0	-14
				0	0	0	1	-12
				0	0	1	0	-10
				0	0	1	1	-8
				0	1	0	0	-6
				0	1	0	1	-4
				0	1	1	0	-2
				0	1	1	1	0
				1	1	1	1	0
				1	1	1	0	2
				1	1	0	1	4
				1	1	0	0	6
				1	0	1	1	8
				1	0	1	0	10
				1	0	0	1	12
				1	0	0	0	14
								TREBLE
								2 dB STEPS
0	0	0	0					-14
0	0	0	1					-12
0	0	1	0					-10
0	0	1	1					-8
0	1	0	0					-6
0	1	0	1					-4
0	1	1	0					-2
0	1	1	1					0
1	1	1	1					0
1	1	1	0					2
1	1	0	1					4
1	1	0	0					6
1	0	1	1					8
1	0	1	0					10
1	0	0	1					12
1	0	0	0					14

Table 12. Input/recout L & R Selection

MSB							LSB	
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**INPUT MULTIPLEXER**
X					1	1	0	IN1
X					0	0	0	IN2
X					0	1	0	IN3
								AUX OUT "L”
X			0	0			0	VAR 1 (3BAND)
X			0	1			0	NOT ALLOWED
X			1	0			0	VAR 3 (REAR)
X			1	1			0	FIX
								AUX OUT "R”
X	0	0					0	VAR 1 (3BAND)
X	0	1					0	NOT ALLOWED
X	1	0					0	VAR 3 (REAR)
X	1	1					0	FIX

Table 13. Power on reset

BASS & MIDDLE	2dB
TREBLE	0dB
SURROUND & OUT CONTROL + (L+R) CONTROL	OFF + FIX + MAX. ATTENUATION
SPEAKER/AUX ATTENUATION L & R	MUTE
INPUT ATTENUATION + (L+R) SWITCH	MAX. ATTENUATION + ON
NATURAL BASE	OFF
INPUT	IN1

Figure 11. Pin: TREBLE-L, TREBLE-R

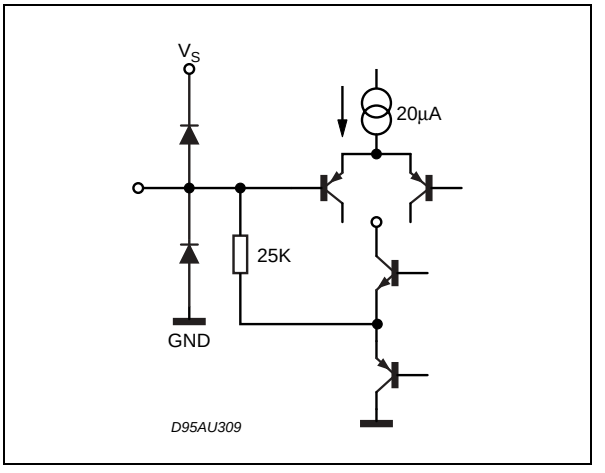


Figure 12. Pin: V_{OUT} REF

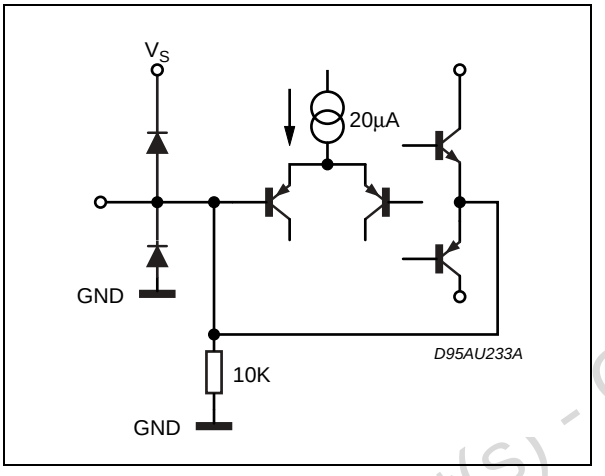


Figure 13. Pin: L-IN, R-IN, L-IN2, R-IN2, L-IN3, R-IN3, L-IN4, R-IN4

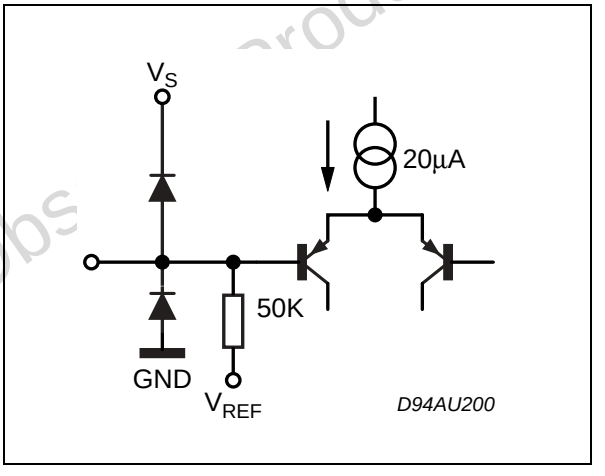


Figure 14. Pin: CREF

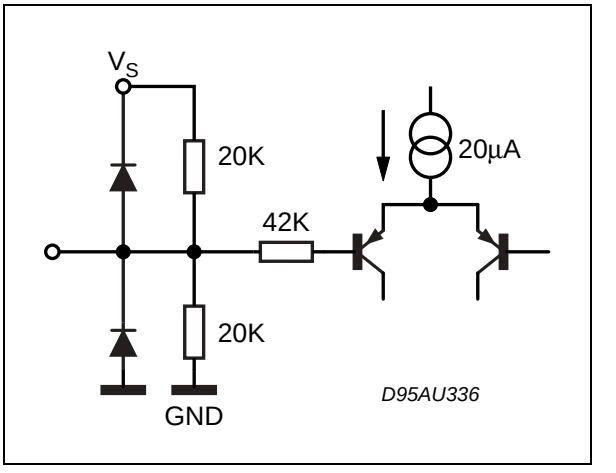


Figure 15. Pin: VAR-L, VAR-R

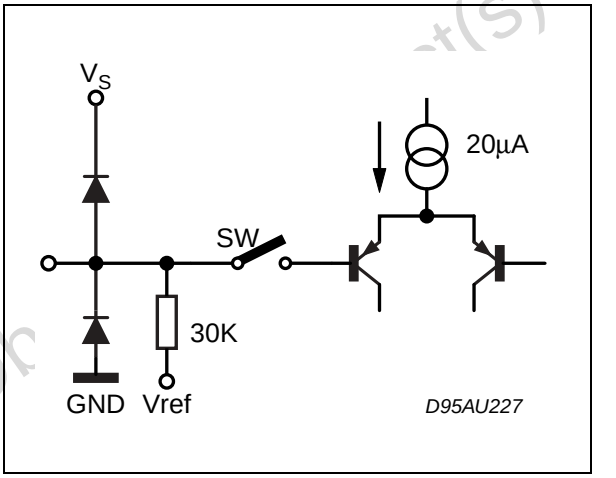


Figure 16. Pin: LP1, LP

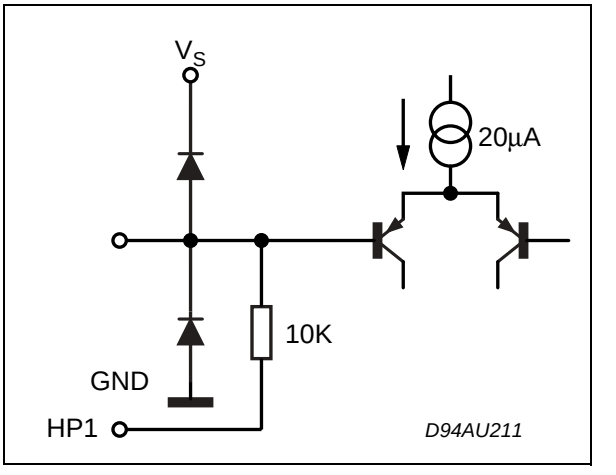


Figure 17. Pin: SCL, SDA

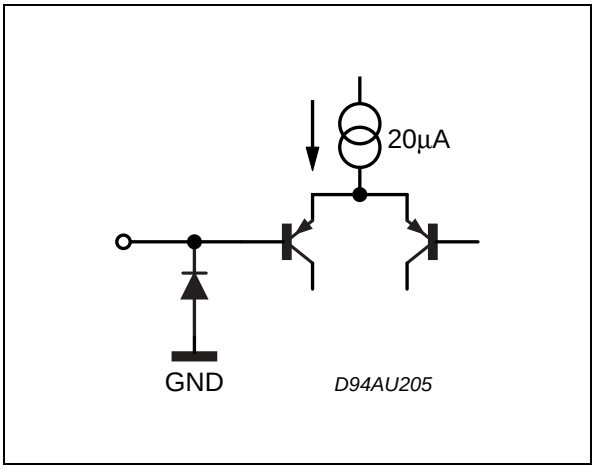


Figure 18. Pin: MONO INPUT

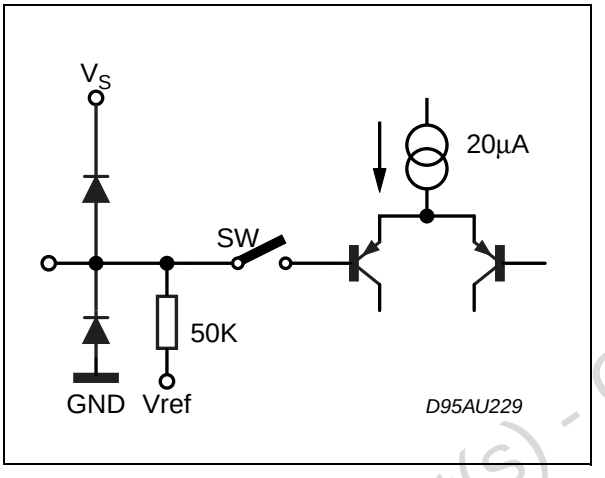


Figure 19. Pin: L-OUT, R-OUT, MONITOR-L, MONITOR-R, LTR OUTPUT, BASSO-L, BASSO-R, AUXOUT_L, AUXOUT_R

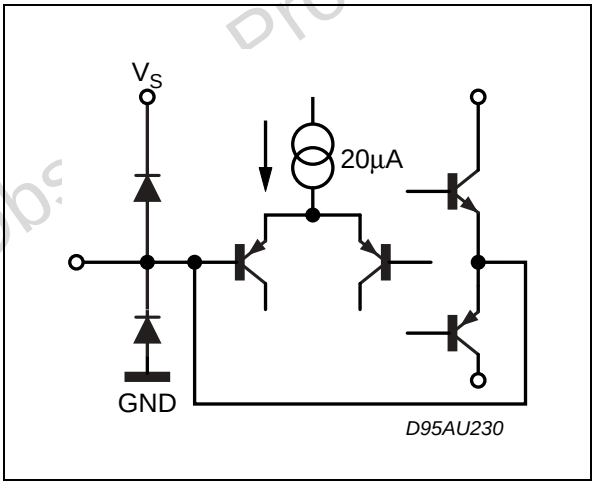


Figure 20. Pin: BASS-LI, BASS-RI, MIDDLE-LI, MIDDLE-R

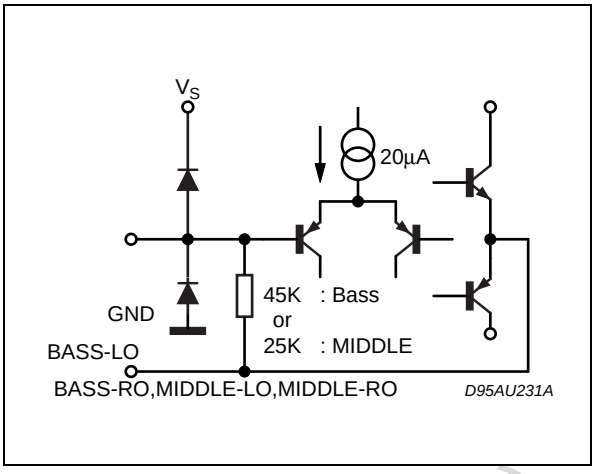


Figure 21. Pin: BASS-LO, BASS-RO, MIDDLE-LO,MIDDLE-RO

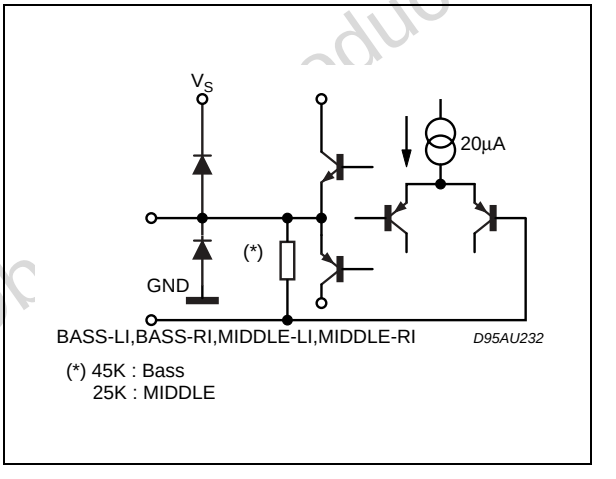
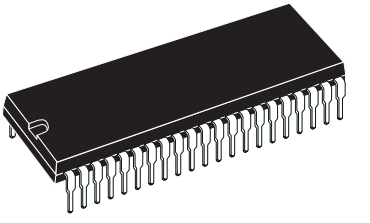


Figure 22. SDIP42 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5.08			0.20
A1	0.51			0.020		
A2	3.05	3.81	4.57	0.120	0.150	0.180
B	0.38	0.46	0.56	0.0149	0.0181	0.0220
B1	0.89	1.02	1.14	0.035	0.040	0.045
c	0.23	0.25	0.38	0.0090	0.0098	0.0150
D	36.58	36.83	37.08	1.440	1.450	1.460
E	15.24		16.00	0.60		0.629
E1	12.70	13.72	14.48	0.50	0.540	0.570
e		1.778			0.070	
e1		15.24			0.60	
e2			18.54			0.730
e3			1.52			0.060
L	2.54	3.30	3.56	0.10	0.130	0.140

OUTLINE AND MECHANICAL DATA



SDIP42 (0.600")

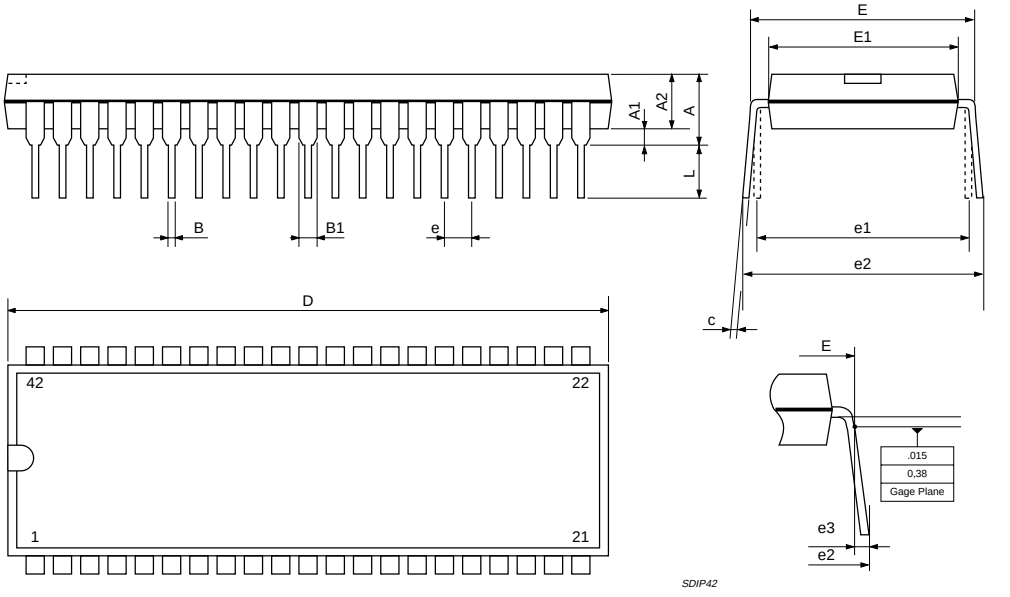


Table 14. Revision History

Date	Revision	Description of Changes
January 2004	2	First Issue in EDOCS DMS
June 2004	3	Changed the Style-sheet in compliance to the new “Corporate Technical Pubblications Design Guide”