

CD4011UB Types

CMOS Quad 2-Input NAND Gate

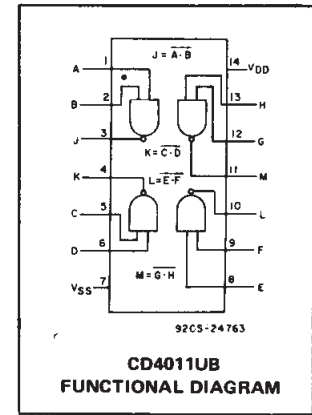
High-Voltage Types (20-Volt Rating)

■ CD4011UB quad 2-input NAND gate provides the system designer with direct implementation of the NAND function and supplements the existing family of CMOS gates.

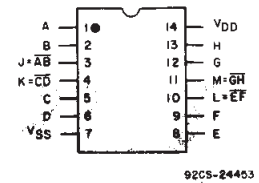
The CD4011UB types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

- Propagation delay time = 30 ns (typ.) at $C_L = 50$ pF, $V_{DD} = 10$ V
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μ A at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



TERMINAL ASSIGNMENT



**TOP VIEW
CD4011UB**

MAXIMUM RATINGS, Absolute-Maximum Values:

| | | |
|--|-------|---|
| DC SUPPLY-VOLTAGE RANGE, (V_{DD}) | | -0.5V to +20V |
| Voltages referenced to V_{SS} Terminal | | |
| INPUT VOLTAGE RANGE, ALL INPUTS | | -0.5V to $V_{DD} + 0.5V$ |
| DC INPUT CURRENT, ANY ONE INPUT | | ± 10 mA |
| POWER DISSIPATION PER PACKAGE (P_D): | | 500 mW |
| For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ | | |
| For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ | | Derate Linearly at 12mW/°C to 200mW |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR | | 100 mW |
| FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types) | | |
| OPERATING-TEMPERATURE RANGE (T_A) | | -55°C to $+125^\circ\text{C}$ |
| STORAGE TEMPERATURE RANGE (T_{stg}) | | -65°C to $+150^\circ\text{C}$ |
| LEAD TEMPERATURE (DURING SOLDERING): | | $+265^\circ\text{C}$ |
| At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10s max | | |

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

| CHARACTERISTIC | MIN. | MAX. | UNITS |
|---|------|------|-------|
| Supply Voltage Range (For $T_A =$ Full Package Temperature Range) | 3 | 18 | V |

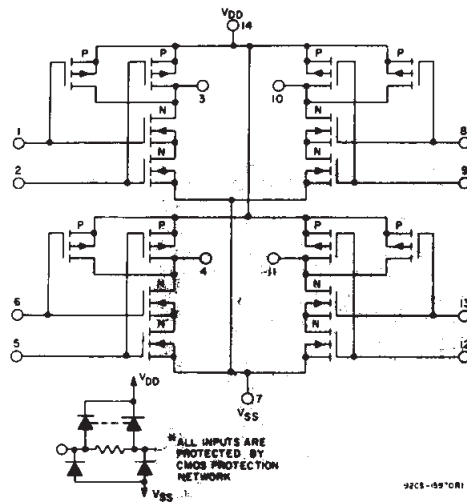


Fig. 1 - Schematic diagram for type CD4011UB.

CD4011UB Types

STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|--|--------------------|---------------------|---------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
| | V _O (V) | V _{IN} (V) | V _{DD} (V) | | | | | +25 | | | |
| | | | | -55 | -40 | +85 | +125 | Min. | Typ. | Max. | |
| Quiescent Device Current, I _{DD} Max. | - | 0,5 | 5 | 0.25 | 0.25 | 7.5 | 7.5 | - | 0.01 | 0.25 | μA |
| | - | 0,10 | 10 | 0.5 | 0.5 | 15 | 15 | - | 0.01 | 0.5 | |
| | - | 0,15 | 15 | 1 | 1 | 30 | 30 | - | 0.01 | 1 | |
| | - | 0,20 | 20 | 5 | 5 | 150 | 150 | - | 0.02 | 5 | |
| Output Low (Sink) Current I _{OL} Min. | 0.4 | 0,5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | - | mA |
| | 0.5 | 0,10 | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | - | |
| | 1.5 | 0,15 | 15 | 4.2 | 4 | 2.8 | 2.4 | 3.4 | 6.8 | - | |
| Output High (Source) Current, I _{OH} Min. | 4.6 | 0,5 | 5 | -0.64 | -0.61 | -0.42 | -0.36 | -0.51 | -1 | - | mA |
| | 2.5 | 0,5 | 5 | -2 | -1.8 | -1.3 | -1.15 | -1.6 | -3.2 | - | |
| | 9.5 | 0,10 | 10 | -1.6 | -1.5 | -1.1 | -0.9 | -1.3 | -2.6 | - | |
| Output Voltage: Low-Level, V _{OL} Max. | - | 0,5 | 5 | 0.05 | | | | - | 0 | 0.05 | V |
| | - | 0,10 | 10 | 0.05 | | | | - | 0 | 0.05 | |
| | - | 0,15 | 15 | 0.05 | | | | - | 0 | 0.05 | |
| Output Voltage: High-Level, V _{OH} Min. | - | 0,5 | 5 | 4.95 | | | | 4.95 | 5 | - | V |
| | - | 0,10 | 10 | 9.95 | | | | 9.95 | 10 | - | |
| | - | 0,15 | 15 | 14.95 | | | | 14.95 | 15 | - | |
| Input Low Voltage, V _{IL} Max. | 4.5 | - | 5 | 1 | | | | - | - | 1 | V |
| | 9 | - | 10 | 2 | | | | - | - | 2 | |
| | 13.5 | - | 15 | 2.5 | | | | - | - | 2.5 | |
| Input High Voltage, V _{IH} Min. | 0.5,4.5 | - | 5 | 4 | | | | 4 | - | - | V |
| | 1,9 | - | 10 | 8 | | | | 8 | - | - | |
| | 1.5,13.5 | - | 15 | 12.5 | | | | 12.5 | - | - | |
| Input Current I _{IN} Max. | | 0,18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | - | ±10 ⁻⁵ | ±0.1 | μA |

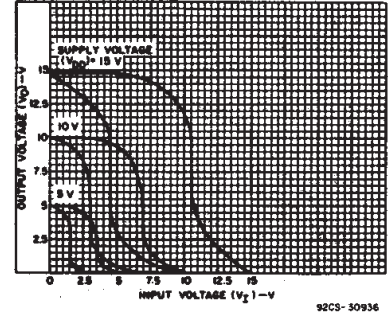


Fig. 2 - Minimum and maximum voltage transfer characteristics.

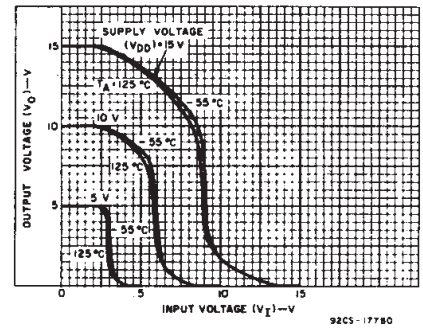


Fig. 3 - Typical voltage transfer characteristics as a function of temperature.

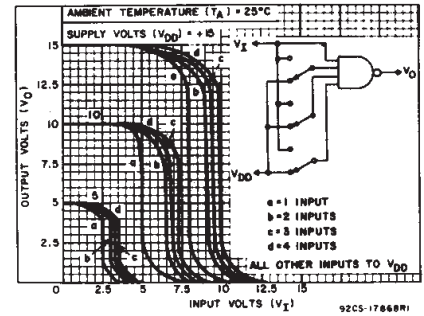


Fig. 4 - Typical multiple input switching transfer characteristics for CD4012UB.

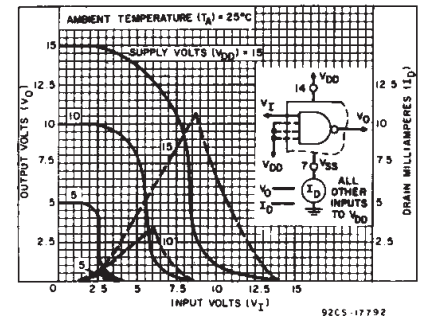


Fig. 5 - Typical current and voltage transfer characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25^\circ\text{C}$, Input $t_p, t_f = 20\text{ ns}$, and $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

| CHARACTERISTIC | TEST CONDITIONS | LIMITS | | UNITS | |
|--|-----------------|-----------------------|------|-------|-----|
| | | V _{DD} VOLTS | TYP. | | MAX |
| Propagation Delay Time, t_{PHL}, t_{PLH} | | 5 | 60 | 120 | ns |
| | | 10 | 30 | 60 | |
| | | 15 | 25 | 50 | |
| Transition Time, t_{THL}, t_{TLH} | | 5 | 100 | 200 | ns |
| | | 10 | 50 | 100 | |
| | | 15 | 40 | 80 | |
| Input Capacitance, C _{IN} | Any Input | | 10 | 15 | pF |

CD4011UB Types

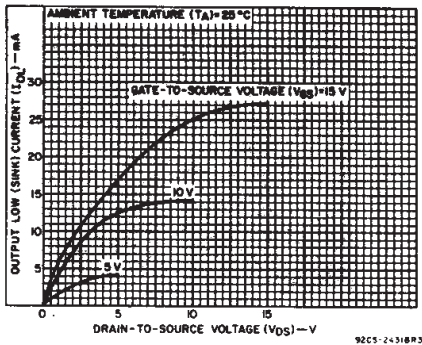


Fig. 6 - Typical output low (sink) current characteristics.

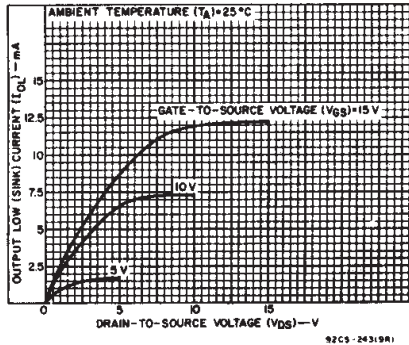


Fig. 7 - Minimum output low (sink) current characteristics.

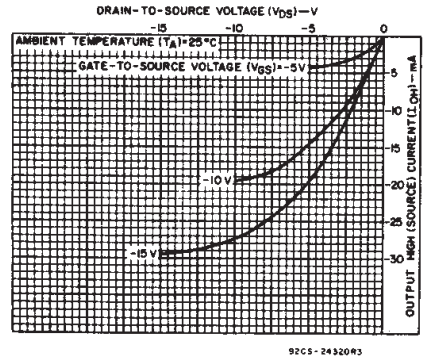


Fig. 8 - Typical output high (source) current characteristics.

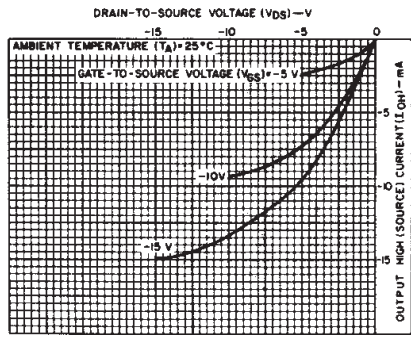


Fig. 9 - Minimum output high (source) current characteristics.

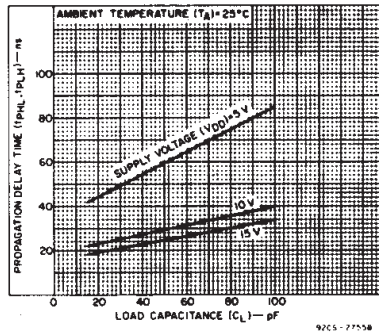


Fig. 10 - Typical propagation delay time vs. load capacitance.

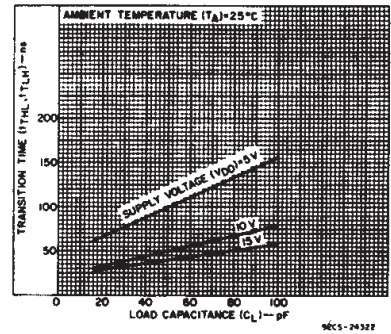


Fig. 11 - Typical transition time vs. load capacitance.

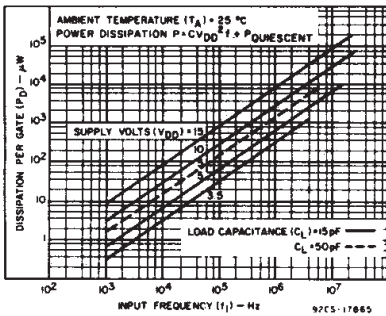


Fig. 12 - Typical power dissipation vs. frequency characteristics.

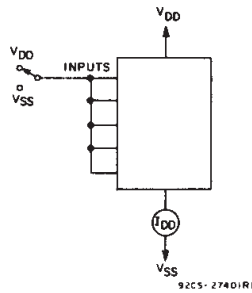


Fig. 13 - Quiescent device current test circuit.

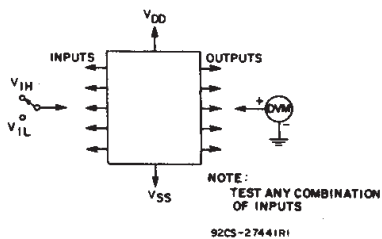


Fig. 14 - Input voltage test circuit.

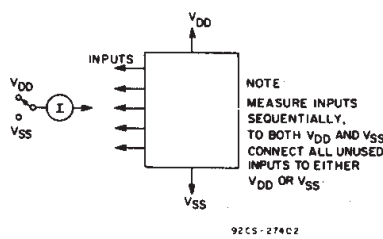
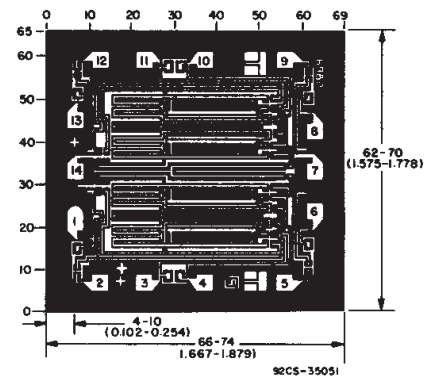


Fig. 15 - Input current test circuit.

Chip Dimensions and Pad Layout



CD4011UBH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| CD4011UBE | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD4011UBEE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD4011UBF | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| CD4011UBM | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4011UBM96 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4011UBM96E4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4011UBM96G4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4011UBME4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4011UBMG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4011UBMT | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4011UBMTE4 | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4011UBMTG4 | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4011UBNSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4011UBNSRE4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4011UBNSRG4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4011UBPWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4011UBPWRE4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4011UBPWG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS

compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD4011UBM96 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| CD4011UBMT | SOIC | D | 14 | 250 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| CD4011UBNSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| CD4011UBPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD4011UBM96 | SOIC | D | 14 | 2500 | 346.0 | 346.0 | 33.0 |
| CD4011UBMT | SOIC | D | 14 | 250 | 346.0 | 346.0 | 33.0 |
| CD4011UBNSR | SO | NS | 14 | 2000 | 346.0 | 346.0 | 33.0 |
| CD4011UBPWR | TSSOP | PW | 14 | 2000 | 346.0 | 346.0 | 29.0 |

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

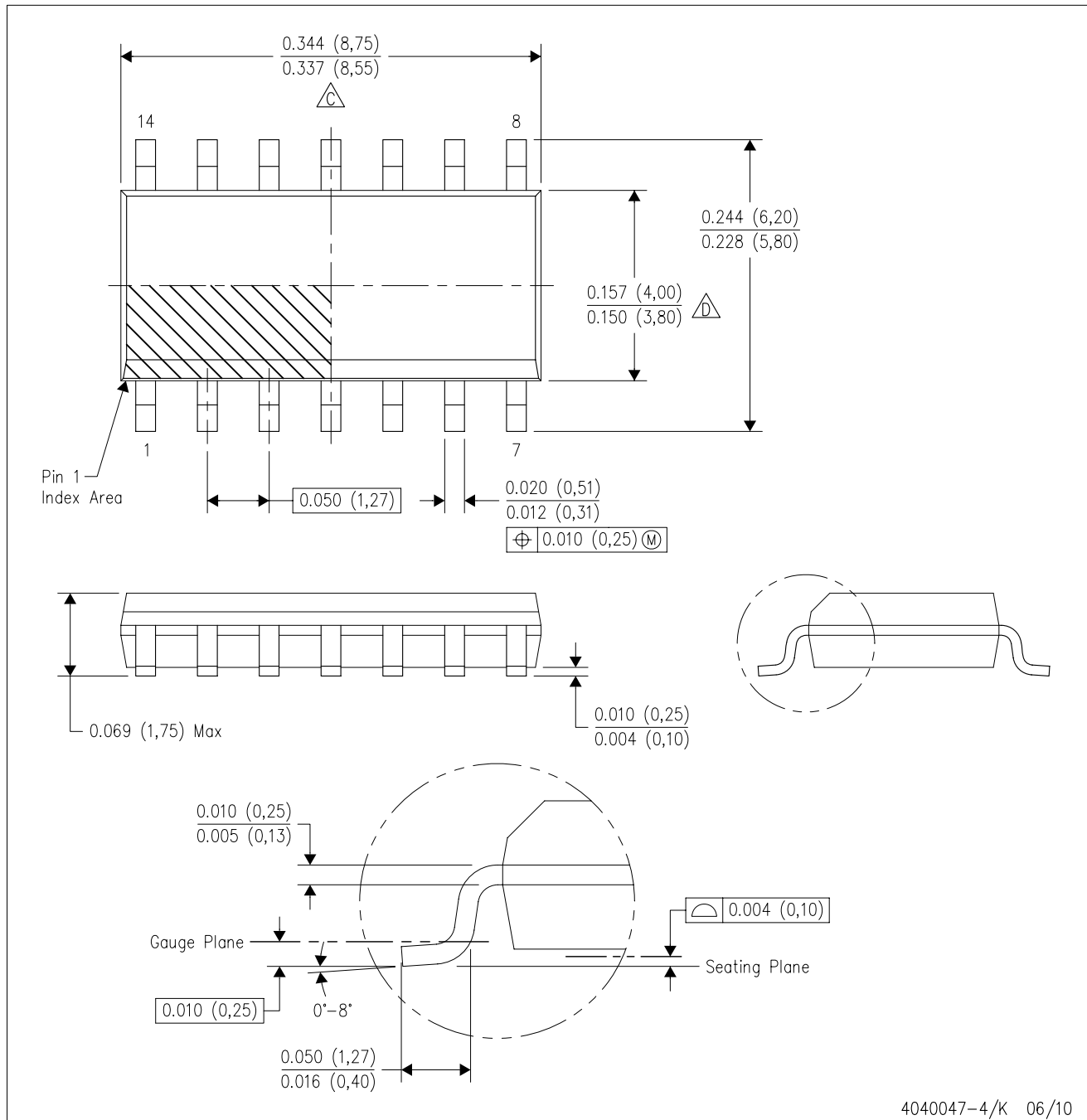


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

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D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE

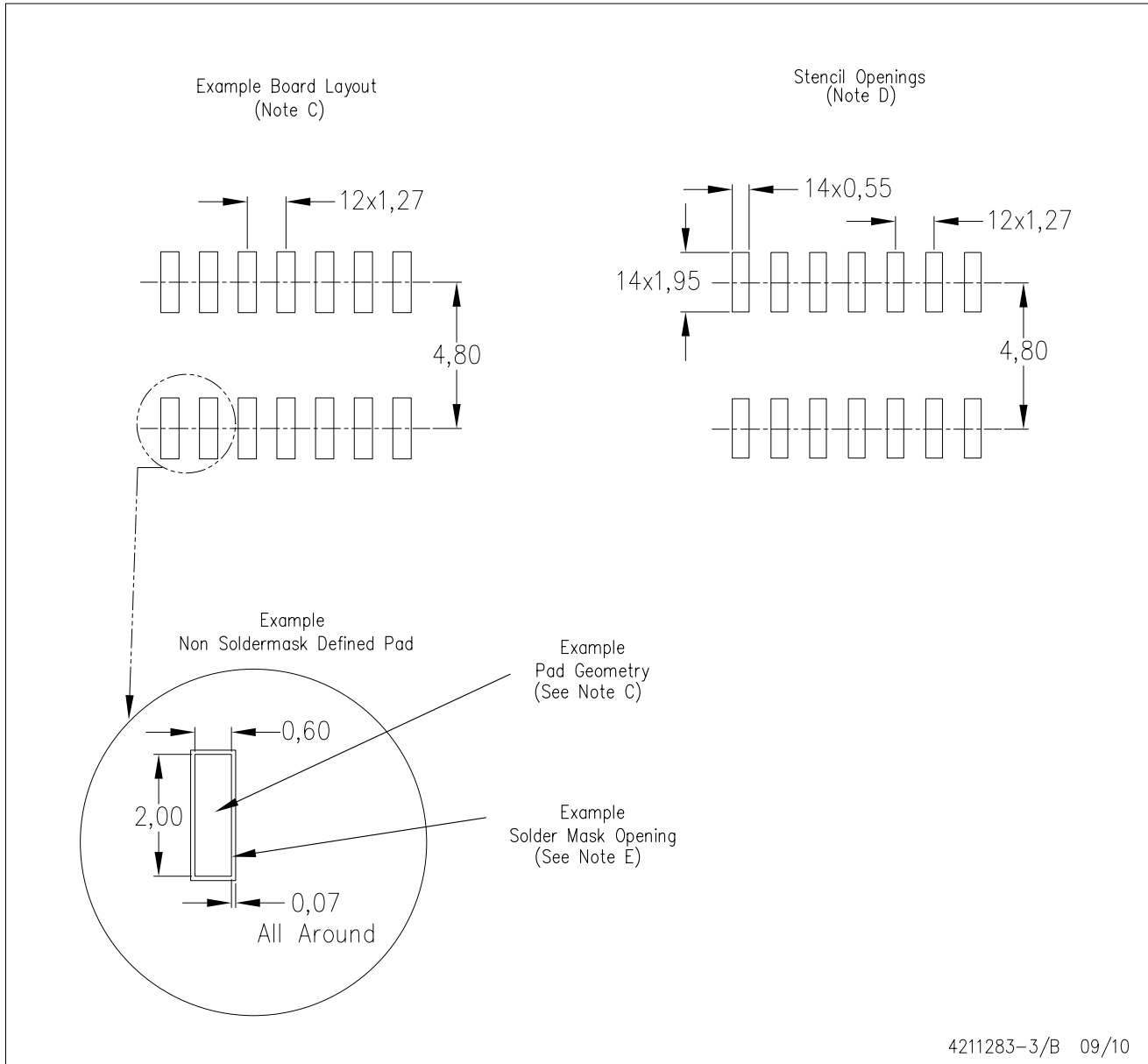


4040047-4/K 06/10

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

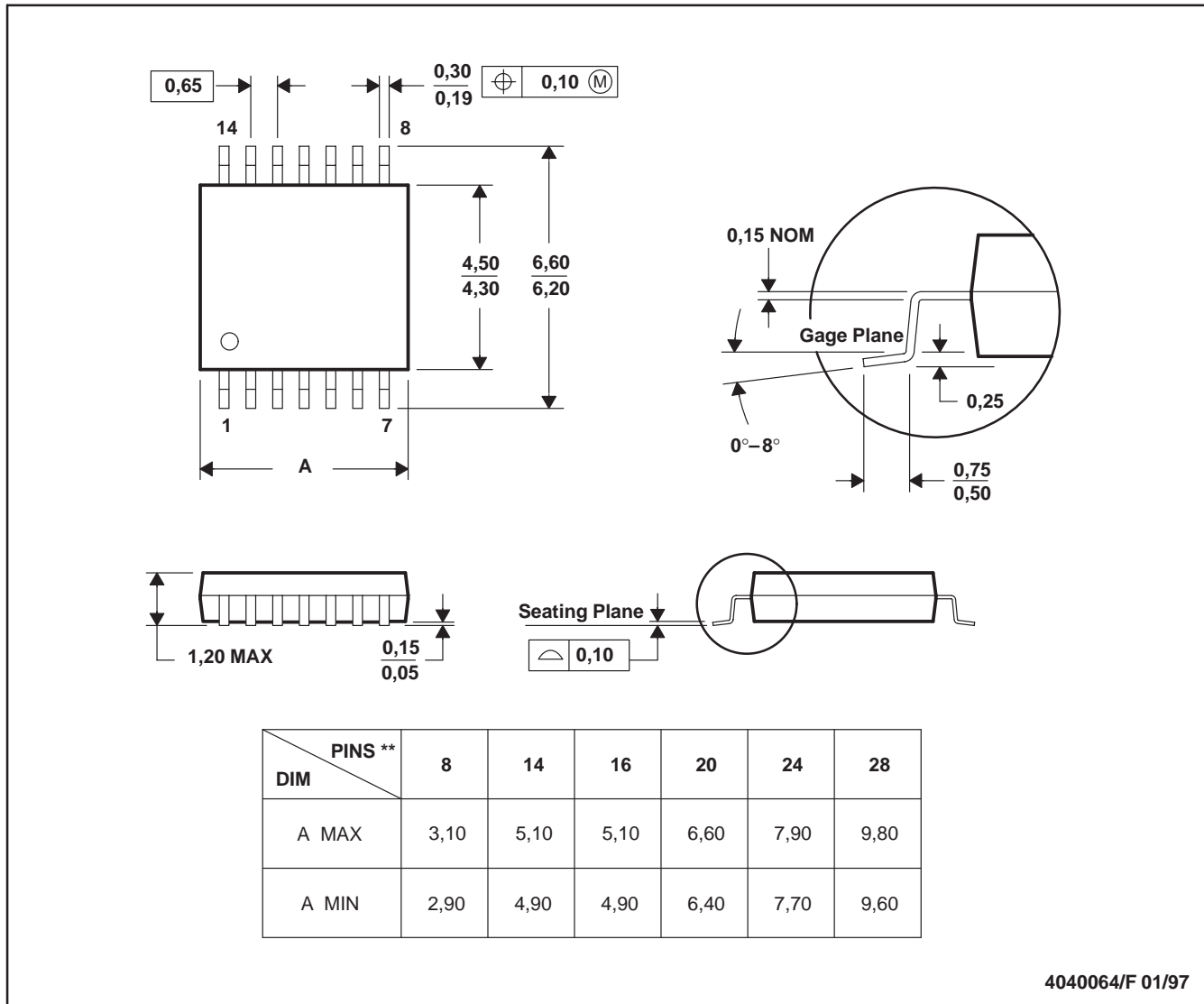


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

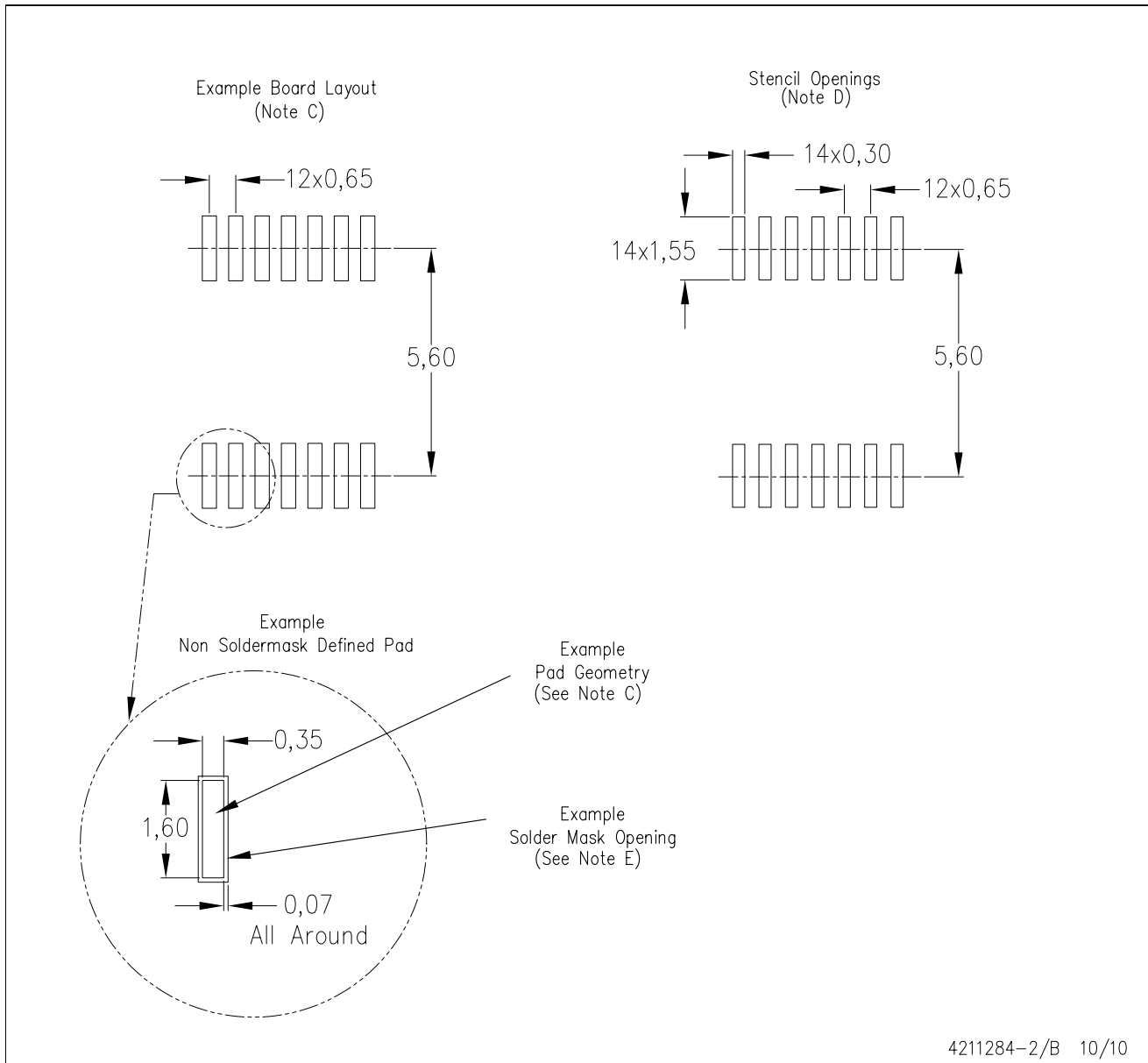


4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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