

CD40147B Types

10-Line to 4-Line BCD Priority Encoder

High-Voltage Types (20-Volt Rating)

The CD40147B CMOS encoder features priority encoding of the inputs to ensure that only the highest-order data line is encoded. Ten data input lines (0-9) are encoded to four-line (8, 4, 2, 1) BCD. The highest priority line is line 9. All four output lines are logic 1 (V_{SS}) when all input lines are logic 0. All inputs and outputs are buffered, and each output can drive one TTL low-power Schottky load. The CD40147B is functionally similar to the TTL5474/147 if pin 15 is tied low.

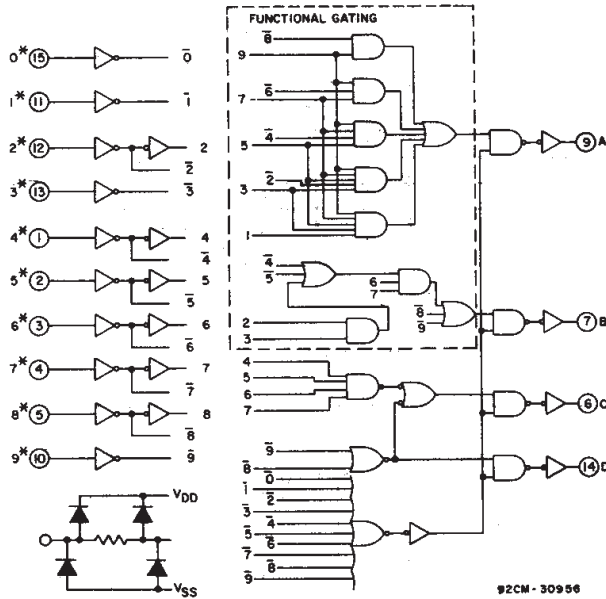
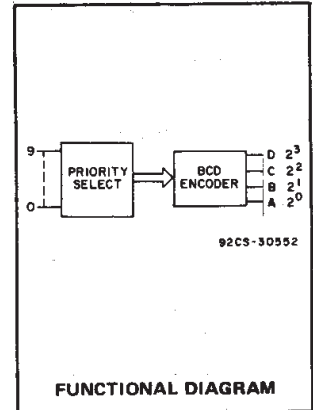
The CD40147B types are supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

- Encodes 10-line to 4-line BCD
- Active low inputs and outputs
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =
 - 1 V at $V_{DD} = 5$ V
 - 2 V at $V_{DD} = 10$ V
 - 2.5 V at $V_{DD} = 15$ V

Applications:

- Keyboard encoding
- 10-line to BCD encoding
- Range selection



* INPUTS PROTECTED BY COS/MOS PROTECTION NETWORK

Fig. 1 - CD40147B logic diagram.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following range:

| CHARACTERISTIC | LIMITS | | UNITS |
|---|--------|------|-------|
| | Min. | Max. | |
| Supply Voltage Range (For T_A = Full Package Temperature Range) | 3 | 18 | V |

TRUTH TABLE (Negative Logic)

| INPUTS | | | | | | | | | | OUTPUTS | | | |
|--------|---|---|---|---|---|---|---|---|---|---------|---|---|---|
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | D | C | B | A |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| X | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| X | X | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| X | X | X | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| X | X | X | X | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| X | X | X | X | X | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| X | X | X | X | X | X | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| X | X | X | X | X | X | X | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| X | X | X | X | X | X | X | X | 1 | 0 | 1 | 0 | 0 | 0 |
| X | X | X | X | X | X | X | X | X | 1 | 1 | 0 | 0 | 1 |

0 = High Level 1 = Low Level X = Don't Care

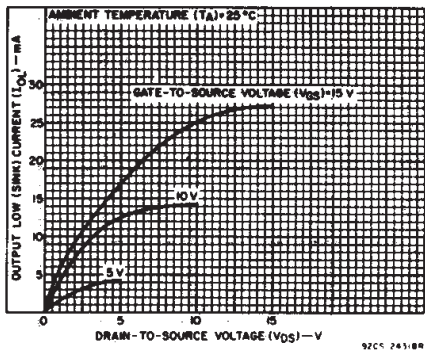


Fig. 2 - Typical output low (sink) current characteristics.

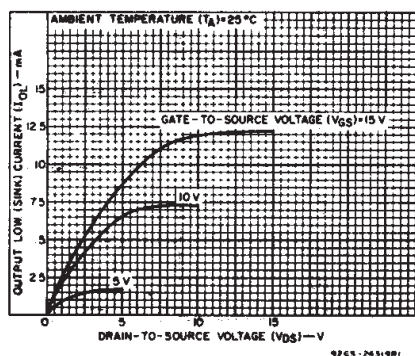


Fig. 3 - Minimum output low (sink) current characteristics.

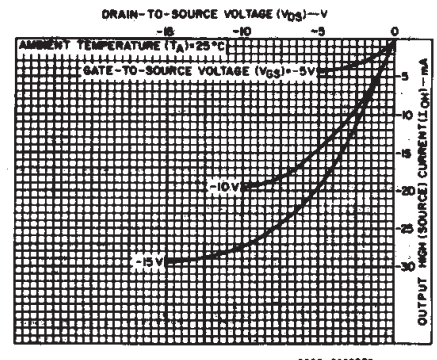


Fig. 4 - Typical output high (source) current characteristics.

CD40147B Types

MAXIMUM RATINGS, Absolute-Maximum Values:

| | |
|---|-------------------------------------|
| DC SUPPLY-VOLTAGE RANGE, (V _{DD}) | -0.5V to +20V |
| Voltages referenced to V _{SS} Terminal | |
| INPUT VOLTAGE RANGE, ALL INPUTS | -0.5V to V _{DD} +0.5V |
| DC INPUT CURRENT, ANY ONE INPUT | ±10mA |
| POWER DISSIPATION PER PACKAGE (P _D): | |
| For T _A = -55°C to +100°C | 500mW |
| For T _A = +100°C to +125°C | Derate Linearly at 12mW/°C to 200mW |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR | |
| FOR T _A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) | 100mW |
| OPERATING-TEMPERATURE RANGE (T _A) | -55°C to +125°C |
| STORAGE TEMPERATURE RANGE (T _{stg}) | -65°C to +150°C |
| LEAD TEMPERATURE (DURING SOLDERING): | |
| At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max | +265°C |

STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|--|-----------------------|------------------------|------------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
| | V _O (V) | V _{IN} (V) | V _{DD} (V) | -55 | -40 | +85 | +125 | +25 | | | |
| | | | | | | | | Min. | Typ. | Max. | |
| Quiescent Device Current, I _{DD} Max. | — | 0.5 | 5 | 5 | 5 | 150 | 150 | — | 0.04 | 5 | μA |
| Output Low (Sink) Current I _{OL} Min. | 0.4 | 0.5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | — | |
| Output (Source) Current, I _{OH} Min. | 4.6 | 0.5 | 5 | -0.64 | -0.61 | -0.42 | -0.36 | -0.51 | -1 | — | |
| Output Voltage: Low-Level, V _{OL} Max. | — | 0.5 | 5 | 0.05 | | | — | 0 | 0.05 | — | V |
| Output Voltage: High-Level, V _{OH} Min. | — | 0.5 | 5 | 4.95 | | | 4.95 | 5 | — | | |
| Input Low Voltage, V _{IL} Max. | 0.5, 4.5 | — | 5 | 1.5 | | | — | — | 1.5 | — | |
| Input High Voltage, V _{IH} Min. | 0.5, 4.5 | — | 5 | 3.5 | | | 3.5 | — | — | — | |
| Input Current I _{IN} Max. | — | 0.18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | — | ±10 ⁻⁵ | ±0.1 | μA |

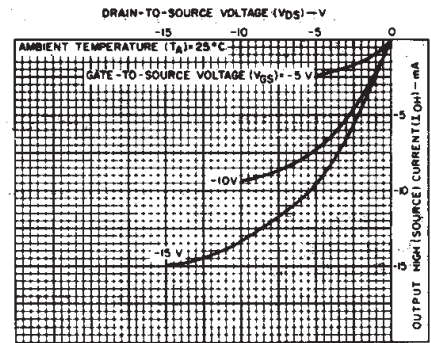


Fig. 5 — Minimum output high (source) current characteristics.

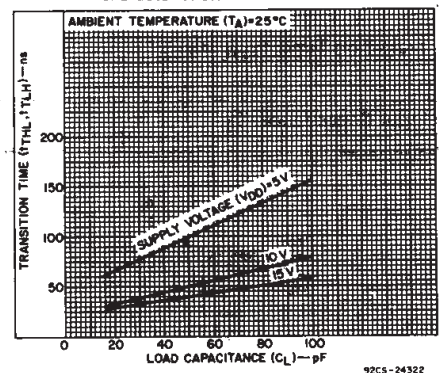


Fig. 6 — Typical transition time as a function of load capacitance.

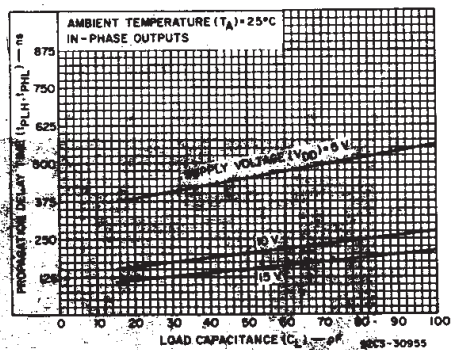


Fig. 7 — Propagation delay time as a function of load capacitance.

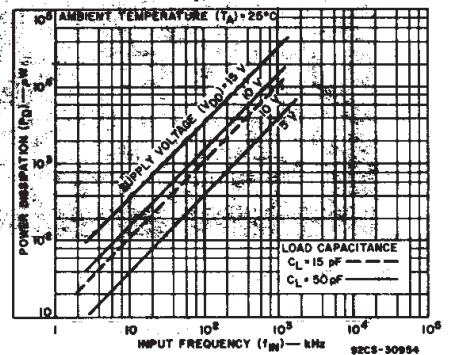


Fig. 8 — Typical dynamic power dissipation as a function of input frequency.

3
COMMERCIAL CMOS HIGH VOLTAGE ICs

CD40147B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20 \text{ ns}$,
 $C_L = 50 \text{ pF}$, $R_L = 200 \text{ k}\Omega$

| CHARACTERISTIC | TEST CONDITIONS | LIMITS ALL TYPES | | UNITS | |
|--|----------------------------|---------------------|------|-------|------|
| | | V_{DD} (V) | Typ. | | Max. |
| Propagation Delay Time, t_{PLH}, t_{PHL} In-Phase Output | Any input to any output | 5 | 450 | 900 | ns |
| | | 10 | 200 | 400 | |
| | | 15 | 150 | 300 | |
| Out-of-Phase Output | | 5 | 425 | 850 | ns |
| | | 10 | 175 | 350 | |
| | | 15 | 125 | 250 | |
| Transition Time, t_{THL}, t_{TLH} | 5 | 100 | 200 | ns | |
| | 10 | 50 | 100 | | |
| | 15 | 40 | 80 | | |
| Input Capacitance, C_1 | Any Input | 5 | 7.5 | pF | |

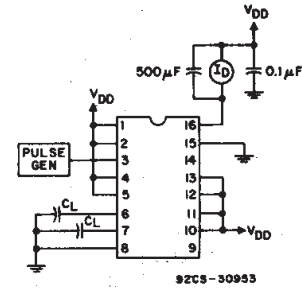


Fig. 9 - Dynamic power dissipation test circuit.

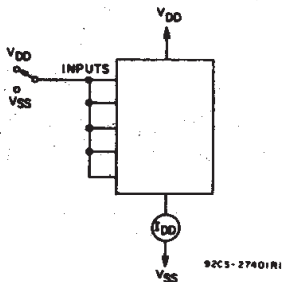


Fig. 10 - Quiescent device current test circuit.

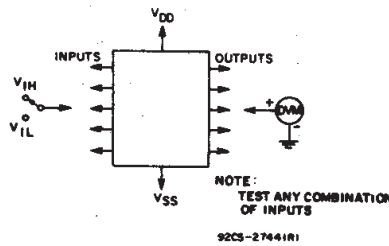


Fig. 11 - Input voltage test circuit.

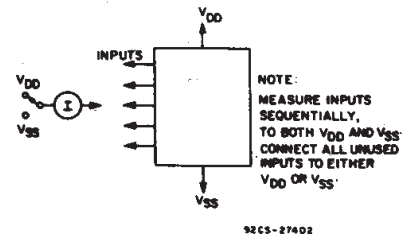
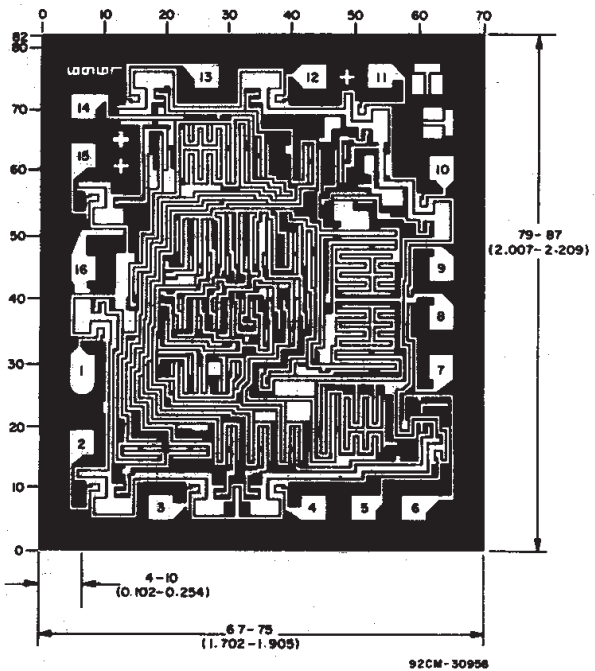
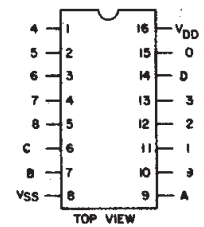


Fig. 12 - Input current test circuit.



Dimensions and pad layout for CD40147BH



CD40147B
 TERMINAL
 ASSIGNMENT

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

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PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| CD40147BE | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD40147BEE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD40147BM | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD40147BM96 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD40147BM96E4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD40147BM96G4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD40147BME4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD40147BMG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD40147BMT | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD40147BMTE4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD40147BMTG4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD40147BNSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD40147BNSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD40147BNSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD40147BPW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD40147BPWE4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD40147BPWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD40147BPWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD40147BPWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD40147BPWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD40147BM96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD40147BNSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| CD40147BPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 7.0 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD40147BM96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| CD40147BNSR | SO | NS | 16 | 2000 | 346.0 | 346.0 | 33.0 |
| CD40147BPWR | TSSOP | PW | 16 | 2000 | 346.0 | 346.0 | 29.0 |

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

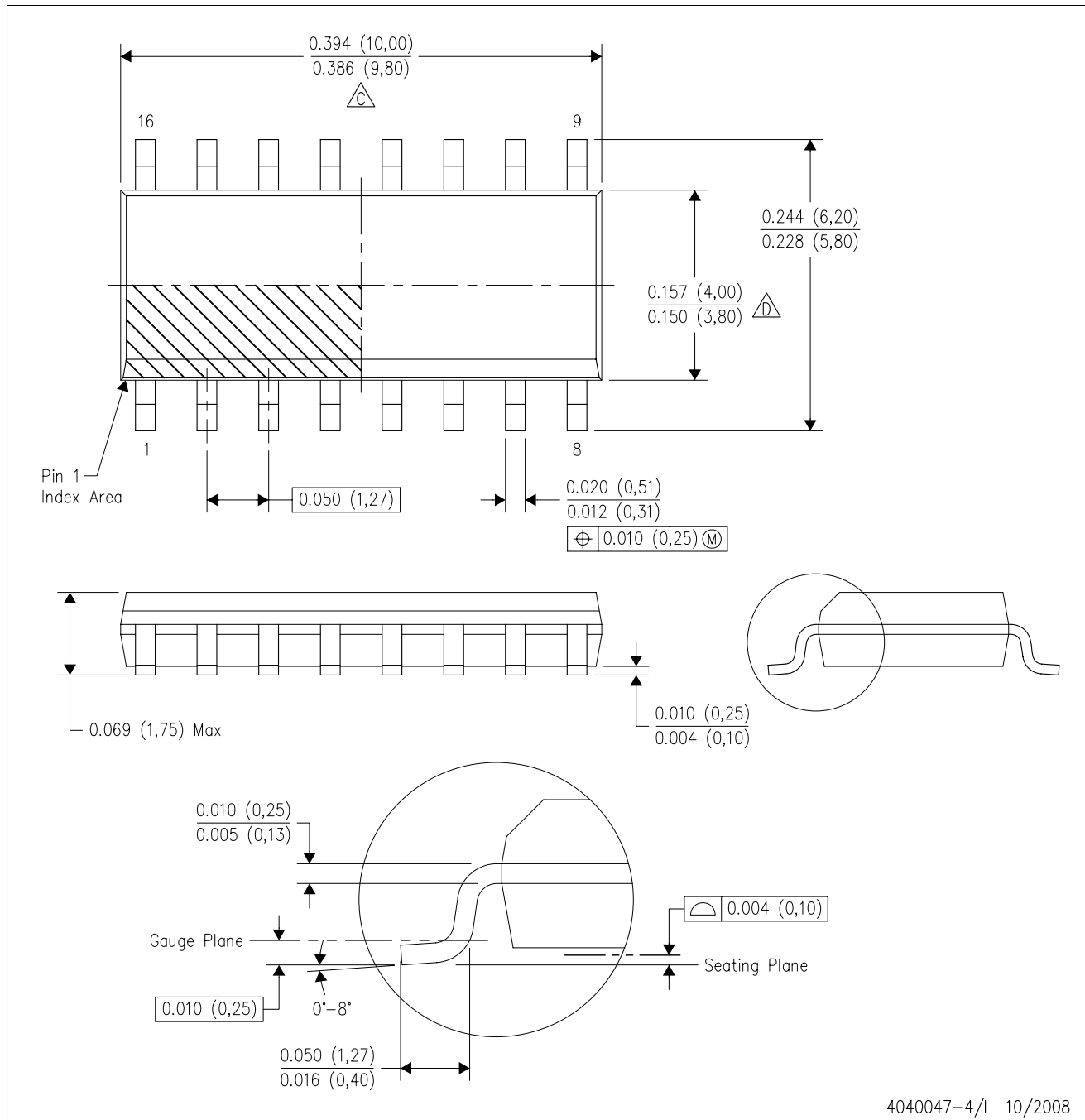


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- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AC.

D(R-PDSO-G16)



4209373/A 03/08

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.