

## High-Speed CMOS Logic 8-Input Multiplexer/Register, Three-State

SCLS459A - June 2001 - Revised May 2003

### Features

- Edge-Triggered Data Flip-Flops
  - Transparent Select Latches
- Buffered Inputs
- 3-State Complementary Outputs
- Bus Line Driving Capability
- Typical Propagation Delay:  $V_{CC} = 5V$ ,  $C_L = 15pF$ ,  $T_A = 25^{\circ}C$ 
  - Clock to Output = 22ns
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . .  $-55^{\circ}C$  to  $125^{\circ}C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- 4.5V to 5.5V Operation
- Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
- CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

### Description

The CD74HCT356 consists of data selectors/multiplexers that select one of eight sources. The data select bits (S0, S1, and S2) are stored in transparent latches that are enabled by a low latch enable input (LE).

The data is stored in edge-triggered flip-flops that are triggered by a low-to-high clock transition.

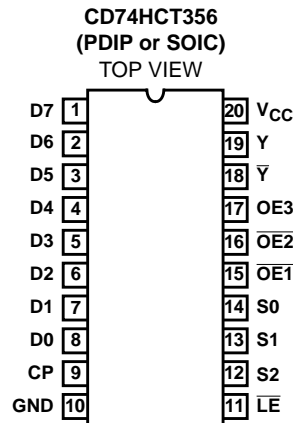
In both types the 3-state outputs are controlled by three output-enable inputs ( $\overline{OE1}$ ,  $\overline{OE2}$ , and  $\overline{OE3}$ ).

### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD74HCT356E	-55 to 125	20 Ld PDIP
CD74HCT356M96	-55 to 125	20 Ld SOIC

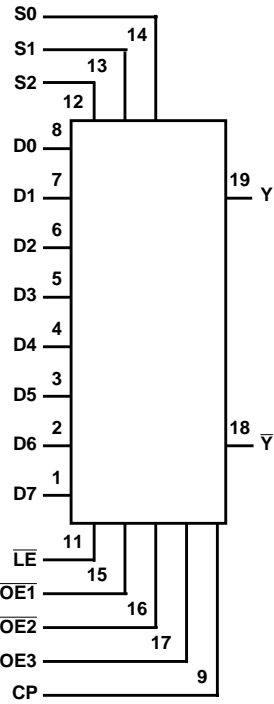
NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel.

### Pinout



# CD74HCT356

## Functional Diagram



TRUTH TABLE

INPUTS							OUTPUTS	
SELECT (NOTE 1)			CLOCK	OUTPUT ENABLES				
S2	S1	S0	CP	OE1	OE2	OE3	Y-bar	Y
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	↑	L	L	H	D0-bar	D0
L	L	L	H or L	L	L	H	D0n-bar	D0n
L	L	H	↑	L	L	H	D1-bar	D1
L	L	H	H or L	L	L	H	D1n-bar	D1n
L	H	L	↑	L	L	H	D2-bar	D2
L	H	L	H or L	L	L	H	D2n-bar	D2n
L	H	H	↑	L	L	H	D3-bar	D3
L	H	H	H or L	L	L	H	D3n-bar	D3n
H	L	L	↑	L	L	H	D4-bar	D4
H	L	L	H or L	L	L	H	D4n-bar	D4n
H	L	H	↑	L	L	H	D5-bar	D5
H	L	H	H or L	L	L	H	D5n-bar	D5n
H	H	L	↑	L	L	H	D6-bar	D6
H	H	L	H or L	L	L	H	D6n-bar	D6n

# CD74HCT356

TRUTH TABLE (Continued)

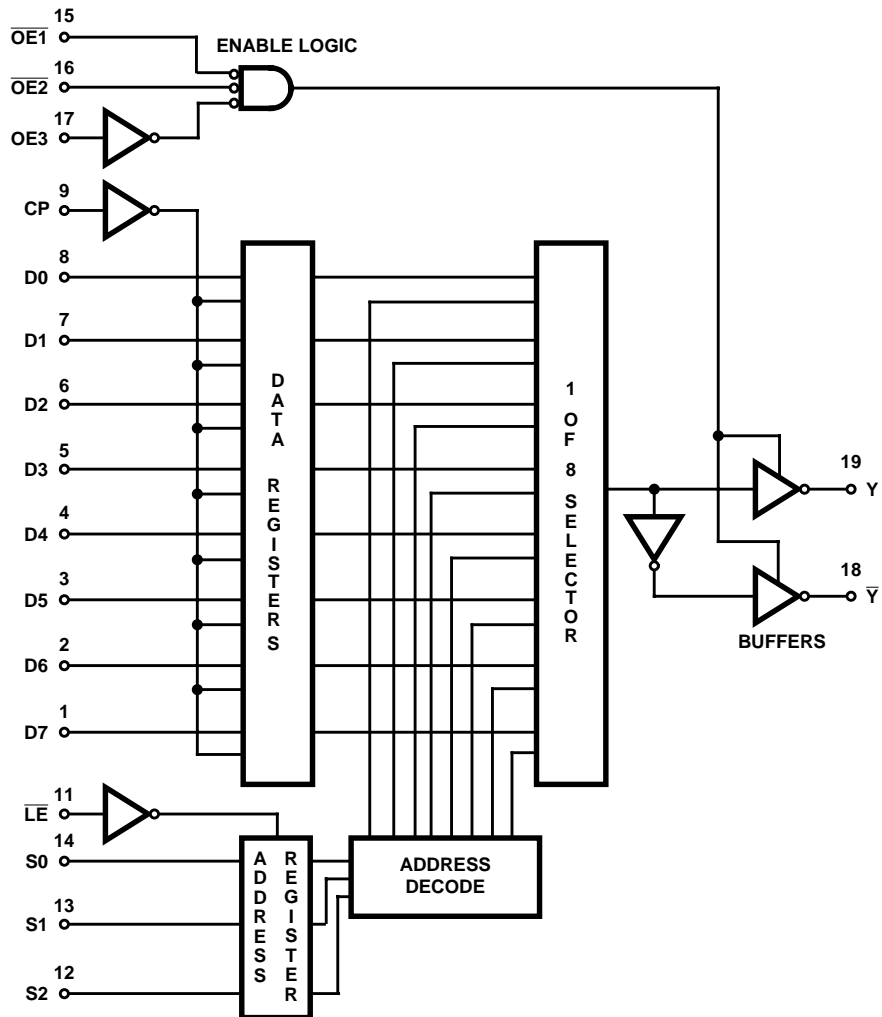
INPUTS							OUTPUTS	
SELECT (NOTE 1)			CLOCK	OUTPUT ENABLES				
S2	S1	S0	CP	$\overline{OE1}$	$\overline{OE2}$	OE3	$\overline{Y}$	Y
H	H	H	↑	L	L	H	$\overline{D7}$	D7
H	H	H	H or L	L	L	H	$\overline{D7}_n$	D7 <sub>n</sub>

H = High Voltage Level (Steady State); L = Low Voltage Level (Steady State); ↑ = Transition from Low to High Level;  
 X = Don't Care; Z = High-Impedance State (Off State); D0<sub>n</sub>...D7<sub>n</sub> = the level of steady-state inputs D0 through D7, respectively,  
 before the most recent low-to-high transition of data control.

NOTE:

1. This column shows the input address setup with  $\overline{LE}$  low.

## Block Diagram



Logic Diagram

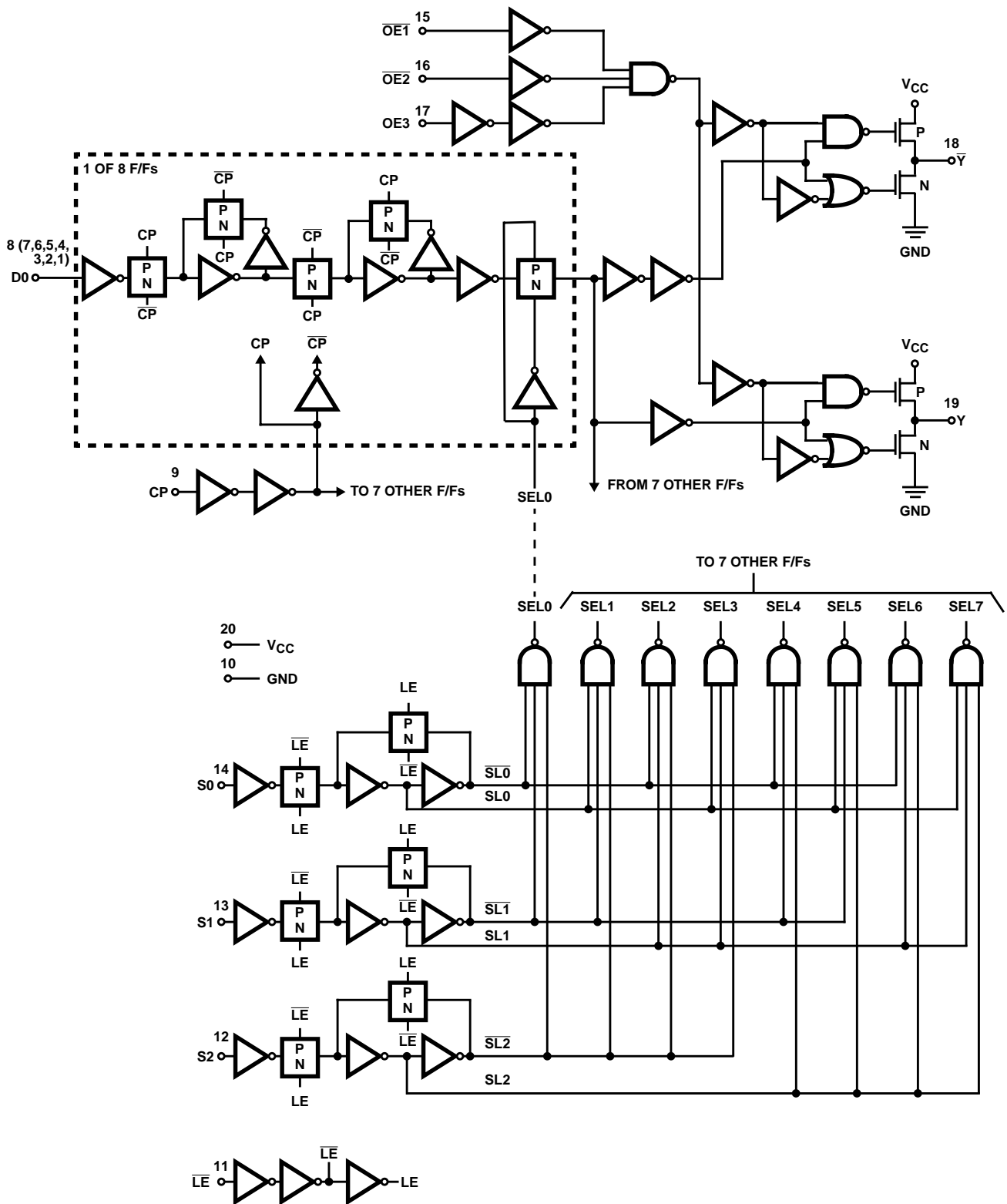


FIGURE 1. LOGIC DIAGRAM

# CD74HCT356

## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 7V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Drain Current, per Output, $I_O$	
For $-0.5V < V_O < V_{CC} + 0.5V$ .....	$\pm 35mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ .....	$\pm 50mA$

## Thermal Information

Thermal Resistance (Typical, Note 2)	$\theta_{JA}$ ( $^{\circ}C/W$ )
E (PDIP) Package .....	69
M (SOIC) Package .....	58
Maximum Junction Temperature .....	$150^{\circ}C$
Maximum Storage Temperature Range .....	$-65^{\circ}C$ to $150^{\circ}C$
Maximum Lead Temperature (Soldering 10s) .....	$300^{\circ}C$ (SOIC - Lead Tips Only)

## Operating Conditions

Temperature Range, $T_A$ .....	$-55^{\circ}C$ to $125^{\circ}C$
Supply Voltage Range, $V_{CC}$ .....	4.5V to 5.5V
DC Input or Output Voltage, $V_I, V_O$ .....	0V to $V_{CC}$
Input Rise and Fall Time	
2V .....	1000ns (Max)
4.5V .....	500ns (Max)
6V .....	400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

- The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25 $^{\circ}C$			-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
High Level Input Voltage	$V_{IH}$	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	$V_{IL}$	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	$I_I$	$V_{CC}$ to GND	0	5.5	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu A$
Quiescent Device Current	$I_{CC}$	$V_{CC}$ or GND	0	5.5	-	-	8	-	80	-	160	$\mu A$
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	$\Delta I_{CC}$ (Note 3)	$V_{CC}$ -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	$\mu A$
3-State Leakage Current	$I_{OZ}$	$V_{IL}$ or $V_{IH}$	$V_O = V_{CC}$ or GND	5.5	-	-	$\pm 0.5$	-	$\pm 5$	-	$\pm 10$	$\mu A$

### NOTE:

- For dual-supply systems theoretical worst case ( $V_I = 2.4V$ ,  $V_{CC} = 5.5V$ ) specification is 1.8mA.

## CD74HCT356

### Input Loading Table

INPUT	UNIT LOADS
D0-D7	0.50
S0, S1, S3	0.70
$\overline{OE1}$ , $\overline{OE2}$	0.80
OE3	0.25
$\overline{LE}$	0.25
CP	0.60

NOTE: Unit Load is  $\Delta I_{CC}$  limit specified in DC Electrical Specifications table, e.g., 360 $\mu$ A max at 25 $^{\circ}$ C.

### Prerequisite For Switching Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25 $^{\circ}$ C			-40 $^{\circ}$ C TO 85 $^{\circ}$ C		-55 $^{\circ}$ C TO 125 $^{\circ}$ C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
CP Pulse Width	$t_{PLH}$ , $t_{PHL}$	-	4.5	16	20	-	25	-	30	-	ns
$\overline{LE}$ Pulse Width	$t_{PLH}$ , $t_{PHL}$	-	4.5	16	20	-	25	-	30	-	ns
Setup Times Dn $\rightarrow \overline{E}$	$t_{SU}$	-	4.5	5	7	-	9	-	11	-	ns
Setup Times Sn $\rightarrow \overline{LE}$	$t_{SU}$	-	4.5	5	7	-	9	-	11	-	ns
Hold Times Dn $\rightarrow \overline{E}$	$t_H$	-	4.5	9	9	-	11	-	14	-	ns
Hold Times Sn $\rightarrow \overline{LE}$	$t_H$	-	4.5	12	12	-	15	-	18	-	ns

# CD74HCT356

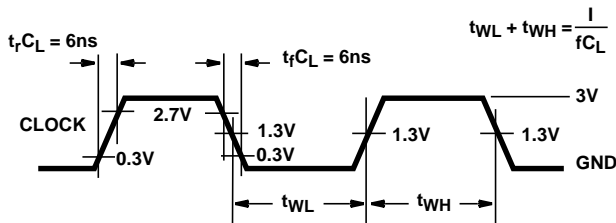
## Switching Specifications Input $t_r, t_f = 6\text{ns}$

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS	
				TYP	MAX	MAX	MAX		
Propagation Delay, $CP \rightarrow Y, \bar{Y}$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	51	64	77	ns	
		$C_L = 15\text{pF}$	5	22	-	-	-	ns	
Propagation Delay, $S_n \rightarrow Y, \bar{Y}$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	59	74	89	ns	
		$C_L = 15\text{pF}$	5	25	-	-	-	ns	
Propagation Delay, $\bar{L}\bar{E} \rightarrow Y, \bar{Y}$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	63	79	94	ns	
		$C_L = 15\text{pF}$	5	25	-	-	-	ns	
Output Disabling Time	$t_{PLZ}, t_{PHZ}$	$C_L = 50\text{pF}$	4.5	-	33	41	50	ns	
		$t_{PLZ}$	$C_L = 15\text{pF}$	5	13	-	-	-	ns
		$t_{PHZ}$	$C_L = 15\text{pF}$	5	15	-	-	-	ns
Output Enabling Time	$t_{PLZ}, t_{PHZ}$	$C_L = 50\text{pF}$	4.5	-	34	43	51	ns	
		$C_L = 15\text{pF}$	5	14	-	-	-	ns	
Output Transition Time	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	4.5	-	12	15	18	ns	
Input Capacitance	$C_{IN}$	-	-	-	10	10	10	pF	
3-State Capacitance	$C_O$	-	-	-	20	20	20	pF	
Power Dissipation Capacitance (Notes 4, 5)	$C_{PD}$	-	5	52	-	-	-	pF	

**NOTES:**

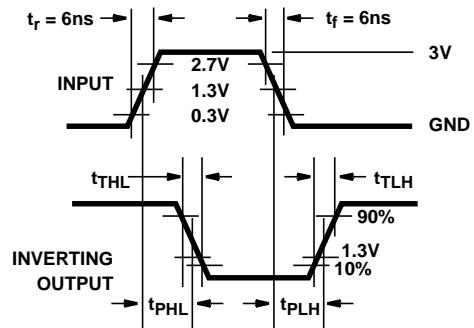
4.  $C_{PD}$  is used to determine the dynamic power consumption, per device.
5.  $P_D = V_{CC}^2 (C_{PD} + C_L) f_i$  where  $f_i$  = Input Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

### Test Circuits and Waveforms



NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

**FIGURE 2. CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**



**FIGURE 3. TRANSITION TIMES AND PROPAGATION-DELAY TIMES, COMBINATION LOGIC**

Test Circuits and Waveforms (Continued)

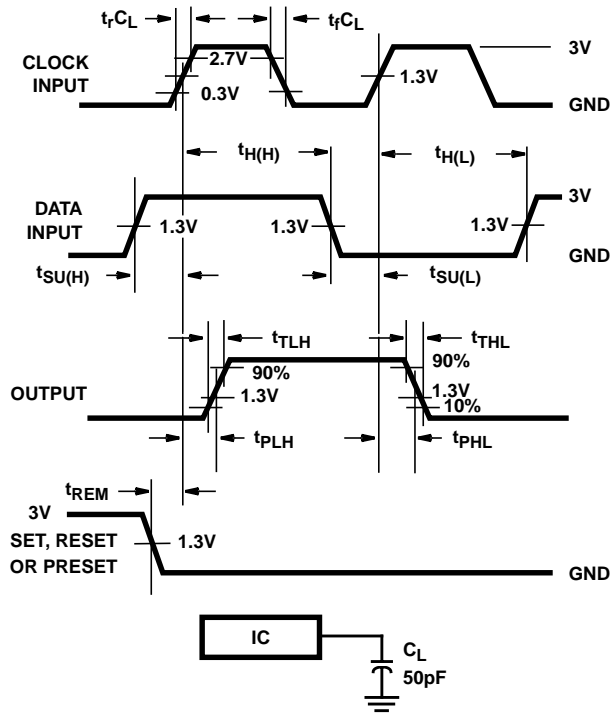


FIGURE 4. SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION-DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

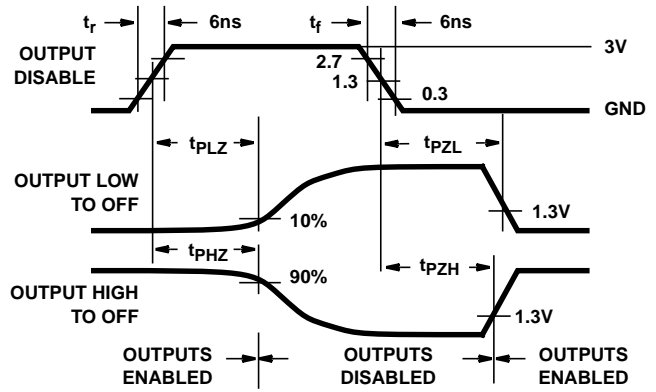
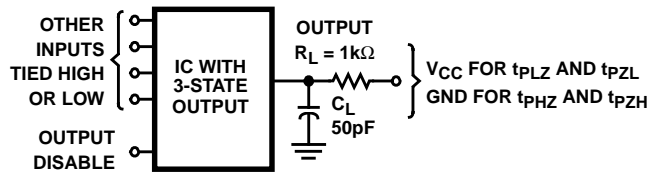


FIGURE 5. 3-STATE PROPAGATION-DELAY WAVEFORM



NOTE: Open-drain waveforms  $t_{PLZ}$  and  $t_{PZL}$  are the same as those for 3-state shown on the left. The test circuit is Output  $R_L = 1k\Omega$  to  $V_{CC}$ ,  $C_L = 50pF$ .

FIGURE 6. 3-STATE PROPAGATION-DELAY TEST CIRCUIT



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CD74HCT356E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HCT356EE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HCT356M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT356M96E4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT356M96G4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

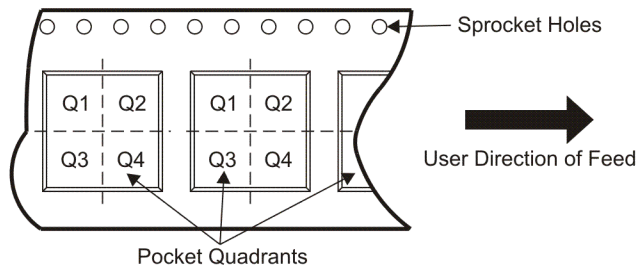
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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HCT356M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HCT356M96	SOIC	DW	20	2000	346.0	346.0	41.0

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
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