

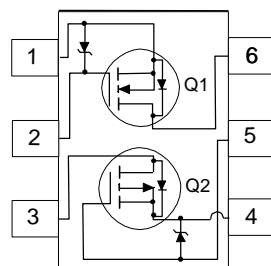
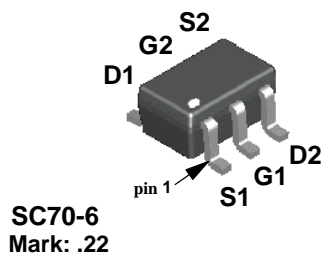
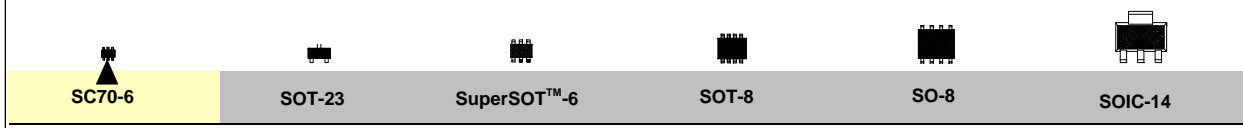
FDG6322C Dual N & P Channel Digital FET

General Description

These dual N & P-Channel logic level enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. This device has been designed especially for low voltage applications as a replacement for bipolar digital transistors and small signal MOSFETs. Since bias resistors are not required, this dual digital FET can replace several different digital transistors, with different bias resistor values.

Features

- N-Ch 0.22 A, 25 V, $R_{DS(ON)} = 4.0 \Omega @ V_{GS} = 4.5 \text{ V}$,
 $R_{DS(ON)} = 5.0 \Omega @ V_{GS} = 2.7 \text{ V}$.
- P-Ch -0.41 A, -25V, $R_{DS(ON)} = 1.1 \Omega @ V_{GS} = -4.5 \text{ V}$,
 $R_{DS(ON)} = 1.5 \Omega @ V_{GS} = -2.7 \text{ V}$.
- Very small package outline SC70-6.
- Very low level gate drive requirements allowing direct operation in 3 V circuits ($V_{GS(th)} < 1.5 \text{ V}$).
- Gate-Source Zener for ESD ruggedness (>6kV Human Body Model).



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless other wise noted

Symbol	Parameter	N-Channel	P-Channel	Units
V_{DS}	Drain-Source Voltage	25	-25	V
V_{GS}	Gate-Source Voltage	8	-8	V
I_D	Drain Current - Continuous	0.22	-0.41	A
	- Pulsed	0.65	-1.2	
P_D	Maximum Power Dissipation (Note 1)	0.3		W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150		$^\circ\text{C}$
ESD	Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100pf / 1500 Ohm)	6		kV

THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note1)	415	$^\circ\text{C/W}$
-----------------	---	-----	--------------------

DMOS Electrical Characteristics ($T_A = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	N-Ch	25			V
		$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-25			
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to $25\text{ }^\circ\text{C}$	N-Ch		25		mV/ $^\circ\text{C}$
		$I_D = -250\text{ }\mu\text{A}$, Referenced to $25\text{ }^\circ\text{C}$	P-Ch		-22		
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$, $T_J = 55\text{ }^\circ\text{C}$	N-Ch			1 10	μA
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$, $T_J = 55\text{ }^\circ\text{C}$	P-Ch			-1 -10	
I_{GSS}	Gate - Body Leakage Current	$V_{GS} = 8\text{ V}, V_{DS} = 0\text{ V}$	N-Ch			100	nA
		$V_{GS} = -8\text{ V}, V_{DS} = 0\text{ V}$	P-Ch			-100	nA
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N-Ch	0.65	0.85	1.5	V
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-0.65	-0.82	-1.5	
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to $25\text{ }^\circ\text{C}$	N-Ch		-2.1		mV/ $^\circ\text{C}$
		$I_D = -250\text{ }\mu\text{A}$, Referenced to $25\text{ }^\circ\text{C}$	P-Ch		2.1		
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 4.5\text{ V}, I_D = 0.22\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$	N-Ch		2.6	4	Ω
		$V_{GS} = 2.7\text{ V}, I_D = 0.19\text{ A}$			5.3	7	
		$V_{GS} = -4.5\text{ V}, I_D = -0.41\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$		P-Ch		0.85	
		$V_{GS} = -2.7\text{ V}, I_D = -0.25\text{ A}$			1.2	1.9	
					1.15	1.5	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$	N-Ch	0.22			A
		$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	P-Ch	-0.41			
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 0.22\text{ A}$	N-Ch		0.2		S
		$V_{DS} = -5\text{ V}, I_D = -0.5\text{ A}$	P-Ch		0.9		
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	N-Channel $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}$	N-Ch		9.5		pF
			P-Ch		62		
C_{oss}	Output Capacitance	f = 1.0 MHz P-Channel	N-Ch		6		
			P-Ch		34		
C_{rss}	Reverse Transfer Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}$, f = 1.0 MHz	N-Ch		1.3		
			P-Ch		10		

Electrical Characteristics (continued)

SWITCHING CHARACTERISTICS (Note 2)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
$t_{D(on)}$	Turn - On Delay Time	N-Channel $V_{DD} = 5\text{ V}, I_D = 0.5\text{ A},$	N-Ch		5	10	nS
			P-Ch		7	15	
t_r	Turn - On Rise Time	$V_{GS} = 4.5\text{ V}, R_{GEN} = 50\ \Omega$	N-Ch		4.5	10	nS
			P-Ch		8	16	
$t_{D(off)}$	Turn - Off Delay Time	P-Channel $V_{DD} = -5\text{ V}, I_D = -0.5\text{ A},$	N-Ch		4	8	nS
			P-Ch		55	80	
t_f	Turn - Off Fall Time	$V_{GS} = -4.5\text{ V}, R_{GEN} = 50\ \Omega$	N-Ch		3.2	7	nS
			P-Ch		35	60	
Q_g	Total Gate Charge	N-Channel $V_{DS} = 5\text{ V}, I_D = 0.22\text{ A},$	N-Ch		0.29	0.4	nC
			P-Ch		1.1	1.5	
Q_{gs}	Gate-Source Charge	$V_{GS} = 4.5\text{ V}$	N-Ch		0.12		nC
			P-Ch		0.31		
Q_{gd}	Gate-Drain Charge	P-Channel $V_{DS} = -5\text{ V}, I_D = -0.41\text{ A},$ $V_{GS} = -4.5\text{ V}$	N-Ch		0.03		nC
			P-Ch		0.29		

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I_S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch			0.25	A
			P-Ch			-0.25	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 0.5\text{ A}$ (Note 2)	N-Ch		0.8	1.2	V
		$V_{GS} = 0\text{ V}, I_S = -0.5\text{ A}$ (Note 2)	P-Ch		-0.85	-1.2	

Notes:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA} = 415^\circ\text{C/W}$ on minimum mounting pad on FR-4 board in still air.
- Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

Typical Electrical Characteristics: N-Channel

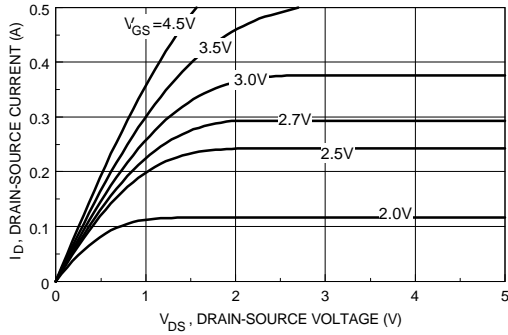


Figure 1. On-Region Characteristics.

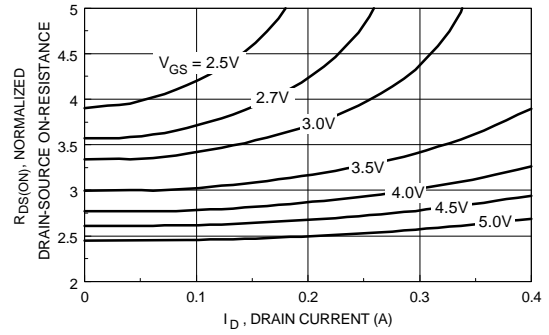


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

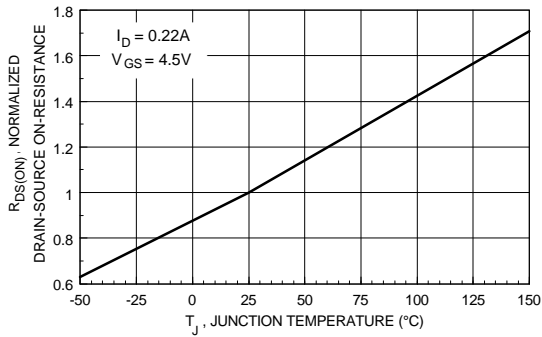


Figure 3. On-Resistance Variation with Temperature.

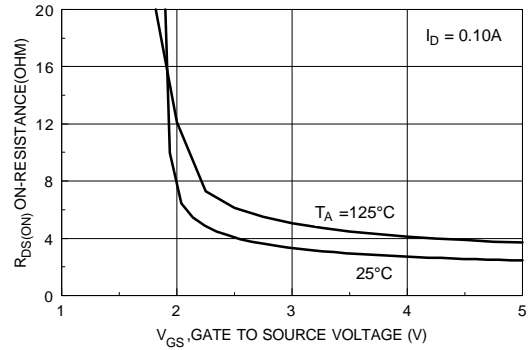


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

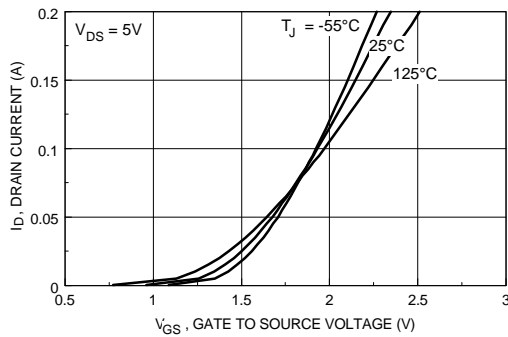


Figure 5. Transfer Characteristics.

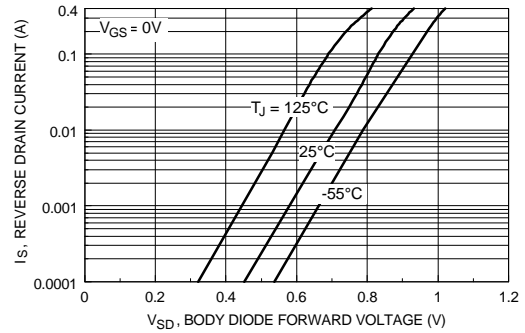


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical Characteristics: N-Channel (continued)

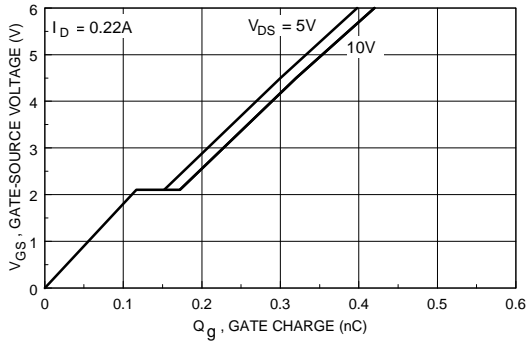


Figure 7. Gate Charge Characteristics.

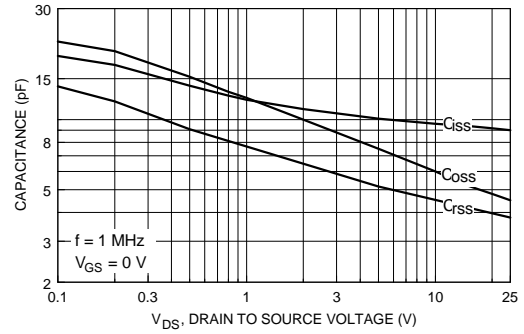


Figure 8. Capacitance Characteristics.

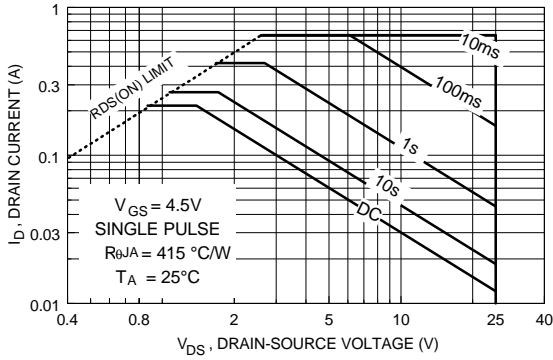


Figure 9. Maximum Safe Operating Area.

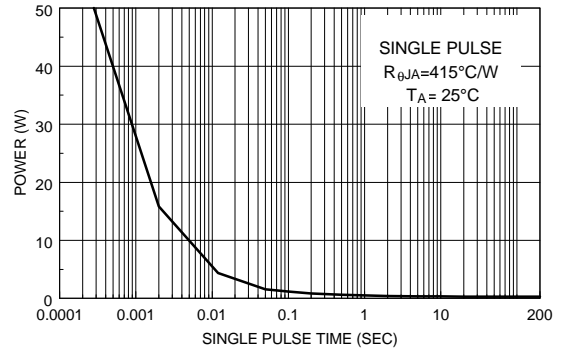


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Electrical Characteristics: P-Channel

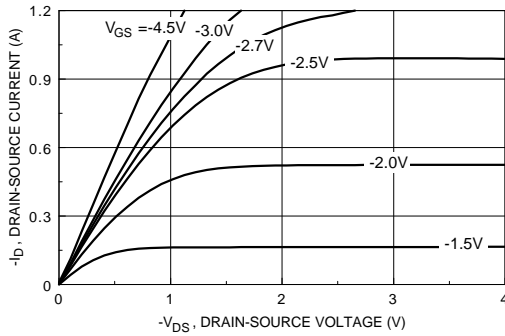


Figure 11. On-Region Characteristics.

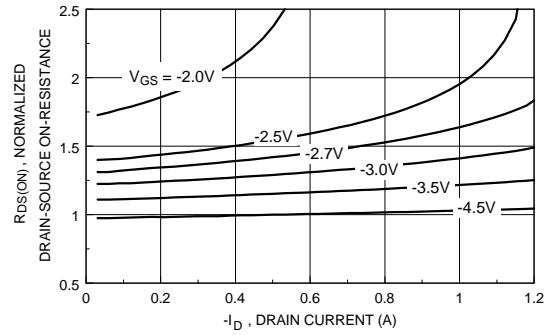


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

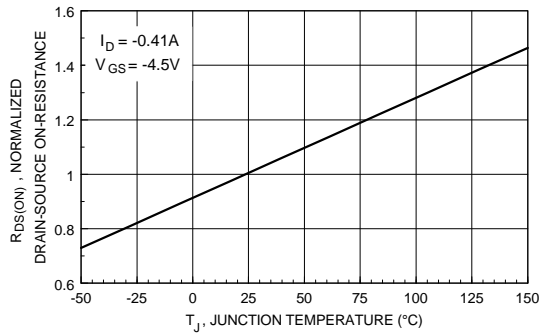


Figure 13. On-Resistance Variation with Temperature.

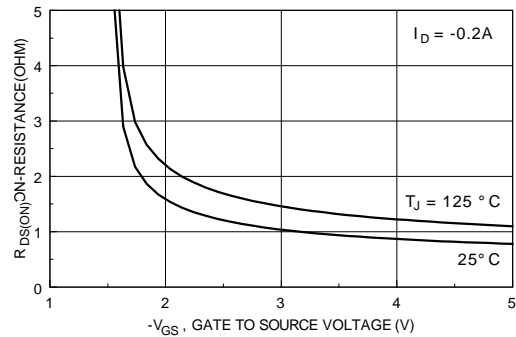


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

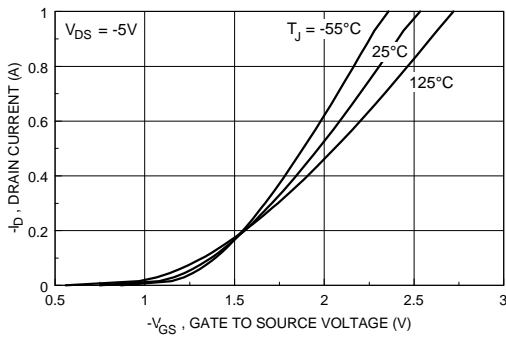


Figure 15. Transfer Characteristics.

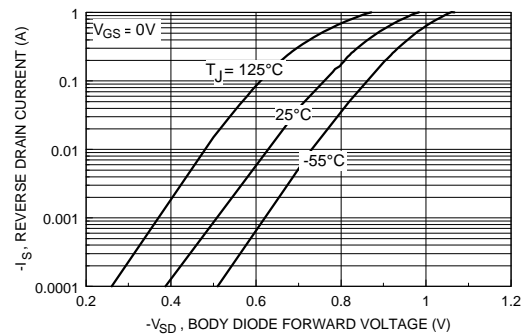


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical Characteristics: P-Channel (continued)

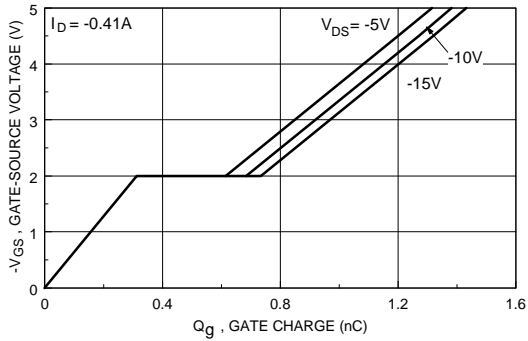


Figure 17. Gate Charge Characteristics.

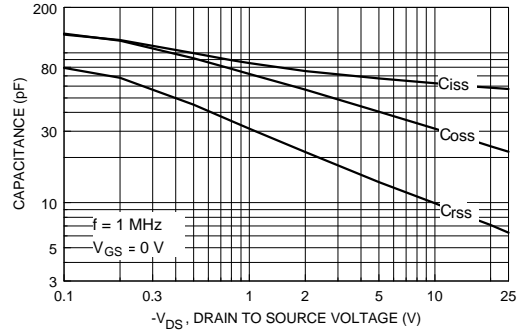


Figure 18. Capacitance Characteristics.

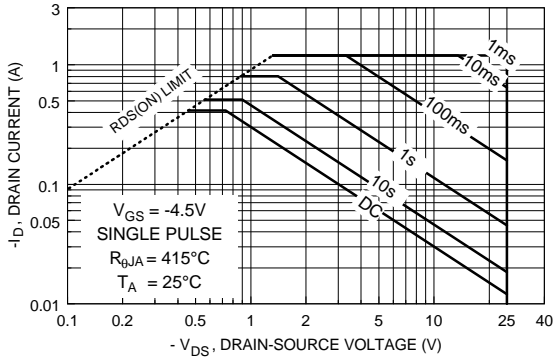


Figure 19. Maximum Safe Operating Area.

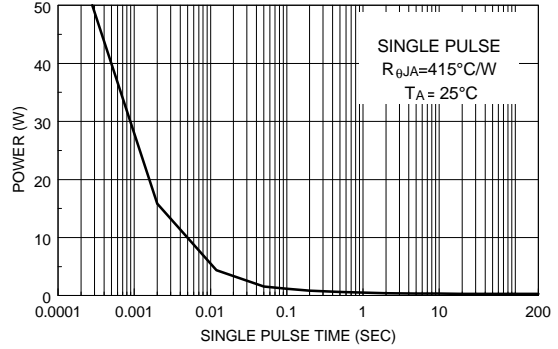


Figure 20. Single Pulse Maximum Power Dissipation.

Typical Thermal Characteristics: N & P-Channel (continued)

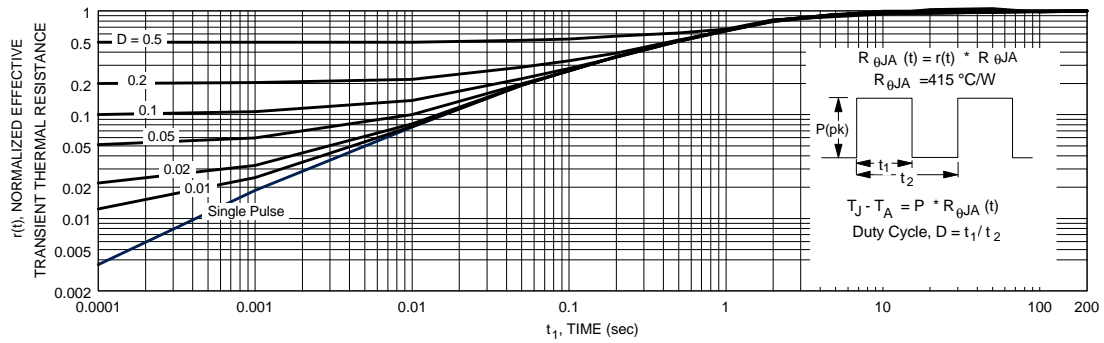




Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in note 1.
 Transient thermal response will change depending on the circuit board design.



TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

- | | | | |
|---|------------------------|----------------------------------|----------------------|
| ACEx® | FPS™ | PDP SPM™ | The Power Franchise® |
| Build it Now™ | F-PFS™ | Power-SPM™ | the power franchise |
| CorePLUS™ | FRFET® | PowerTrench® | TinyBoost™ |
| CorePOWER™ | Global Power Resource™ | Programmable Active Droop™ | TinyBuck™ |
| CROSSVOL™ | Green FPS™ | QFET® | TinyLogic® |
| CTL™ | Green FPS™ e-Series™ | QS™ | TINYOPTO™ |
| Current Transfer Logic™ | GTO™ | Quiet Series™ | TinyPower™ |
| EcoSPARK® | IntelliMAX™ | RapidConfigure™ | TinyPWM™ |
| EfficientMax™ | ISOPLANAR™ | Saving our world, 1mW at a time™ | SmartMax™ |
| EZSWITCH™ * | MegaBuck™ | SmartMax™ | SMART START™ |
|  | MICROCOUPLER™ | SMART START™ | SPM® |
|  | MicroFET™ | SPM® | STEALTH™ |
| Fairchild® | MicroPak™ | SPM® | SuperFET™ |
| Fairchild Semiconductor® | MillerDrive™ | SuperSOT™-3 | SuperSOT™-6 |
| FACT Quiet Series™ | MotionMax™ | SuperSOT™-8 | SupreMOS™ |
| FACT® | Motion-SPM™ | SyncFET™ | SYSTEM GENERAL® |
| FAST® | OPTOLOGIC® | UHC® | UHC® |
| FastvCore™ | OPTOPLANAR® | Ultra FRFET™ | UniFET™ |
| FlashWriter® * | | VCX™ | VisualMax™ |

* EZSWITCH™ and FlashWriter® are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
- A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.