Data Sheet FN2921.11

110MHz, High Slew Rate, High Output Current Buffer

The HA-5002 is a monolithic, wideband, high slew rate, high output current, buffer amplifier.

Utilizing the advantages of the Intersil D.I. technologies, the HA-5002 current buffer offers 1300V/µs slew rate with 110MHz of bandwidth. The ±200mA output current capability is enhanced by a 3Ω output impedance.

The monolithic HA-5002 will replace the hybrid LH0002 with corresponding performance increases. These characteristics range from the 3000kΩ input impedance to the increased output voltage swing. Monolithic design technologies have allowed a more precise buffer to be developed with more than an order of magnitude smaller gain error.

The HA-5002 will provide many present hybrid users with a higher degree of reliability and at the same time increase overall circuit performance.

For the military grade product, refer to the HA-5002/883 datasheet.

Features

- Voltage Gain. 0.995
- High Input Impedance 3000kΩ
- Low Output Impedance 3Ω
- Very High Slew Rate 1300V/µs
- Very Wide Bandwidth. 110MHz
- High Output Current. . . . . ±200mA
- Pulsed Output Current 400mA
- Monolithic Construction
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Line Driver
- Data Acquistion
- 110MHz Buffer
- Radara Cable Driver
- High Power Current Booster
- High Power Current Source
- Sample and Holds
- Video Products

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HA2-5002-2	HA2-5002-2	-55 to 125	8 Pin Metal Can	T8.C
HA2-5002-5	HA2-5002-5	0 to 75	8 Pin Metal Can	T8.C
HA3-5002-5	HA3-5002-5	0 to 75	8 Ld PDIP	E8.3
HA3-5002-5Z (Note)	HA3-5002-5Z	0 to 75	8 Ld PDIP* (Pb-free)	E8.3
HA4P5002-5	HA4P5002-5	0 to 75	20 Ld PLCC	N20.35
HA4P5002-5Z (Note)	HA4P5002-5Z	0 to 75	20 Ld PLCC (Pb-free)	N20.35
HA9P5002-5	50025	0 to 75	8 Ld SOIC	M8.15
HA9P5002-5Z (Note)	50025Z	0 to 75	8 Ld SOIC (Pb-free)	M8.15
HA9P5002-9	50029	-40 to 85	8 Ld SOIC	M8.15
HA9P5002-9Z (Note)	50029Z	-40 to 85	8 Ld SOIC (Pb-free)	M8.15

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 44V
Input Voltage . . . . . V_1+ to V_1-
Output Current (Continuous) . . . . . ±200mA
Output Current (50ms On, 1s Off) . . . . . ±400mA

Operating Conditions

Temperature Range
HA-5002-2 . . . . . -55°C to 125°C
HA-5002-5 . . . . . 0°C to 75°C
HA-5002-9 . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package*	92	N/A
Metal Can Package	155	67
PLCC Package	74	N/A
SOIC Package	157	N/A

Max Junction Temperature (Hermetic Packages, Note 1) . . . . . 175°C
Max Junction Temperature (Plastic Packages, Note 1) . . . . . 150°C
Max Storage Temperature Range . . . . . -65°C to 150°C
Max Lead Temperature (Soldering 10s) . . . . . 300°C
(PLCC and SOIC - Lead Tips Only)

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation, including load conditions, must be designed to maintain the maximum junction temperature below 175°C for the can packages, and below 150°C for the plastic packages.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{SUPPLY} = ±12V to ±15V, R_S = 50Ω, R_L = 1kΩ, C_L = 10pF, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	HA-5002-2			HA-5002-5, -9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS									
Offset Voltage		25	-	5	20	-	5	20	mV
		Full	-	10	30	-	10	30	mV
Average Offset Voltage Drift		Full	-	30	-	-	30	-	µV/°C
Bias Current		25	-	2	7	-	2	7	µA
		Full	-	3.4	10	-	2.4	10	µA
Input Resistance		Full	1.5	3	-	1.5	3	-	MΩ
Input Noise Voltage	10Hz-1MHz	25	-	18	-	-	18	-	μV_{P-P}
TRANSFER CHARACTERISTICS									
Voltage Gain (V_{OUT} = ±10V)	R_L = 50Ω	25	-	0.900	-	-	0.900	-	V/V
	R_L = 100Ω	25	-	0.971	-	-	0.971	-	V/V
	R_L = 1kΩ	25	-	0.995	-	-	0.995	-	V/V
	R_L = 1kΩ	Full	0.980	-	-	0.980	-	-	V/V
-3dB Bandwidth	V_{IN} = $1V_{P-P}$	25	-	110	-	-	110	-	MHz
AC Current Gain		25	-	40	-	-	40	-	A/mA
OUTPUT CHARACTERISTICS									
Output Voltage Swing	R_L = 100Ω	25	±10	±10.7	-	±10	±11.2	-	V
	R_L = 1kΩ, V_S = ±15V	Full	±10	±13.5	-	±10	±13.9	-	V
	R_L = 1kΩ, V_S = ±12V	Full	±10	±10.5	-	±10	±10.5	-	V
Output Current	V_{IN} = ±10V, R_L = 40Ω	25	-	220	-	-	220	-	mA
Output Resistance		Full	-	3	10	-	3	10	Ω
Harmonic Distortion	V_{IN} = $1V_{RMS}$, f = 10kHz	25	-	<0.005	-	-	<0.005	-	%
TRANSIENT RESPONSE									
Full Power Bandwidth (Note 3)		25	-	20.7	-	-	20.7	-	MHz
Rise Time		25	-	3.6	-	-	3.6	-	ns
Propagation Delay		25	-	2	-	-	2	-	ns
Overshoot		25	-	30	-	-	30	-	%
Slew Rate		25	1.0	1.3	-	1.0	1.3	-	V/ns
Settling Time	To 0.1%	25	-	50	-	-	50	-	ns

Electrical Specifications V_{SUPPLY} = ±12V to ±15V, R_S = 50Ω, R_L = 1kΩ, C_L = 10pF, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	HA-5002-2			HA-5002-5, -9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Differential Gain	R_L = 500Ω	25	-	0.06	-	-	0.06	-	%
Differential Phase	R_L = 500Ω	25	-	0.22	-	-	0.22	-	Degrees
POWER REQUIREMENTS									
Supply Current		25	-	8.3	-	-	8.3	-	mA
		Full	-	-	10	-	-	10	mA
Power Supply Rejection Ratio	A_V = 10V	Full	54	64	-	54	64	-	dB

NOTE:

3. $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$; V_P = 10V.

Test Circuit and Waveforms

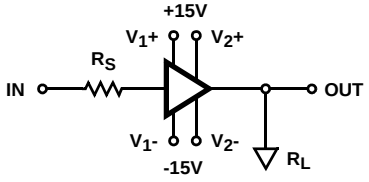
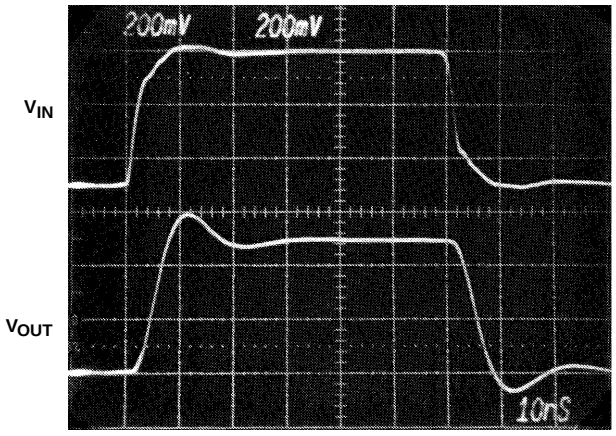
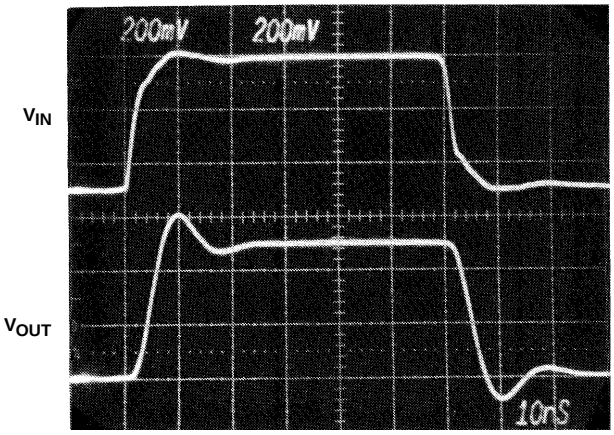


FIGURE 1. LARGE AND SMALL SIGNAL RESPONSE



R_S = 50Ω, R_L = 100Ω

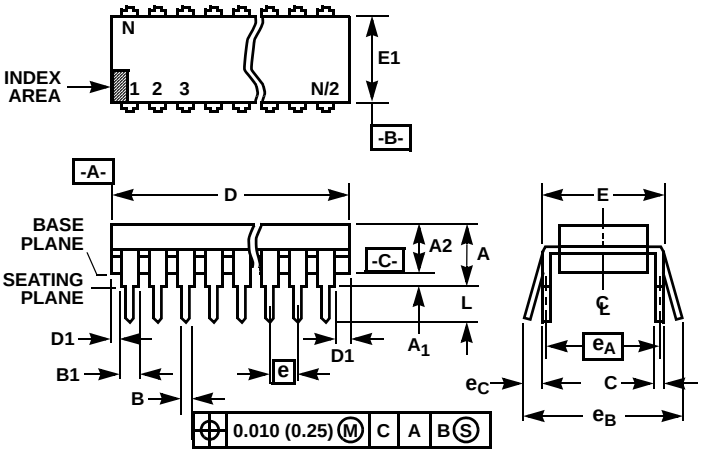
SMALL SIGNAL WAVEFORMS



R_S = 50Ω, R_L = 1kΩ

SMALL SIGNAL WAVEFORMS

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

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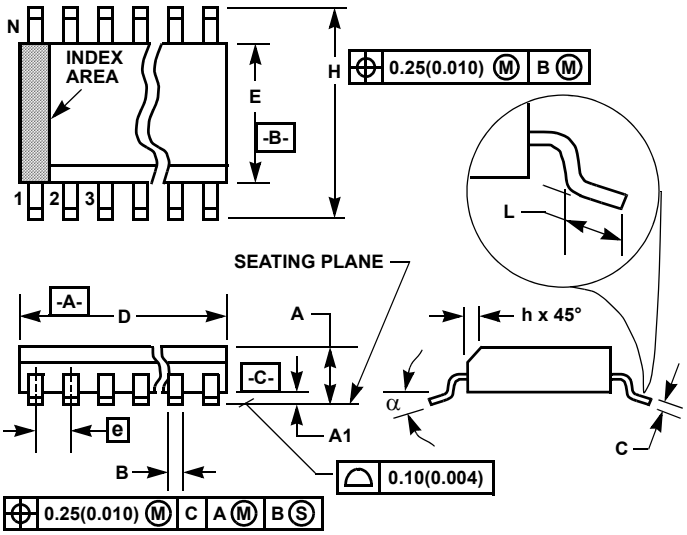
Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

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