100MHz Current Feedback Video Amplifier With Disable

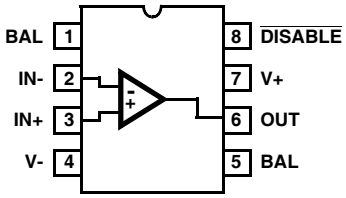
The HA-5020 is a wide bandwidth, high slew rate amplifier optimized for video applications and gains between 1 and 10. Manufactured on Intersil's Reduced Feature Complementary Bipolar DI process, this amplifier uses current mode feedback to maintain higher bandwidth at a given gain than conventional voltage feedback amplifiers. Since it is a closed loop device, the HA-5020 offers better gain accuracy and lower distortion than open loop buffers.

The HA-5020 features low differential gain and phase and will drive two double terminated 75Ω coax cables to video levels with low distortion. Adding a gain flatness performance of 0.1dB makes this amplifier ideal for demanding video applications. The bandwidth and slew rate of the HA-5020 are relatively independent of closed loop gain. The 100MHz unity gain bandwidth only decreases to 60MHz at a gain of 10. The HA-5020 used in place of a conventional op amp will yield a significant improvement in the speed power product. To further reduce power, HA-5020 has a disable function which significantly reduces supply current, while forcing the output to a true high impedance state. This allows the outputs of multiple amplifiers to be wire-OR'd into multiplexer configurations. The device also includes output short circuit protection and output offset voltage adjustment.

For multi channel versions of the HA-5020 see the HA5022 dual with disable, HA5023 dual, HA5013 triple and HA5024 quad with disable op amp data sheets.

Pinout

HA-5020
(PDIP, SOIC)
TOP VIEW



Features

- Wide Unity Gain Bandwidth 100MHz
- Slew Rate. 800V/μs
- Output Current . . . . . ±30mA (Min)
- Drives 3.5V into 75Ω
- Differential Gain 0.03%
- Differential Phase. . . . . .0.03°
- Low Input Voltage Noise . . . . . 4.5nV/$\sqrt{Hz}$
- Low Supply Current . . . . . 10mA (Max)
- Wide Supply Range . . . . . ±5V to ±15V
- Output Enable/Disable
- High Performance Replacement for EL2020
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Unity Gain Video/Wideband Buffer
- Video Gain Block
- Video Distribution Amp/Coax Cable Driver
- Flash A/D Driver
- Waveform Generator Output Driver
- Current to Voltage Converter; D/A Output Buffer
- Radar Systems
- Imaging Systems

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HA3-5020-5	HA3-5020-5	0 to 75	8 Ld PDIP	E8.3
HA3-5020-5Z (Note)	HA3-5020-5Z	0 to 75	8 Ld PDIP (Pb-free)	E8.3
HA9P5020-5	50205	0 to 75	8 Ld SOIC	M8.15
HA9P5020-5Z (Note)	50205Z	0 to 75	8 Ld SOIC (Pb-free)	M8.15
HA9P5020-5X96	50205	0 to 75	8 Ld SOIC Tape and Reel	M8.15
HA9P5020-5ZX96 (Note)	50205Z	0 to 75	8 Ld SOIC Tape and Reel (Pb-free)	M8.15

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 36V
DC Input Voltage . . . . . $\pm V_{SUPPLY}$
Differential Input Voltage 10V
Output Current . . . . . Short Circuit Protected

Operating Conditions

Temperature Range
HA-5020-5 . . . . . 0°C to 75°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	120	N/A
SOIC Package	165	N/A

Maximum Junction Temperature (Plastic Packages, Note 1) . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation, including output load, must be designed to maintain junction temperature below 150°C for plastic packages.
1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

$V_{SUPPLY} = \pm 15V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Input Offset Voltage (Notes 3, 14)		25	-	2	8	mV
		Full	-	-	10	mV
Average Input Offset Voltage Drift		Full	-	10	-	µV/°C
V_{IO} Common Mode Rejection Ratio (Note 14)	$V_{CM} = \pm 10V$	25	60	-	-	dB
		Full	50	-	-	dB
V_{IO} Power Supply Rejection Ratio (Note 14)	$\pm 4.5V \leq V_S \leq \pm 18V$	25	64	-	-	dB
		Full	60	-	-	dB
Non-Inverting Input (+IN) Current (Note 14)		25	-	3	8	µA
		Full	-	-	20	µA
+IN Common Mode Rejection	$V_{CM} = \pm 10V$	25	-	-	0.1	µA/V
		Full	-	-	0.5	µA/V
+IN Power Supply Rejection	$\pm 4.5V \leq V_S \leq \pm 18V$	25	-	-	0.06	µA/V
		Full	-	-	0.2	µA/V
Inverting Input (-IN) Current (Note 14)		25	-	12	20	µA
		Full	-	25	50	µA
-IN Common Mode Rejection	$V_{CM} = \pm 10V$	25	-	-	0.4	µA/V
		Full	-	-	0.5	µA/V
-IN Power Supply Rejection	$\pm 4.5V \leq V_S \leq \pm 18V$	25	-	-	0.2	µA/V
		Full	-	-	0.5	µA/V
TRANSFER CHARACTERISTICS						
Transimpedance (Notes 9, 14)		25	3500	-	-	V/mA
		Full	1000	-	-	V/mA
Open Loop DC Voltage Gain (Note 9)	$R_L = 400\Omega$, $V_{OUT} = \pm 10V$	25	70	-	-	dB
		Full	65	-	-	dB
Open Loop DC Voltage Gain	$R_L = 100\Omega$, $V_{OUT} = \pm 2.5V$	25	60	-	-	dB
		Full	55	-	-	dB

Electrical Specifications $V_{SUPPLY} = \pm15V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
OUTPUT CHARACTERISTICS						
Output Voltage Swing (Note 14)	$R_L = 150\Omega$	25 to 85	±12	±12.7	-	V
		-40 to 0	±11	±11.8	-	V
Output Current (Guaranteed by Output Voltage Test)		25	±30	±31.7	-	mA
		Full	±27.5	-	-	mA
POWER SUPPLY CHARACTERISTICS						
Quiescent Supply Current (Note 14)		Full	-	7.5	10	mA
Supply Current, Disabled (Note 14)	$\overline{DISABLE} = 0V$	Full	-	5	7.5	mA
$\overline{Disable}$ Pin Input Current	$\overline{DISABLE} = 0V$	Full	-	1.0	1.5	mA
Minimum Pin 8 Current to Disable (Note 4)		Full	350	-	-	µA
Maximum Pin 8 Current to Enable (Note 5)		Full	-	-	20	µA
AC CHARACTERISTICS ($A_V = +1$)						
Slew Rate (Note 6)		25	600	800	-	V/µs
		Full	500	700	-	V/µs
Full Power Bandwidth (Note 7) (Guaranteed by Slew Rate Test)		25	9.6	12.7	-	MHz
		Full	8.0	11.1	-	MHz
Rise Time (Note 8)		25	-	5	-	ns
Fall Time (Note 8)		25	-	5	-	ns
Propagation Delay (Notes 8, 14)		25	-	6	-	ns
-3dB Bandwidth (Note 14)	$V_{OUT} = 100mV$	25	-	100	-	MHz
Settling Time to 1%	10V Output Step	25	-	45	-	ns
Settling Time to 0.25%	10V Output Step	25	-	100	-	ns
AC CHARACTERISTICS ($A_V = +10$, $R_F = 383\Omega$)						
Slew Rate (Notes 6, 9)		25	900	1100	-	V/µs
		Full	700	-	-	V/µs
Full Power Bandwidth (Note 7) (Guaranteed by Slew Rate Test)		25	14.3	17.5	-	MHz
		Full	11.1	-	-	MHz
Rise Time (Note 8)		25	-	8	-	ns
Fall Time (Note 8)		25	-	8	-	ns
Propagation Delay (Notes 8, 14)		25	-	9	-	ns
-3dB Bandwidth	$V_{OUT} = 100mV$	25	-	60	-	MHz
Settling Time to 1%	10V Output Step	25	-	55	-	ns
Settling Time to 0.1%	10V Output Step	25	-	90	-	ns
INTERSIL VALUE ADDED SPECIFICATIONS						
Input Noise Voltage (Note 14)	f = 1kHz	25	-	4.5	-	$nV/\sqrt{Hz}$
+Input Noise Current (Note 14)	f = 1kHz	25	-	2.5	-	$pA/\sqrt{Hz}$
-Input Noise Current (Note 14)	f = 1kHz	25	-	25	-	$pA/\sqrt{Hz}$
Input Common Mode Range		Full	±10	±12	-	V
$-I_{BIAS}$ Adjust Range (Note 3)		Full	±25	±40	-	µA
Overshoot (Note 14)		25	-	7	-	%

Electrical Specifications $V_{SUPPLY} = \pm15V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
Output Current, Short Circuit (Note 14)	$V_{IN} = \pm10V$, $V_{OUT} = 0V$	Full	±50	±65	-	mA
Output Current, Disabled (Note 14)	$\overline{DISABLE} = 0V$, $V_{OUT} = \pm10V$	Full	-	-	1	µA
Output Disable Time (Notes 10, 14)		25	-	10	-	µs
Output Enable Time (Notes 11, 14)		25	-	200	-	ns
Supply Voltage Range		25	±5	-	±15	V
Output Capacitance, Disabled (Note 12)	$\overline{DISABLE} = 0V$	25	-	6	-	pF
VIDEO CHARACTERISTICS						
Differential Gain (Notes 13, 14)	$R_L = 150\Omega$	25	-	0.03	-	%
Differential Phase (Notes 13, 14)	$R_L = 150\Omega$	25	-	0.03	-	°
Gain Flatness	To 5MHz	25	-	0.1	-	dB

Electrical Specifications V+ = +5V, V- = -5V, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified. Parameters are not tested. The limits are guaranteed based on lab characterizations, and reflect lot-to-lot variation.

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Input Offset Voltage (Notes 3, 14)		25	-	2	8	mV
		Full	-	-	10	mV
Average Input Offset Voltage Drift		Full	-	10	-	µV/°C
V_{IO} Common Mode Rejection Ratio (Notes 14, 15)		25	50	-	-	dB
		Full	35	-	-	dB
V_{IO} Power Supply Rejection Ratio (Note 14)	$\pm3.5V \leq V_S \leq \pm6.5V$	25	55	-	-	dB
		Full	50	-	-	dB
Non-Inverting Input (+IN) Current (Note 14)		25	-	3	8	µA
		Full	-	-	20	µA
+IN Common Mode Rejection (Note 15)		25	-	-	0.1	µA/V
		Full	-	-	0.5	µA/V
+IN Power Supply Rejection	$\pm3.5V \leq V_S \leq \pm6.5V$	25	-	-	0.06	µA/V
		Full	-	-	0.2	µA/V
Inverting Input (-IN) Current (Note 14)		25	-	12	20	µA
		Full	-	25	50	µA
-IN Common Mode Rejection (Note 15)		25	-	-	0.4	µA/V
		Full	-	-	0.5	µA/V
-IN Power Supply Rejection	$\pm3.5V \leq V_S \leq \pm6.5V$	25	-	-	0.2	µA/V
		Full	-	-	0.5	µA/V
TRANSFER CHARACTERISTICS						
Transimpedance (Notes 9, 14)		25	1000	-	-	V/mA
		Full	850	-	-	V/mA
Open Loop DC Voltage Gain	$R_L = 400\Omega$, $V_{OUT} = \pm2.5V$	25	65	-	-	dB
		Full	60	-	-	dB

Electrical Specifications $V+ = +5V$, $V- = -5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified. Parameters are not tested. The limits are guaranteed based on lab characterizations, and reflect lot-to-lot variation. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
Open Loop DC Voltage Gain	$R_L = 100\Omega$, $V_{OUT} = \pm 2.5V$	25	50	-	-	dB
		Full	45	-	-	dB
OUTPUT CHARACTERISTICS						
Output Voltage Swing (Note 14)		25 to 85	±2.5	±3.0	-	V
		-40 to 0	±2.5	±3.0	-	V
Output Current (Guaranteed by Output Voltage Test)	$R_L = 100\Omega$	25	±16.6	±20	-	mA
		Full	±16.6	±20	-	mA
POWER SUPPLY CHARACTERISTICS						
Quiescent Supply Current (Note 14)		Full	-	7.5	10	mA
Supply Current, Disabled (Note 14)	$\overline{DISABLE} = 0V$	Full	-	5	7.5	mA
$\overline{Disable}$ Pin Input Current	$\overline{DISABLE} = 0V$	Full	-	1.0	1.5	mA
Minimum Pin 8 Current to Disable (Note 16)		Full	350	-	-	µA
Maximum Pin 8 Current to Enable (Note 5)		Full	-	-	20	µA
AC CHARACTERISTICS ($A_V = +1$)						
Slew Rate (Note 17)		25	215	400	-	V/µs
Full Power Bandwidth (Note 18)		25	22	28	-	MHz
Rise Time (Note 8)		25	-	6	-	ns
Fall Time (Note 8)		25	-	6	-	ns
Propagation Delay (Note 8)		25	-	6	-	ns
Overshoot		25	-	4.5	-	%
-3dB Bandwidth (Note 14)	$V_{OUT} = 100mV$	25	-	125	-	MHz
Settling Time to 1%	2V Output Step	25	-	50	-	ns
Settling Time to 0.25%	2V Output Step	25	-	75	-	ns
AC CHARACTERISTICS ($A_V = +2$, $R_F = 681\Omega$)						
Slew Rate (Note 17)		25	-	475	-	V/µs
Full Power Bandwidth (Note 18)		25	-	26	-	MHz
Rise Time (Note 8)		25	-	6	-	ns
Fall Time (Note 8)		25	-	6	-	ns
Propagation Delay (Note 8)		25	-	6	-	ns
Overshoot		25	-	12	-	%
-3dB Bandwidth (Note 14)	$V_{OUT} = 100mV$	25	-	95	-	MHz
Settling Time to 1%	2V Output Step	25	-	50	-	ns
Settling Time to 0.25%	2V Output Step	25	-	100	-	ns
AC CHARACTERISTICS ($A_V = +10$, $R_F = 383\Omega$)						
Slew Rate (Note 17)		25	350	475	-	V/µs
Full Power Bandwidth (Note 18)		25	28	38	-	MHz
Rise Time (Note 8)		25	-	8	-	ns
Fall Time (Note 8)		25	-	9	-	ns
Propagation Delay (Note 8)		25	-	9	-	ns
Overshoot		25	-	1.8	-	%

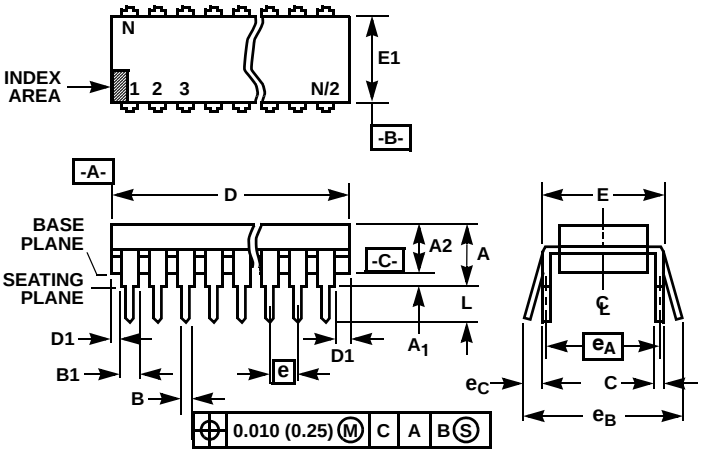
Electrical Specifications $V+ = +5V$, $V- = -5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified. Parameters are not tested. The limits are guaranteed based on lab characterizations, and reflect lot-to-lot variation. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
-3dB Bandwidth (Note 14)	V_{OUT} = 100mV	25	-	65	-	MHz
Settling Time to 1%	2V Output Step	25	-	75	-	ns
Settling Time to 0.25%	2V Output Step	25	-	130	-	ns
INTERSIL VALUE ADDED SPECIFICATIONS						
Input Noise Voltage (Note 14)	f = 1kHz	25	-	4.5	-	$nV/\sqrt{Hz}$
+Input Noise Current (Note 14)	f = 1kHz	25	-	2.5	-	$pA/\sqrt{Hz}$
-Input Noise Current (Note 14)	f = 1kHz	25	-	25	-	$pA/\sqrt{Hz}$
Input Common Mode Range		Full	±2.5V	–	-	V
Output Current, Short Circuit	$V_{IN} = \pm 2.5V$, V_{OUT} = 0V	Full	±40	±60	-	mA
Output Current, Disabled (Note 14)	$\overline{DISABLE}$ = 0V, $V_{OUT} = \pm 2.5V$, V_{IN} = 0V	Full	-	-	2	µA
Output Disable Time (Notes 14, 20)		25	-	40	-	µs
Output Enable Time (Notes 14, 21)		25	-	40	-	ns
Supply Voltage Range		25	±5	-	±15	V
Output Capacitance, Disabled (Note 19)	$\overline{DISABLE}$ = 0V	25	-	6	-	pF
VIDEO CHARACTERISTICS						
Differential Gain (Notes 13, 14)	$R_L = 150\Omega$	25	-	0.03	-	%
Differential Phase (Notes 13, 14)	$R_L = 150\Omega$	25	-	0.03	-	°
Gain Flatness	To 5MHz	25	-	0.1	-	dB

NOTES:

2. Suggested V_{OS} Adjust Circuit: The inverting input current ($-I_{BIAS}$) can be adjusted with an external 10kΩ pot between pins 1 and 5, wiper connected to V+. Since $-I_{BIAS}$ flows through the feedback resistor (R_F), the result is an adjustment in offset voltage. The amount of offset voltage adjustment is determined by the value of R_F ($\Delta V_{OS} = \Delta -I_{BIAS} * R_F$).
3. $R_L = 100\Omega$, $V_{IN} = 10V$. This is the minimum current which must be pulled out of the $\overline{Disable}$ pin in order to disable the output. The output is considered disabled when $-10mV \leq V_{OUT} \leq +10mV$.
4. V_{IN} = 0V. This is the maximum current that can be pulled out of the $\overline{Disable}$ pin with the HA-5020 remaining enabled. The HA-5020 is considered disabled when the supply current has decreased by at least 0.5mA.
5. V_{OUT} switches from -10V to +10V, or from +10V to -10V. Specification is from the 25% to 75% points.
6. $FPBW = \frac{Slew\ Rate}{2\pi V_{PEAK}}$; V_{PEAK} = 10V.
7. $R_L = 100\Omega$, V_{OUT} = 1V. Measured from 10% to 90% points for rise/fall times; from 50% points of input and output for propagation delay.
8. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.
9. V_{IN} = +10V, $\overline{Disable}$ = +15V to 0V. Measured from the 50% point of $\overline{Disable}$ to V_{OUT} = 0V.
10. V_{IN} = +10V, $\overline{Disable}$ = 0V to +15V. Measured from the 50% point of $\overline{Disable}$ to V_{OUT} = 10V.
11. V_{IN} = 0V, Force V_{OUT} from 0V to ±10V, $t_R = t_F$ = 50ns.
12. Measured with a VM700A video tester using a NTC-7 composite VITS.
13. See “Typical Performance Curves” for more information.
14. $V_{CM} = \pm 2.5V$. At -40°C product is tested at $V_{CM} = \pm 2.25V$ because short test duration does not allow self heating.
15. $R_L = 100\Omega$. V_{IN} = 2.5V. This is the minimum current which must be pulled out of the $\overline{Disable}$ pin in order to disable the output. The output is considered disabled when $-10mV \leq V_{OUT} \leq +10mV$.
16. V_{OUT} switches from -2V to +2V, or from +2V to -2V. Specification is from the 25% to 75% points.
17. $FPBW = \frac{Slew\ Rate}{2\pi V_{PEAK}}$; V_{PEAK} = 2V .
18. V_{IN} = 0V, Force V_{OUT} from 0V to ±2.5V, $t_R = t_F$ = 50ns.
19. V_{IN} = +2V, $\overline{Disable}$ = +5V to 0V. Measured from the 50% point of $\overline{Disable}$ to V_{OUT} = 0V.
20. V_{IN} = +2V, $\overline{Disable}$ = 0V to +5V. Measured from the 50% point of $\overline{Disable}$ to V_{OUT} = 2V.

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

Rev. 0 12/93