



# HIGH-SPEED 4K x 8 FourPort™ STATIC RAM

IDT7054S/L

## Features

- ◆ **High-speed access**
  - Commercial: 20/25/35ns (max.)
  - Industrial: 25ns (max.)
  - Military: 25/35ns (max.)
- ◆ **Low-power operation**
  - IDT7054S  
Active: 750mW (typ.)  
Standby: 7.5mW (typ.)
  - IDT7054L  
Active: 750mW (typ.)  
Standby: 1.5mW (typ.)
- ◆ **True FourPort memory cells which allow simultaneous access of the same memory locations**
- ◆ **Fully asynchronous operation from each of the four ports: P1, P2, P3, and P4**

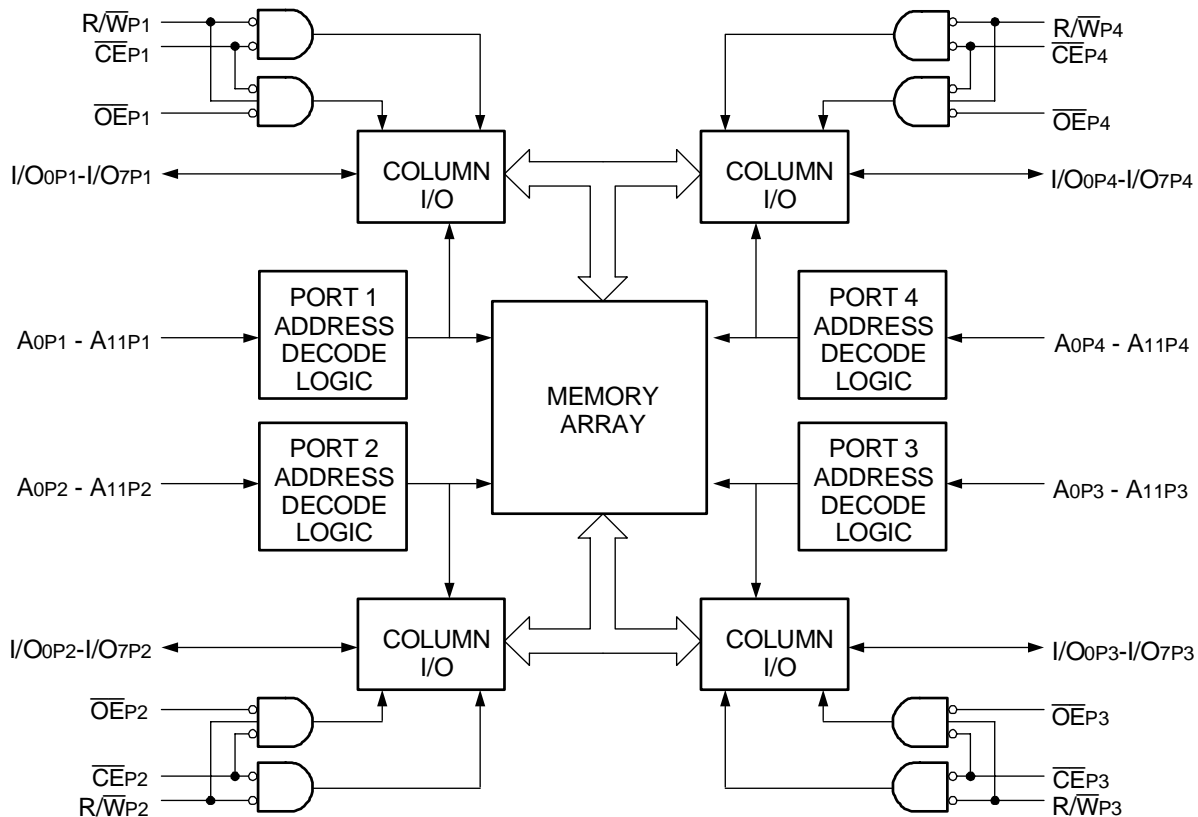
- ◆ **TTL-compatible; single 5V (±10%) power supply**
- ◆ **Available in 128 pin Thin Quad Flatpack and 108 pin PGA packages**
- ◆ **Industrial temperature range (-40°C to +85°C) is available for selected speeds**

## Description

The IDT7054 is a high-speed 4K x 8 FourPort™ Static RAM designed to be used in systems where multiple access into a common RAM is required. This FourPort Static RAM offers increased system performance in multiprocessor systems that have a need to communicate in real-time and also offers added benefit for high-speed systems in which multiple access is required in the same cycle.

The IDT7054 is also designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to

## Functional Block Diagram



3241 drw 01

JANUARY 2009

externally arbitrated or withstand contention when all ports simultaneously access the same FourPort RAM location.

The IDT7054 provides four independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from all ports. An automatic power down feature, controlled by  $\overline{CE}$ , permits the on-chip circuitry of each port to enter a very low power standby power mode.

Fabricated using IDT's CMOS high-performance technology, this FourPort SRAM typically operates on only 750mW of power. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 50µW from a 2V battery.

The IDT7054 is packaged in a ceramic 108-pin Pin Grid Array (PGA) and a 128-pin Thin Quad Flatpack (TQFP). The military grade product is manufactured in compliance with the latest revision of MIL-PRF-38535 QML, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

## Pin Configurations<sup>(1,2,3)</sup>

11/14/01

81	80	77	74	72	69	68	65	63	60	57	54	12									
R/W P2	A11 P2	A7 P2	A5 P2	A3 P2	A0 P2	A0 P3	A3 P3	A5 P3	A7 P3	A11 P3	R/W P3										
84	83	78	76	73	70	67	64	61	59	56	53	11									
NC	$\overline{OE}$ P2	A8 P2	A10 P2	A4 P2	A1 P2	A1 P3	A4 P3	A10 P3	A8 P3	$\overline{OE}$ P3	NC										
87	86	82	79	75	71	66	62	58	55	51	50	10									
A2 P1	A1 P1	$\overline{CE}$ P2	A9 P2	A6 P2	A2 P2	A2 P3	A6 P3	A9 P3	$\overline{CE}$ P3	A1 P4	A2 P4										
90	88	85	IDT7054G G108-1 <sup>(4)</sup>  108-Pin PGA Top View <sup>(5)</sup>						52	49	47	09									
A5 P1	A3 P1	A0 P1							48	46	45	08									
A10 P1	A6 P1	A4 P1							44	43	42	07									
A8 P1	A7 P1	Vcc							39	40	41	06									
A9 P1	A11 P1	$\overline{CE}$ P1							35	37	38	05									
R/W P1	$\overline{OE}$ P1	I/O0 P1							31	34	36	04									
NC	I/O1 P1	GND							104	105	1	4	8	12	17	21	25	28	32	33	03
I/O2 P1	I/O3 P1	I/O6 P1							Vcc	GND	Vcc	Vcc	GND	Vcc	I/O2 P4	I/O5 P4	I/O6 P4				
107	2	5	7	10	13	16	19	22	24	29	30	02									
I/O4 P1	I/O7 P1	I/O0 P2	I/O2 P2	I/O4 P2	I/O6 P2	I/O1 P3	I/O3 P3	I/O5 P3	I/O7 P3	I/O3 P4	I/O4 P4										
108	3	6	9	11	14	15	18	20	23	26	27	01									
I/O5 P1	NC	I/O1 P2	I/O3 P2	I/O5 P2	I/O7 P2	I/O0 P3	I/O2 P3	I/O4 P3	I/O6 P3	I/O0 P4	I/O1 P4										
	A	B	C	D	E	F	G	H	J	K	L	M									

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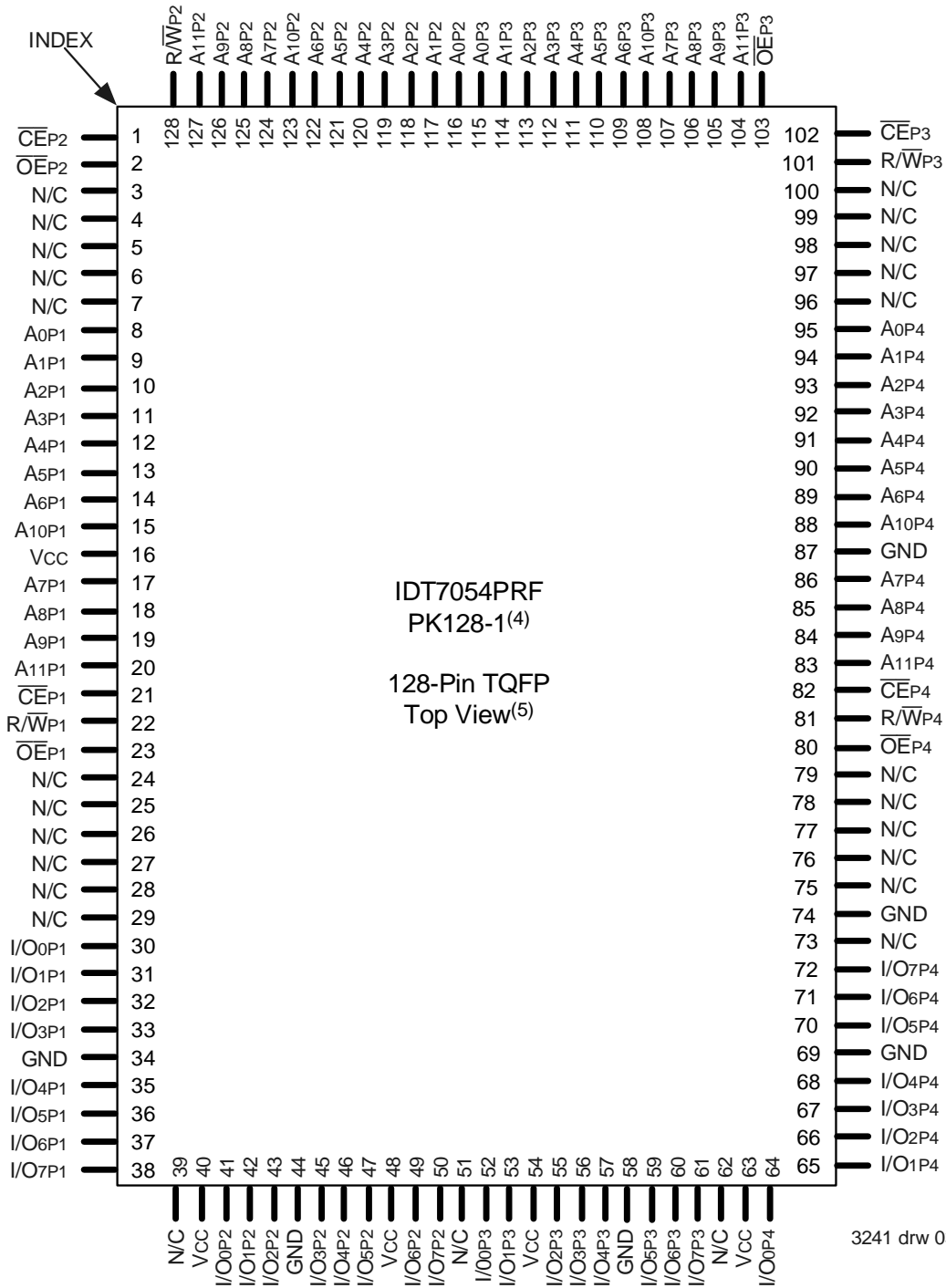
3241 drw 02

### NOTES:

1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. Package body is approximately 1.21 in x 1.21 in x .16 in.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Configurations<sup>(1,2,3)</sup> (con't.)

11/14/01



3241 drw 03

NOTES:

1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. Package body is approximately 14mm x 20mm x 1.4mm.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

## Pin Configurations<sup>(1,2)</sup>

## Capacitance<sup>(1)</sup>

(TA = +25°C, f = 1.0MHz) TQFP ONLY

Symbol	Parameter	Conditions <sup>(2)</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	9	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	10	pF

3241 tbl 03

### NOTES:

1. This parameter is determined by device characterization but is not production tested.
2. 3dV references the interpolated capacitance when the input and the output signals switch from 0V to 3V or from 3V to 0V.

## Maximum Operating Temperature and Supply Voltage<sup>(1)</sup>

Grade	Ambient Temperature	GND	V <sub>CC</sub>
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%

3241 tbl 04

### NOTES:

1. This is the parameter TA. This is the "instant on" case temperature.

### NOTES:

1. All V<sub>CC</sub> pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.

## Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	—	6.0 <sup>(2)</sup>	V
V <sub>IL</sub>	Input Low Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

3241 tbl 02

### NOTES:

1. V<sub>IL</sub> ≥ -1.5V for pulse width less than 10ns.
2. V<sub>TERM</sub> must not exceed V<sub>CC</sub> + 10%.

## Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Rating	Commercial & Industrial	Military	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T <sub>BAS</sub>	Temperature Under Bias	-55 to +125	-65 to +135	°C
T <sub>STG</sub>	Storage Temperature	-65 to +150	-65 to +150	°C
I <sub>OUT</sub>	DC Output Current	50	50	mA

3241 tbl 05

### NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V<sub>TERM</sub> must not exceed V<sub>CC</sub> + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of V<sub>TERM</sub> ≥ V<sub>CC</sub> + 10%.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range<sup>(1,5)</sup> ( $V_{CC} = 5.0V \pm 10\%$ )

Symbol	Parameter	Condition	Version	7054X20 Com'l Only		7054X25 Com'l, Ind & Military		7054X35 Com'l & Military		Unit	
				TYP. <sup>(2)</sup>	Max.	TYP. <sup>(2)</sup>	Max.	TYP. <sup>(2)</sup>	Max.		
ICC1	Operating Power Supply Current (All Ports Active)	$\overline{CE} = V_{IL}$ Outputs Disabled $f = 0^{(3)}$	COM'L.	S	150	300	150	300	150	300	mA
				L	150	250	150	250	150	250	
			MIL. & IND.	S	—	—	150	360	150	360	mA
				L	—	—	150	300	150	300	
ICC2	Dynamic Operating Current (All Ports Active)	$\overline{CE} = V_{IL}$ Outputs Disabled $f = f_{MAX}^{(4)}$	COM'L.	S	240	370	225	350	210	335	mA
				L	210	325	195	305	180	290	
			MIL. & IND.	S	—	—	225	400	210	395	mA
				L	—	—	195	340	180	330	
ISB	Standby Current (All Ports - TTL Level Inputs)	$\overline{CE} = V_{IH}$ $f = f_{MAX}^{(4)}$	COM'L.	S	70	95	60	85	40	75	mA
				L	60	80	50	70	35	60	
			MIL. & IND.	S	—	—	60	115	40	110	mA
				L	—	—	50	85	35	80	
ISB1	Full Standby Current (All Ports - All CMOS Level Inputs)	All Ports $\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V, f = 0^{(3)}$	COM'L.	S	1.5	15	1.5	15	1.5	15	mA
				L	0.3	1.5	0.3	1.5	0.3	1.5	
			MIL. & IND.	S	—	—	1.5	30	1.5	30	mA
				L	—	—	0.3	4.5	0.3	4.5	

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NOTES:

- 'X' in part number indicates power rating (S or L).
- $V_{CC} = 5V$ ,  $T_A = +25^\circ C$  and are not production tested.
- $f = 0$  means no address or control lines change.
- At  $f = f_{MAX}$ , address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of  $1/t_{rc}$ , and using "AC Test Conditions" of input levels of GND to 3V.
- For the case of one port, divide the appropriate current above by four.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ( $V_{CC} = 5.0V \pm 10\%$ )

Symbol	Parameter	Test Conditions	7054S		7054L		Unit
			Min.	Max.	Min.	Max.	
$ I_{L} $	Input Leakage Current <sup>(1)</sup>	$V_{CC} = 5.5V, V_{IN} = 0V$ to $V_{CC}$	—	10	—	5	$\mu A$
$ I_{LO} $	Output Leakage Current	$\overline{CE} = V_{IH}, V_{OUT} = 0V$ to $V_{CC}$	—	10	—	5	$\mu A$
$V_{OL}$	Output Low Voltage	$I_{OL} = 4mA$	—	0.4	—	0.4	V
$V_{OH}$	Output High Voltage	$I_{OH} = -4mA$	2.4	—	2.4	—	V

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NOTE:

- At  $V_{CC} \leq 2.0V$  input leakages are undefined.

### AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2

3241 tbl 08

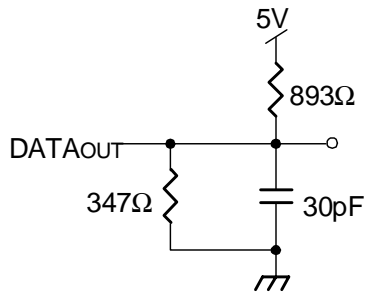
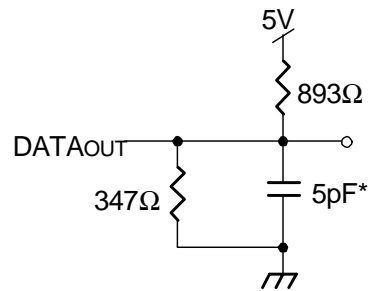


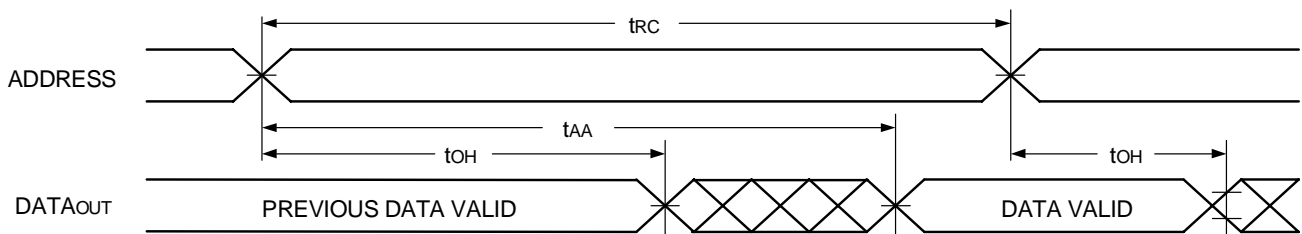
Figure 1. AC Output Test Load



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Figure 2. Output Test Load  
(for  $t_{LZ}$ ,  $t_{HZ}$ ,  $t_{WZ}$ ,  $t_{OW}$ )  
\*Including scope and jig

### Timing Waveform of Read Cycle No. 1, Any Port<sup>(1)</sup>



3241 drw 05

**NOTE:**

1.  $R/\bar{W} = V_{IH}$ ,  $\bar{OE} = V_{IL}$ , and  $\bar{CE} = V_{IL}$ .

### AC Electrical Characteristics Over the Operating Temperature and Supply Voltage<sup>(3)</sup>

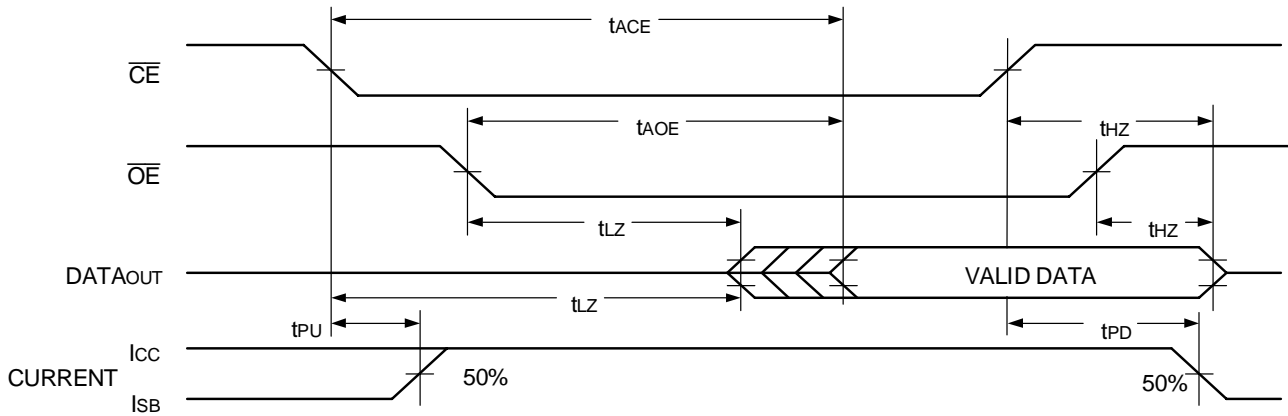
Symbol	Parameter	7054X20 Com'l Only		7054X25 Com'l, Ind & Military		7054X35 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>								
t <sub>RC</sub>	Read Cycle Time	20	—	25	—	35	—	ns
t <sub>AA</sub>	Address Access Time	—	20	—	25	—	35	ns
t <sub>ACE</sub>	Chip Enable Access Time	—	20	—	25	—	35	ns
t <sub>AOE</sub>	Output Enable Access Time	—	10	—	15	—	25	ns
t <sub>OH</sub>	Output Hold from Address Change	0	—	0	—	0	—	ns
t <sub>LZ</sub>	Output Low-Z Time <sup>(1,2)</sup>	5	—	5	—	5	—	ns
t <sub>HZ</sub>	Output High-Z Time <sup>(1,2)</sup>	—	12	—	15	—	15	ns
t <sub>PU</sub>	Chip Enable to Power Up Time <sup>(2)</sup>	0	—	0	—	0	—	ns
t <sub>PD</sub>	Chip Disable to Power Down Time <sup>(2)</sup>	—	20	—	25	—	35	ns

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**NOTES:**

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization but is not production tested.
3. 'X' in part number indicates power rating (S or L).

### Timing Waveform of Read Cycle No. 2, Any Port<sup>(1, 2)</sup>



3241 drw 06

**NOTES:**

1.  $R/\overline{W} = V_{IH}$  for Read Cycles.
2. Addresses valid prior to or coincident with  $\overline{CE}$  transition LOW.

## AC Electrical Characteristics Over the Operating Temperature and Supply Voltage<sup>(5)</sup>

Symbol	Parameter	7054X20 Com'l Only		7054X25 Com'l, Ind & Military		7054X35 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>WRITE CYCLE</b>								
t <sub>WC</sub>	Write Cycle Time	20	—	25	—	35	—	ns
t <sub>EW</sub>	Chip Enable to End-of-Write	15	—	20	—	30	—	ns
t <sub>AW</sub>	Address Valid to End-of-Write	15	—	20	—	30	—	ns
t <sub>AS</sub>	Address Set-up Time	0	—	0	—	0	—	ns
t <sub>WP</sub>	Write Pulse Width <sup>(3)</sup>	15	—	20	—	30	—	ns
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	0	—	ns
t <sub>DW</sub>	Data Valid to End-of-Write	15	—	15	—	20	—	ns
t <sub>HZ</sub>	Output High-Z Time <sup>(1,2)</sup>	—	15	—	15	—	15	ns
t <sub>DH</sub>	Data Hold Time	0	—	0	—	0	—	ns
t <sub>WZ</sub>	Write Enable to Output in High-Z <sup>(1,2)</sup>	—	12	—	15	—	15	ns
t <sub>OW</sub>	Output Active from End-of-Write <sup>(1,2)</sup>	0	—	0	—	0	—	ns
t <sub>WDD</sub>	Write Pulse to Data Delay <sup>(4)</sup>	—	35	—	45	—	55	ns
t <sub>DDD</sub>	Write Data Valid to Read Data Delay <sup>(4)</sup>	—	30	—	35	—	45	ns

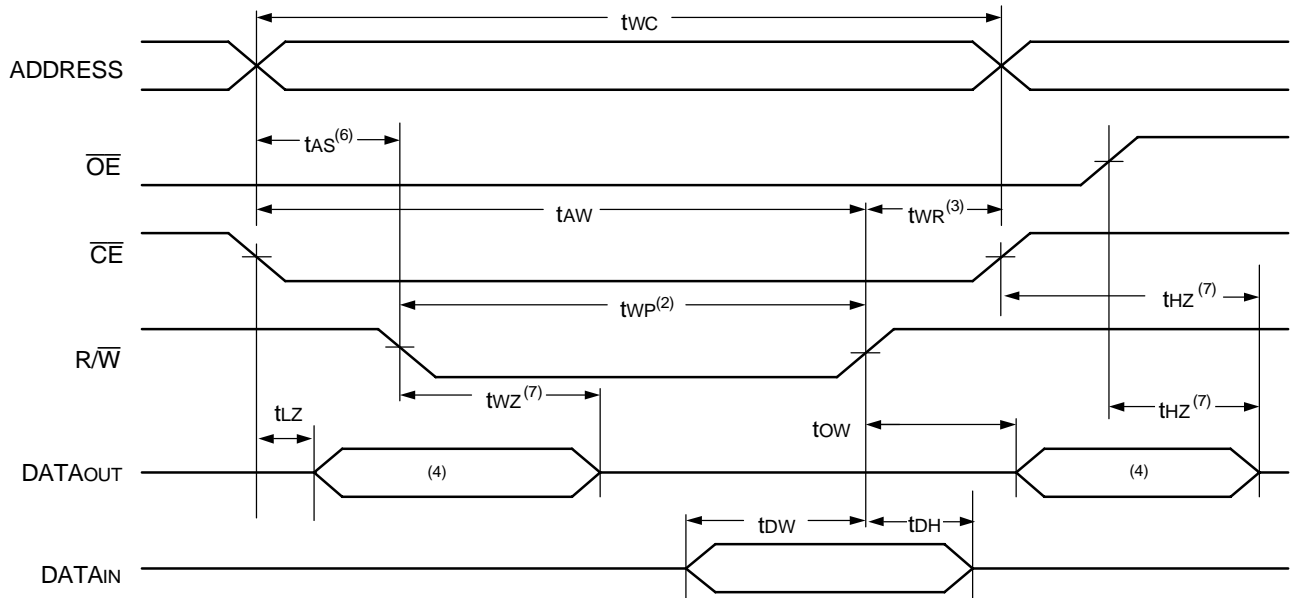
3241 tbl 10

**NOTES:**

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization but is not production tested.
3. If  $\overline{OE} = V_{IL}$  during a  $R/\overline{W}$  controlled write cycle, the write pulse width must be the larger of t<sub>WP</sub> or (t<sub>WZ</sub> + t<sub>DW</sub>) to allow the I/O drivers to turn off data to be placed on the bus for the required t<sub>OW</sub>. If  $\overline{OE} = V_{IH}$  during an  $R/\overline{W}$  controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t<sub>WP</sub>. Specified for  $\overline{OE} = V_{IH}$  (refer to "Timing Waveform of Write Cycle", Note 8).
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read".
5. 'X' in part number indicates power rating.

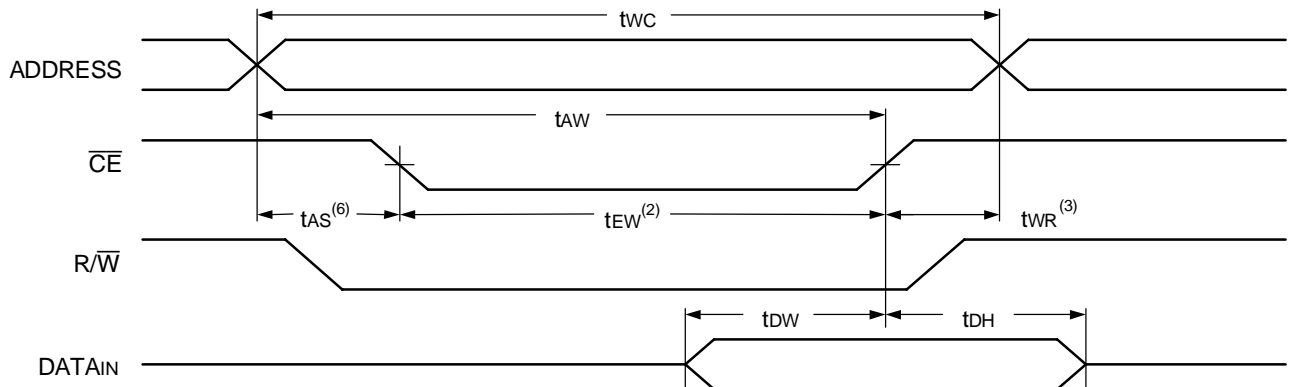


Timing Waveform of Write Cycle No. 1, R/W Controlled Timing<sup>(5,8)</sup>



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Timing Waveform of Write Cycle No. 2, CE Controlled Timing<sup>(1,5)</sup>

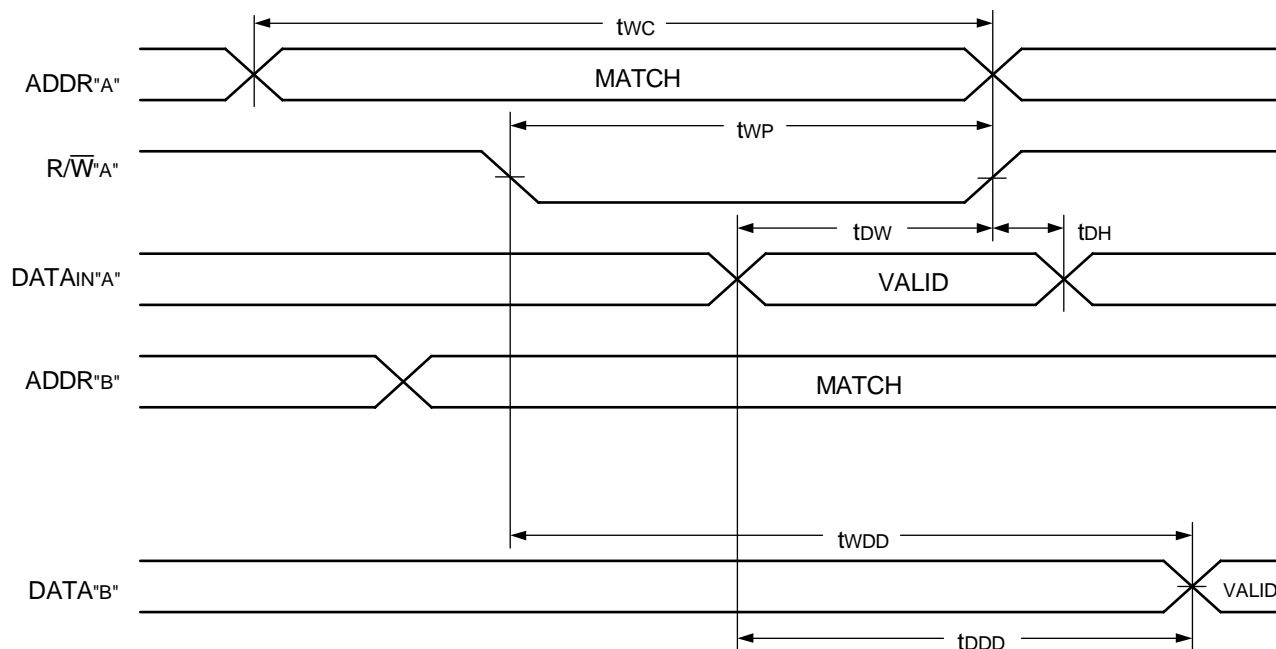


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NOTES:

1.  $R/\overline{W}$  or  $\overline{CE} = V_{IH}$  during all address transitions.
2. A write occurs during the overlap ( $t_{EW}$  or  $t_{WP}$ ) of a  $\overline{CE} = V_{IL}$  and a  $R/\overline{W} = V_{IL}$ .
3.  $t_{WR}$  is measured from the earlier of  $\overline{CE}$  or  $R/\overline{W} = V_{IH}$  to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the  $\overline{CE}$  LOW transition occurs simultaneously with or after the  $R/\overline{W} = V_{IL}$  transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal is asserted last,  $\overline{CE}$  or  $R/\overline{W}$ .
7. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed but is not production tested.
8. If  $\overline{OE} = V_{IL}$  during a  $R/\overline{W}$  controlled write cycle, the write pulse width must be the larger of  $t_{WP}$  or  $(t_{WZ} + t_{OW})$  to allow the I/O drivers to turn off data to be placed on the bus for the required  $t_{OW}$ . If  $\overline{OE} = V_{IH}$  during an  $R/\overline{W}$  controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified  $t_{WP}$ .

### Timing Waveform of Write with Port-to-Port Read<sup>(1, 2)</sup>



**NOTES:**

1.  $\overline{OE} = V_{IL}$  for the reading ports.
2. All timing is the same for left and right ports. Port "A" may be either of the four ports and Port "B" is any other port.

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### Functional Description

The IDT7054 provides four ports with separate control, address, and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by  $\overline{CE}$ . The  $\overline{CE}$  controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ( $\overline{CE} = V_{IH}$ ). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ( $\overline{OE}$ ). In the read mode, the port's  $\overline{OE}$  turns on the output drivers when set LOW. READ/WRITE conditions are illustrated in the table.

Table I – Read/Write Control

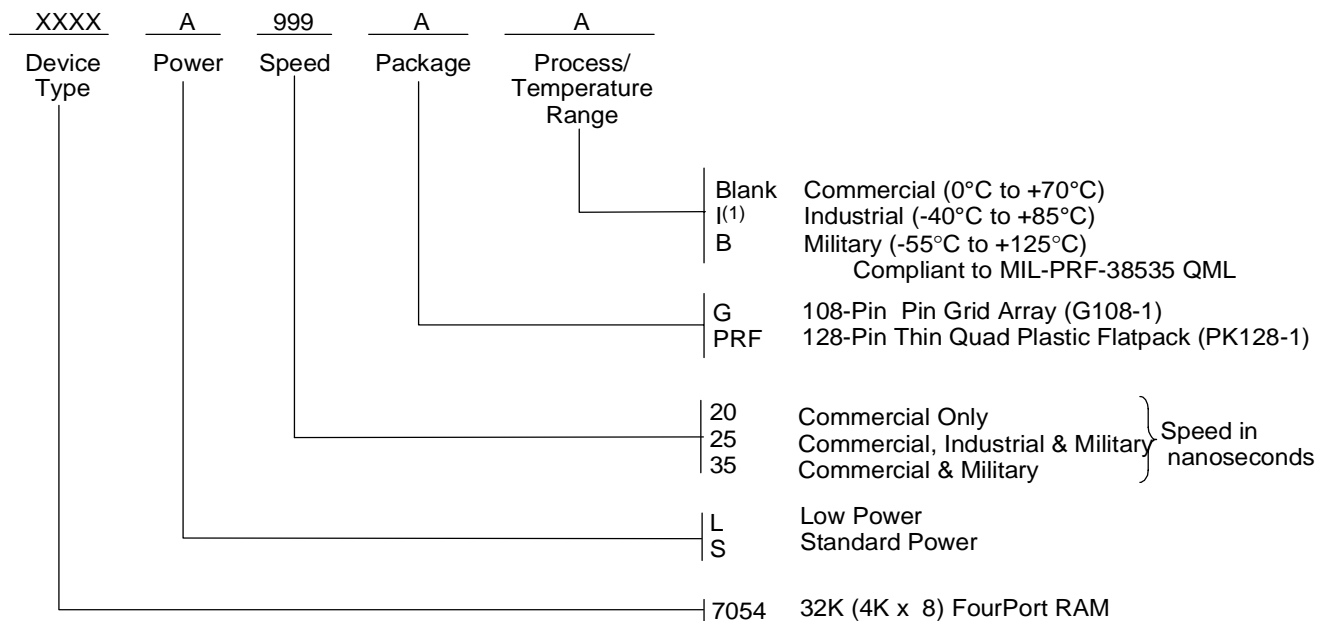
Any Port <sup>(1)</sup>				Function
R/W	$\overline{CE}$	$\overline{OE}$	Do-7	
X	H	X	Z	Port Deselected: Power-Down
X	H	X	Z	$\overline{CEP1} = \overline{CEP2} = \overline{CEP3} = \overline{CEP4} = V_{IH}$ Power Down Mode ISB or ISB1
L	L	X	DATAIN	Data on port written into memory <sup>(2)</sup>
H	L	L	DATAOUT	Data in memory output on port
X	X	H	Z	Outputs Disabled

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**NOTES:**

1. "H" =  $V_{IH}$ , "L" =  $V_{IL}$ , "X" = Don't Care, "Z" = High Impedance
2. For valid write operation, no more than one port can write to the same address location at the same time.

## Ordering Information



**NOTE:**

- Industrial temperature range is available.  
For other speeds, packages and powers contact your sales office.

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## Datasheet Document History

- 1/18/99: Initiated datasheet document history  
Converted to new format  
Cosmetic typographical corrections  
Added additional notes to pin configurations
- 6/4/99: Changed drawing format  
Page 1 Corrected DSC number
- 9/1/99: Removed Preliminary
- 11/10/99: Replaced IDT logo
- 5/23/00: Page 4 Increased storage temperature parameter  
Clarified TA parameter  
Page 5 DC Electrical parameters—changed wording from "open" to "disabled"  
Changed ±200mV to 0mV in notes
- 10/22/01: Page 2 & 3 Added date revision for pin configurations  
Page 5, 7 & 8 Added Industrial temp to column heading for 25ns speed to DC & AC Electrical Characteristics  
Page 11 Added Industrial temp offering to 25ns ordering information  
Page 4, 5, 7 & 8 Removed Industrial temp footnote from all tables  
Page 6 Changed 5ns to 3ns in AC Test Conditions table  
Page 1 & 11 Replace ™ logo with ® logo
- 01/29/09: Page 11 Removed "IDT" from orderable part number



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San Jose, CA 95138

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800-345-7015 or 408-284-8200  
fax: 408-284-2775  
www.idt.com

**for Tech Support:**  
408-284-2794  
DualPortHelp@idt.com

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