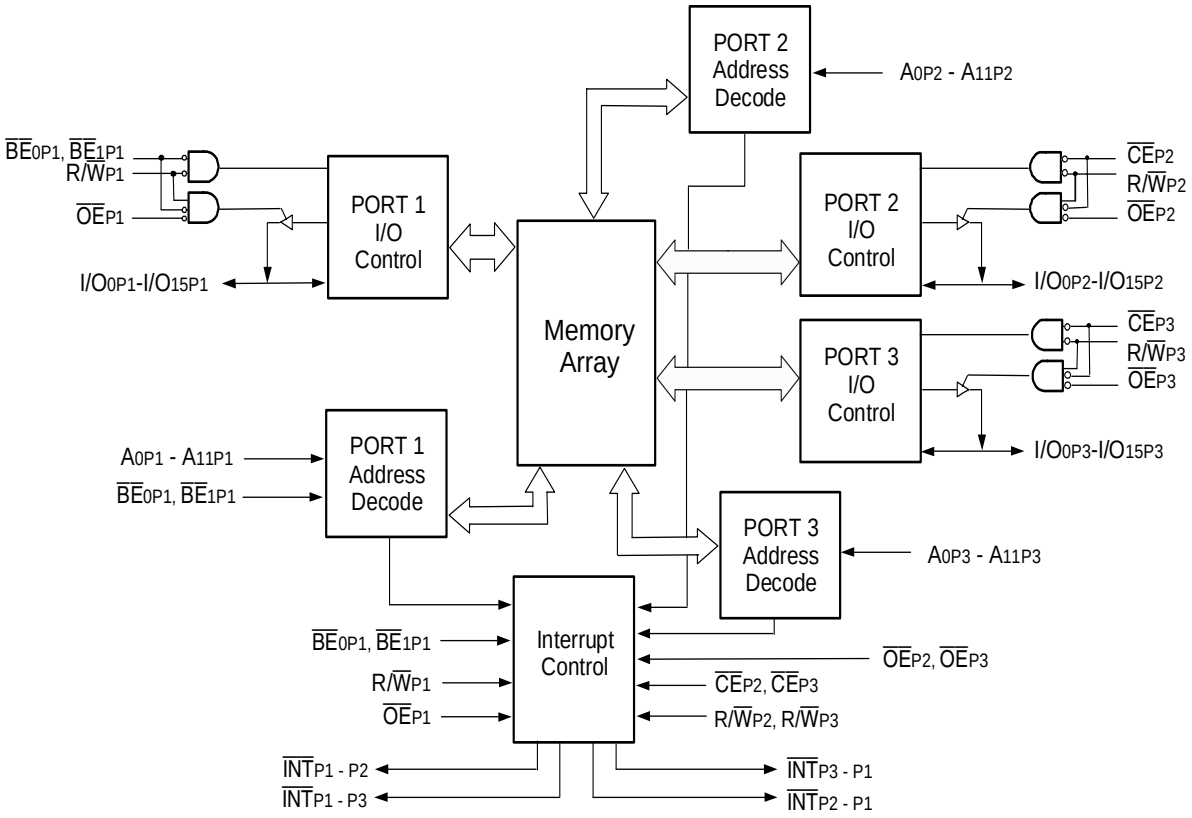
# HIGH-SPEED 8K x 16 TriPort STATIC RAM

**IDT70P5258ML**
**IDT70P525ML**
**IDT70V525ML**

## Features

- **High-speed access**
  - *Industrial: 55ns (max.)*
- **Low-power operation**
  - *IDT70P5258ML and IDT70P525ML*
    *Active: 54mW (typ.)*
    *Standby: 7.2µW (typ.)*
  - *IDT70V525ML*
    *Active: 450mW (typ.)*
    *Standby: 250µW (typ.)*
- **TriPort architecture allows simultaneous access to the memory from all three ports**
- **Fully asynchronous operation from each of the three ports: P1, P2, and P3**
- **IDT70P5258 supports 3.0V and 1.8V I/O's**
- **Available in 144-ball 0.5mm-pitch *fp*BGA**
- **Industrial temperature range (–40°C to +85°C)**
- **Greeen parts available, see ordering information**

## Functional Block Diagram




5681 drw 01

JANUARY 2009

## Description

The IDT70X525X is a high-speed 8K x 16 TriPort Static RAM designed to be used in systems where multiple access into a common RAM is required. This TriPort Static RAM offers increased system performance in multiprocessor systems that have a need to communicate in real time and also offers added benefit for high-speed systems in which multiple access is required in the same cycle.

The IDT70X525X is also designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to externally arbitrated or withstand contention when more than one port simultaneously accesses the same TriPort RAM location.

The IDT70X525X provides three independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from mutiple ports. An automatic power down feature, controlled by $\overline{BE}_0$ and $\overline{BE}_1$ on Port 1 and $\overline{CE}$ on Port 2 and on Port 3, permits the on-chip circuitry of each port to enter a very low power standby power mode.

The IDT70X525X is packaged in a 144-ball 0.5mm-pitch *fp*BGA.

## Pin Configurations[1,2,3]

70(P/V)525XBZ
BZ-144

Top View

12/19/03

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A1 $I/O_{7P3}$ | A2 $I/O_{6P2}$ | A3 $I/O_{4P3}$ | A4 $I/O_{3P2}$ | A5 $I/O_{1P2}$ | A6 $\overline{OE}_{P3}$ | A7 $R/\overline{W}_{P2}$ | A8 NC | A9 $A_{11P2}$ | A10 $A_{9P2}$ | A11 $A_{7P2}$ | A12 $A_{6P2}$ |
| B1 $I/O_{7P2}$ | B2 $I/O_{6P3}$ | B3 $V_{DD}$(1) | B4 $I/O_{2P3}$ | B5 $I/O_{0P3}$ | B6 $\overline{OE}_{P2}$ | B7 $\overline{CE}_{P3}$ | B8 NC | B9 $A_{10P3}$ | B10 $A_{8P3}$ | B11 $A_{6P3}$ | B12 $A_{5P3}$ |
| C1 $I/O_{9P2}$ | C2 $V_{SS}$ | C3 $I/O_{5P2}$ | C4 $I/O_{2P2}$ | C5 $I/O_{0P2}$ | C6 $R/\overline{W}_{P3}$ | C7 $\overline{CE}_{P2}$ | C8 $A_{11P3}$ | C9 $A_{10P2}$ | C10 $A_{8P2}$ | C11 $A_{5P2}$ | C12 $A_{4P3}$ |
| D1 $I/O_{10P3}$ | D2 $I/O_{8P2}$ | D3 $I/O_{5P3}$ | D4 $I/O_{3P3}$ | D5 $I/O_{1P3}$ | D6 $V_{DD}$ | D7 $V_{DD}$(1) | D8 $V_{SS}$ | D9 $A_{9P3}$ | D10 $A_{7P3}$ | D11 $A_{4P2}$ | D12 $A_{3P2}$ |
| E1 $I/O_{11P3}$ | E2 $I/O_{11P2}$ | E3 $I/O_{8P3}$ | E4 $I/O_{4P2}$ | E5 $V_{DD}$ | E6 $V_{SS}$ | E7 $V_{SS}$ | E8 $V_{SS}$ | E9 $A_{0P3}$ | E10 $A_{3P3}$ | E11 $A_{2P3}$ | E12 $A_{2P2}$ |
| F1 $I/O_{12P3}$ | F2 $I/O_{12P2}$ | F3 $I/O_{9P3}$ | F4 $V_{DD}$(1) | F5 $V_{DD}$(1) | F6 $V_{SS}$ | F7 $V_{SS}$ | F8 $V_{SS}$ | F9 $V_{SS}$ | F10 $V_{DD}$ | F11 $A_{1P3}$ | F12 $A_{0P2}$ |
| G1 $I/O_{15P2}$ | G2 $I/O_{13P3}$ | G3 $I/O_{10P2}$ | G4 $I/O_{13P2}$ | G5 $V_{SS}$ | G6 $V_{SS}$ | G7 $V_{SS}$ | G8 $V_{SS}$ | G9 $V_{SS}$ | G10 $V_{DD}$ | G11 $A_{1P2}$ | G12 $V_{DD}$(1) |
| H1 $I/O_{15P3}$ | H2 $I/O_{14P3}$ | H3 $I/O_{14P2}$ | H4 $V_{DD}$ | H5 $V_{SS}$ | H6 $V_{SS}$ | H7 $V_{SS}$ | H8 $V_{SS}$ | H9 $V_{DD}$ | H10 $V_{DD}$ | H11 $\overline{INT}_{P3P1}$ | H12 $\overline{INT}_{P2P1}$ |
| J1 $I/O_{2P1}$ | J2 $I/O_{1P1}$ | J3 $V_{DD}$ | J4 $V_{SS}$ | J5 $V_{SS}$ | J6 $V_{SS}$ | J7 $V_{SS}$ | J8 $V_{DD}$ | J9 $V_{DD}$ | J10 $A_{0P1}$ | J11 $\overline{INT}_{P1P3}$ | J12 $\overline{INT}_{P1P2}$ |
| K1 $I/O_{3P1}$ | K2 $I/O_{0P1}$ | K3 $I/O_{4P1}$ | K4 $V_{SS}$ | K5 $V_{DD}$ | K6 $V_{SS}$ | K7 $V_{DD}$ | K8 $V_{DD}$ | K9 $A_{10P1}$ | K10 $A_{3P1}$ | K11 $A_{2P1}$ | K12 $A_{1P1}$ |
| L1 $I/O_{6P1}$ | L2 $I/O_{5P1}$ | L3 $I/O_{8P1}$ | L4 $I/O_{10P1}$ | L5 $I/O_{12P1}$ | L6 $I/O_{14P1}$ | L7 $\overline{OE}_{P1}$ | L8 $\overline{BE}_{0P1}$ | L9 NC | L10 $A_{9P1}$ | L11 $A_{7P1}$ | L12 $A_{4P1}$ |
| M1 $I/O_{7P1}$ | M2 $V_{DD}$ | M3 $I/O_{9P1}$ | M4 $I/O_{11P1}$ | M5 $I/O_{13P1}$ | M6 $I/O_{15P1}$ | M7 $R/\overline{W}_{P1}$ | M8 $\overline{BE}_{1P1}$ | M9 $A_{11P1}$ | M10 $A_{8P1}$ | M11 $A_{6P1}$ | M12 $A_{5P1}$ |

5681 drw 02

**NOTES:**
1. $V_{DDQ}$ for 70P5258.

## Pin Configurations[1,2]

| Symbol | Pin Name |
|---|---|
| $A_{0P1}$ - $A_{11P1}$ | Address Lines - Port 1 (Input) |
| $A_{0P2}$ - $A_{11P2}$ | Address Lines - Port 2 (Input) |
| $A_{0P3}$ - $A_{11P3}$ | Address Lines - Port 3 (Input) |
| $I/O_{0P1}$ - $I/O_{15P1}$ | Data I/O - Port 1 |
| $I/O_{0P2}$ - $I/O_{15P2}$ | Data I/O - Port 2 |
| $I/O_{0P3}$ - $I/O_{15P3}$ | Data I/O - Port 3 |
| $R/\overline{W}_{P1}$ | Read/Write - Port 1 (Input) |
| $R/\overline{W}_{P2}$ | Read/Write - Port 2 (Input) |
| $R/\overline{W}_{P3}$ | Read/Write - Port 3 (Input) |
| $\overline{CE}_{P2}$ | Chip Enable - Port 2 (Input) |
| $\overline{CE}_{P3}$ | Chip Enable - Port 3 (Input) |
| $\overline{OE}_{P1}$ | Output Enable - Port 1 (Input) |
| $\overline{OE}_{P2}$ | Output Enable - Port 2 (Input) |
| $\overline{OE}_{P3}$ | Output Enable - Port 3 (Input) |
| $\overline{BE}_{0P1}$ | Bank Enable 0 - Port 1 (Input) |
| $\overline{BE}_{1P1}$ | Bank Enable 1 - Port 1 (Input) |
| $\overline{INT}_{P1 - P2}$ | Interrupt $_{P1 - P2}$ - Port 1 (Output) |
| $\overline{INT}_{P1 - P3}$ | Interrupt $_{P1 - P3}$ - Port 1 (Output) |
| $\overline{INT}_{P2 - P1}$ | Interrupt $_{P2 - P1}$ - Port 2 (Output) |
| $\overline{INT}_{P3 - P1}$ | Interrupt $_{P3 - P1}$ - Port 3 (Output) |
| $V_{DD}$ | Power (Input) |
| $V_{DDQ}$ | Port Power Supply (Input)[3,4] |
| $V_{SS}$ | Ground (Input) |

5681 tbl 01

**NOTES:**
1. All $V_{DD}$ pins must be connected to the power supply.
2. All $V_{SS}$ pins must be connected to the ground supply.
3. IDT70P5258 only.
4. For Port 2 and Port 3.

## Capacitance[1]

($T_A$ = +25°C, f = 1.0MHz)

| Symbol | Parameter | Port | Conditions[2] | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | Port 1 | $V_{IN}$ = 3dV | 18 | pF |
| | | Port 2 & 3 | $V_{IN}$ = 3dV | 9 | pF |
| $C_{OUT}$ | Output Capacitance | Port 1 | $V_{OUT}$ = 3dV | 20 | pF |
| | | Port 2 & 3 | $V_{OUT}$ = 3dV | 11 | pF |

5681 tbl 03

**NOTES:**
1. This parameter is determined by device characterization but is not production tested.
2. 3dV references the interpolated capacitance when the input and the output signals switch from 0V to 3V or from 3V to 0V.

## Maximum Operating Temperature and Supply Voltage[1]

| Grade | Ambient Temperature | Device | $V_{SS}$ | $V_{DD}$ |
|---|---|---|---|---|
| Industrial | -40°C to +85°C | 70P525<br>70P5258 | 0V | 1.8V ± 100mV |
| | | 70V525 | 0V | 3.0V ± 300mV |

5681 tbl 04

**NOTE:**
1. This is the parameter $T_A$. This is the "instant on" case temperature.

## Absolute Maximum Ratings(1)

| Symbol | Rating | Industrial | Unit |
|---|---|---|---|
| $V_{TERM}$ | Supply Voltage on $V_{DD}$ with Respect to GND | -0.5 to +2.9 | V |
| $V_{TERM}$ | Supply Voltage on $V_{DDQ}$ with Respect to GND | -0.5 to +3.6 | V |
| $V_{TERM}$(2) | Terminal Voltage with Respect to GND | -0.5 to $V_{DD}$ + 0.3(4) | V |
| $T_{BIAS}$(3) | Temperature Under Bias | -55 to +125 | °C |
| $T_{STG}$ | Storage Temperature | -65 to +150 | °C |
| $T_{JN}$ | Junction Temperatue | +150 | °C |
| $I_{OUT}$ (for 70V525) | DC Output Current | 50 | mA |
| $I_{OUT}$ (for 70P525 and 70P5258) | DC Output Current | 20 | mA |

5681 tbl 05

**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. $V_{TERM}$ must not exceed $V_{DD}$ + 10% for Port 1 or $V_{DDQ}$ + 10% for Port 2 and Port 3 for more than 25% of the cycle time or 10ns maximum, and is limited to $\leq$ 20mA for the period of $V_{TERM} \geq V_{DD}$ + 10% (Port 1) or $V_{DDQ}$ + 10% (Port 2 and Port 3).
3. Ambient Temperature under DC Bias. No AC Conditions. Chip Deselected.
4. $V_{DDQ}$ + 0.3V for 70P5258.

## Recommended DC Operating Conditions

| Symbol | Device | Port | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DD}$ | 70P5258 | All | Supply Voltage | 1.7 | 1.8 | 1.9 | V |
| | 70P525 | | | 1.7 | 1.8 | 1.9 | |
| | 70V525 | | | 2.7 | 3 | 3.3 | |
| $V_{DDQ}$ | 70P5258 | Port 2 & 3 | I/O Supply Voltage(1) | 2.7 | 3 | 3.3 | V |
| | 70P525 | N/A | | — | — | — | |
| | 70V525 | N/A | | — | — | — | |
| $V_{SS}$ | All | All | Ground | 0 | 0 | 0 | V |
| $V_{IH}$ | 70P5258 | Port 1 | Input High Voltage | 1.2 | — | $V_{DD}$+0.2 | V |
| | | Port 2 & 3 | | 2 | — | $V_{DDQ}$+0.2 | |
| | 70P525 | All | | 1.2 | — | $V_{DD}$+0.2 | |
| | 70V525 | All | | 2 | — | $V_{DD}$+0.2 | |
| $V_{IL}$ | 70P5258 | Port 1 | Input Low Voltage | -0.2 | — | 0.4 | V |
| | | Port 2 & 3 | | -0.2 | — | 0.6 | |
| | 70P525 | All | | -0.2 | — | 0.4 | |
| | 70V525 | All | | -0.2 | — | 0.6 | |

5681 tbl 02

**NOTES:**
1. The supply voltage for all ports on the IDT70P525 and IDT70V525 is supplied by $V_{DD}$ so there are no $V_{DDQ}$ pins on these devices.
2. $V_{IL} \geq$ -1.5V for pulse width less than 10ns.
3. $V_{TERM}$ must not exceed $V_{DD}$ + 10% for Port 1 or $V_{DDQ}$ + 10% for Port 2 and Port 3.

## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(1,4)

| Symbol | Parameter | Test Condition | Version | 70P5258 70P525 Ind'l Only | | 70V525 Ind'l Only | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Typ.(1) | Max. | Typ.(1) | Max. | |
| $I_{DD}$ | Dynamic Operating Current (Both Ports Active - CMOS Level Inputs) | $\overline{CE}$ = $V_{IL}$, Outputs Open<br>f = $f_{MAX}$(2) | IND'L L | 30 | 50 | 150 | 180 | mA |
| $I_{SB1}$ | Standby Current (Both Ports - CMOS Level Inputs) | $\overline{CE}_R$ and $\overline{CE}_L$ = $V_{IH}$<br>f = $f_{MAX}$(2) | IND'L L | .004 | .016 | 5 | 10 | mA |
| $I_{SB2}$ | Standby Current (One Port - CMOS Level Inputs) | $\overline{CE}_{"A"}$ = $V_{IL}$ and $\overline{CE}_{"B"}$ = $V_{IH}$(3), Active Port Outputs Open<br>f = $f_{MAX}$(2) | IND'L L | 17 | 28 | 90 | 110 | mA |
| $I_{SB3}$ | Full Standby Current (Both Ports - CMOS Level Inputs) | Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{DDQ}$ - 0.2V,<br>$V_{IN} \geq V_{DDQ}$ - 0.2V or $V_{IN} \leq$ 0.2V<br>f = $f_{MAX}$(2) | IND'L L | 4 | 16 | 84 | 150 | µA |
| $I_{SB4}$ | Standby Current (One Port - CMOS Level Inputs) | $\overline{CE}_{"A"} \leq$ 0.2V and $\overline{CE}_{"B"} \geq V_{DDQ}$ - 0.2V(3)<br>$V_{IN} \geq V_{DDQ}$ - 0.2V or $V_{IN} \leq$ 0.2V, Active Port Outputs Open<br>f = $f_{MAX}$(2) | IND'L L | 17 | 28 | 90 | 110 | mA |

5681 tbl 06

**NOTES:**
1. $V_{DD}$ = 1.8V for 70P5258 and 70P525. $V_{DD}$ = 3.0V for 70V525, $T_A$ = +25°C, and are not production tested. $I_{DD\,DC}$ = 15mA (typ.)
2. At f = $f_{MAX}$, address and control lines are cycling at the maximum frequency read cycle of 1/$t_{RC}$, and using "AC Test Conditions".
3. For the 70P5258, if Port "A" is Port 1 then Port "B" may be either Port 2 or Port 3. If Port "A" is either Port 2 or Port 3, Port "B" must be Port 1.
4. $V_{DD}$ = 1.8V ± 100mV for 70P525 and 70P5258. $V_{DD}$ = 3.0V ± 300mV for 70V525.

## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(2)

| Symbol | Device | Port | Parameter | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{LI}$ | 70P5258 | All | Input Leakage Current | $V_{DD}$ = 1.8V, $V_{IN}$ = 0V to $V_{DD}$ | — | 1 | µA |
| | 70P525 | All | | $V_{DD}$ = 1.8V, $V_{IN}$ = 0V to $V_{DD}$ | — | 1 | |
| | 70V525 | All | | $V_{DD}$ = 3.0V, $V_{IN}$ = 0V to $V_{DD}$ | — | 1 | |
| $I_{LO}$ | 70P5258 | All | Output Leakage Current | $\overline{CE}x$ = $\overline{BE}x$ = $V_{IH}$, $V_{OUT}$ = 0V to $V_{DD}$ | — | 1 | µA |
| | 70P525 | All | | $\overline{CE}x$ = $\overline{BE}x$ = $V_{IH}$, $V_{OUT}$ = 0V to $V_{DD}$ | — | 1 | |
| | 70V525 | All | | $\overline{CE}x$ = $\overline{BE}x$ = $V_{IH}$, $V_{OUT}$ = 0V to $V_{DD}$ | — | 1 | |
| $V_{OL}$ | 70P5258 | Port 1 | Output Low Voltage | $I_{OL}$ = +0.1mA | — | 0.2 | V |
| | | Port 2 & 3 | | $I_{OL}$ = +2mA | — | 0.4 | |
| | 70P525 | All | | $I_{OL}$ = +0.1mA | — | 0.2 | |
| | 70V525 | All | | $I_{OL}$ = +2mA | — | 0.4 | |
| $V_{OH}$ | 70P5258 | Port 1 | Output High Voltage | $I_{OH}$ = -0.1mA | 1.4 | — | V |
| | | Port 2 & 3 | | $I_{OH}$ = -2mA | 2.1 | — | |
| | 70P525 | All | | $I_{OH}$ = -0.1mA | 1.4 | — | |
| | 70V525 | All | | $I_{OH}$ = -2mA | 2.1 | — | |

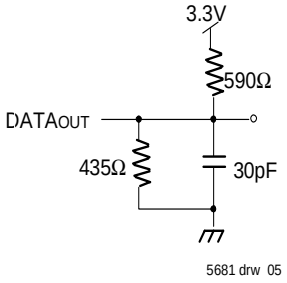
5681 tbl 07

**NOTE:**
1. At $V_{DD} \leq$ 2.0V input leakages are undefined.
2. $V_{DD}$ = 1.8V ± 100mV for 70P525 and 70P5258. $V_{DD}$ = 3.0V ± 300mV for 70V525.

## AC Test Conditions

| | |
|---|---|
| Input Pulse Levels | GND to 3.0V/GND to 1.8V |
| Input Rise/Fall Times | 3ns Max. |
| Input Timing Reference Levels | 1.5V/0.9V |
| Output Reference Levels | 1.5V/0.9V |
| Output Load | Figures 1, 2 and 3 |

5681 tbl 08

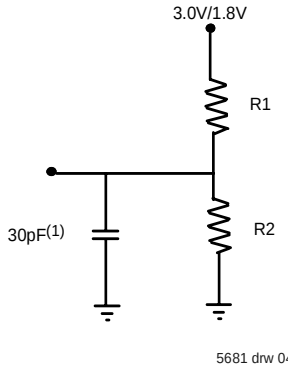



5681 drw 05

**Figure 2. AC Output Test Load for the 70V525**

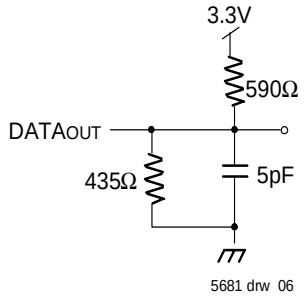
| | 3.0V | 1.8V |
|---|---|---|
| R1 | 1022Ω | 13500Ω |
| R2 | 729Ω | 10800Ω |

5681 tbl 09




5681 drw 04

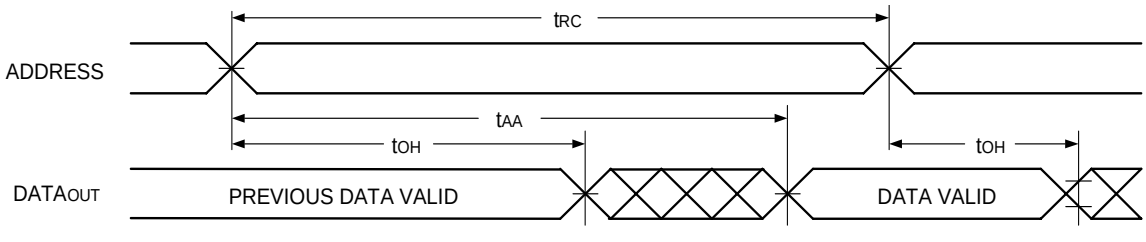
**Figure 1. AC Output Test Load for the 70P525 and 70P5258**




5681 drw 06

**Figure3. AC Output Test Load for the 70V525 (for $t_{HZ}$, $t_{LX}$, $t_{WZ}$, $t_{OW}$)**

## Timing Waveform of Read Cycle No. 1, Any Port(1)

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**NOTE:**
1. $R/\overline{W}$ = $V_{IH}$ and $\overline{CE}$ (or $\overline{BE}_X$) = $V_{IL}$.

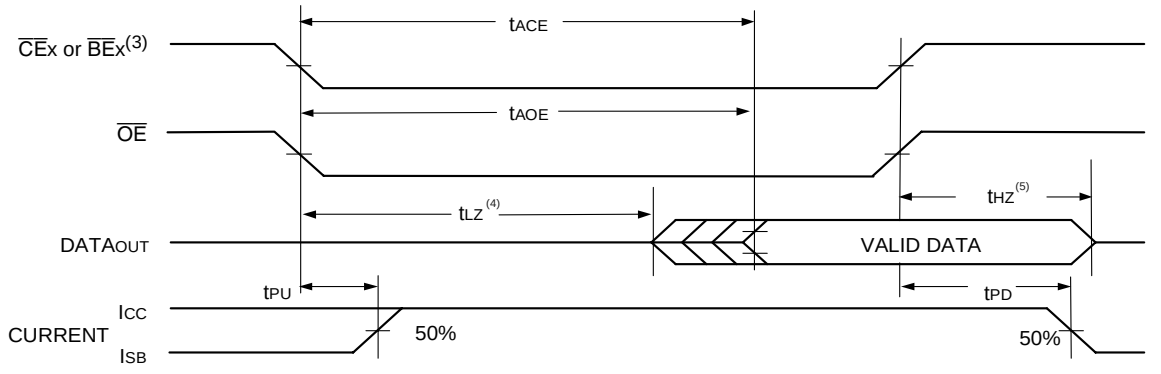
## AC Electrical Characteristics Over the Operating Temperature and Supply Voltage

| Symbol | Parameter | 70X525X Ind'l Only | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| **READ CYCLE** | | | | |
| $t_{RC}$ | Read Cycle Time | 55 | — | ns |
| $t_{AA}$ | Address Access Time | — | 55 | ns |
| $t_{ACE}$ | Chip Enable Access Time | — | 55 | ns |
| $t_{AOE}$ | Output Enable Access Time | — | 30 | ns |
| $t_{OH}$ | Output Hold from Address Change | 5 | — | ns |
| $t_{LZ}$ | Output Low-Z Time(1,2) | 5 | — | ns |
| $t_{HZ}$ | Output High-Z Time(1,2) | — | 25 | ns |
| $t_{PU}$ | Chip Enable to Power Up Time(2) | 0 | — | ns |
| $t_{PD}$ | Chip Disable to Power Down Time(2) | — | 55 | ns |

5681 tbl0

**NOTES:**
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization but is not production tested.

## Timing Waveform of Read Cycle No. 2, Any Port(1, 2)

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**NOTES:**
1. R/$\overline{W}$ = $V_{IH}$ for Read Cycles.
2. Addresses valid prior to or coincident with $\overline{CE}$ (or $\overline{BE}$x) transition LOW.
3. $\overline{CE}$ for Port 2 or Port 3, $\overline{BE}$x for Port 1.
4. Timing depends on which signal is asserted last, $\overline{CE}$ (or $\overline{BE}$x) or $\overline{OE}$.
5. Timing depends on which signal is deasserted first, $\overline{CE}$ (or $\overline{BE}$x) or $\overline{OE}$.

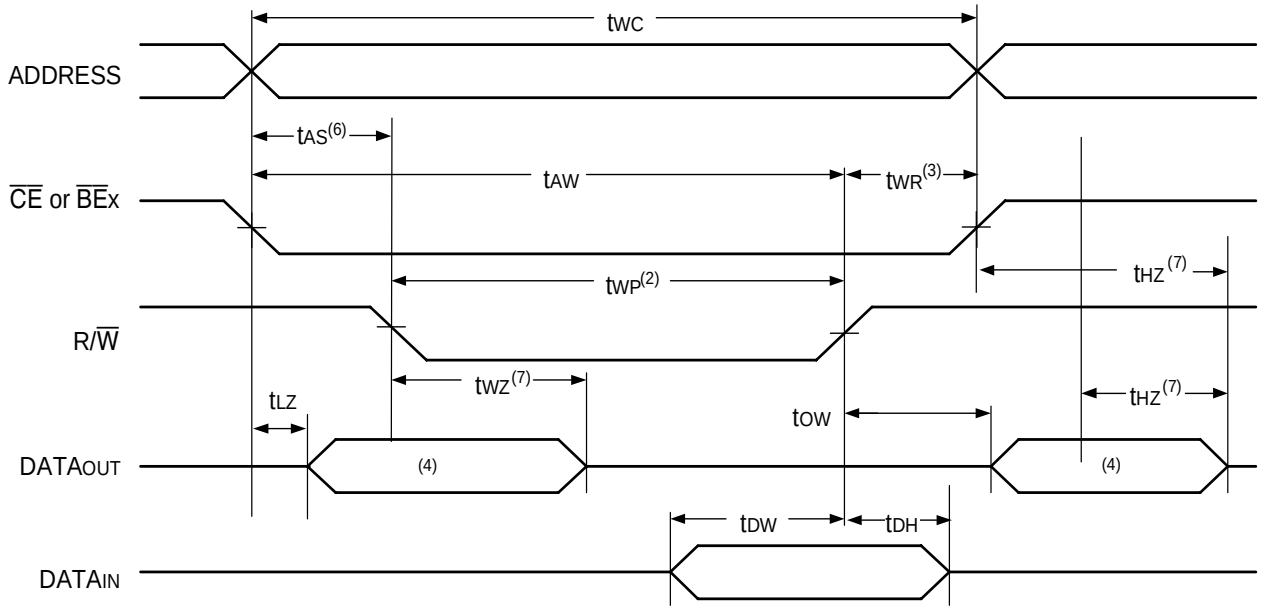
## AC Electrical Characteristics Over the Operating Temperature and Supply Voltage

| Symbol | Parameter | 70X525X Ind'l Only | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| **WRITE CYCLE** | | | | |
| $t_{WC}$ | Write Cycle Time | 55 | — | ns |
| $t_{EW}$ | Chip Enable to End-of-Write | 45 | — | ns |
| $t_{AW}$ | Address Valid to End-of-Write | 45 | — | ns |
| $t_{AS}$ | Address Set-up Time | 0 | — | ns |
| $t_{WP}$ | Write Pulse Width[3] | 40 | — | ns |
| $t_{WR}$ | Write Recovery Time | 0 | — | ns |
| $t_{DW}$ | Data Valid to End-of-Write | 30 | — | ns |
| $t_{HZ}$ | Output High-Z Time[1,2] | — | 25 | ns |
| $t_{DH}$ | Data Hold Time | 0 | — | ns |
| $t_{WZ}$ | Write Enable to Output in High-Z[1,2] | — | 25 | ns |
| $t_{OW}$ | Output Active from End-of-Write[1,2] | 0 | — | ns |

5681 tbl 11

**NOTES:**
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization but is not production tested.

## Timing Waveform of Write Cycle No. 1, R/$\overline{W}$ Controlled Timing(5)

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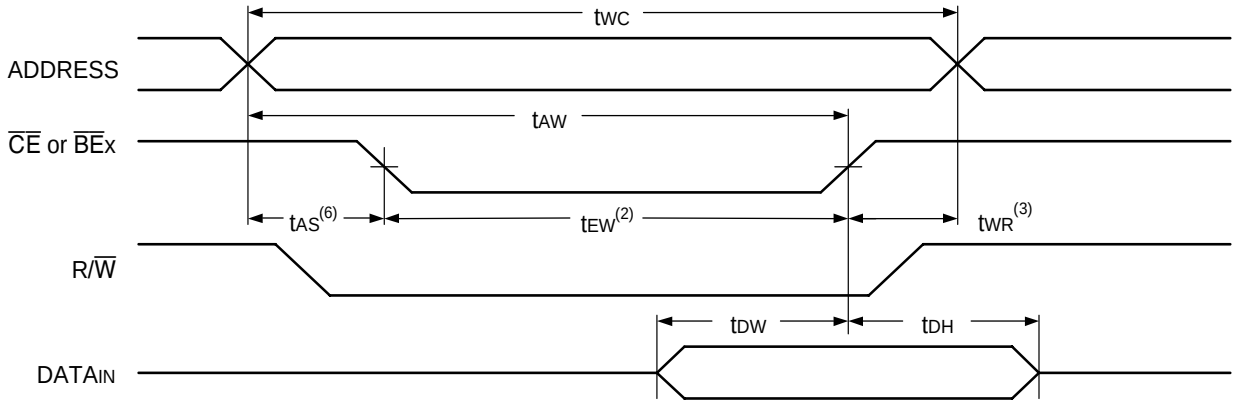
## Timing Waveform of Write Cycle No. 2, $\overline{CE}$ Controlled Timing(1,5)




5681 drw 10

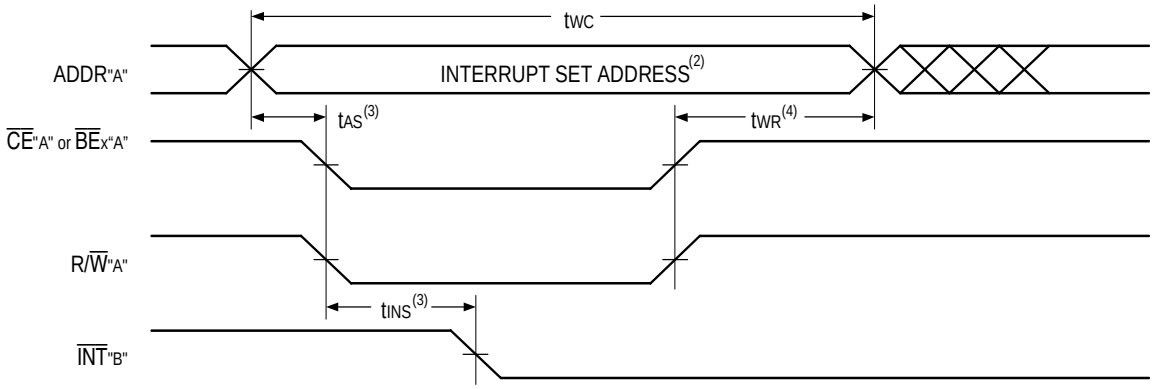
**NOTES:**
1. R/$\overline{W}$ or $\overline{CE}$ (or $\overline{BE}$x) = $V_{IH}$ during all address transitions.
2. A write occurs during the overlap ($t_{EW}$ or $t_{WP}$) of a $\overline{CE}$ (or $\overline{BE}$x) = $V_{IL}$ and a R/$\overline{W}$ = $V_{IL}$.
3. $t_{WR}$ is measured from the earlier of $\overline{CE}$ (or $\overline{BE}$x) or R/$\overline{W}$ = $V_{IH}$ to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ (or $\overline{BE}$x) LOW transition occurs simultaneously with or after the R/$\overline{W}$ = $V_{IL}$ transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$ (or $\overline{BE}$x) or R/$\overline{W}$.
7. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 3). This parameter is guaranteed but is not production tested.

## AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range

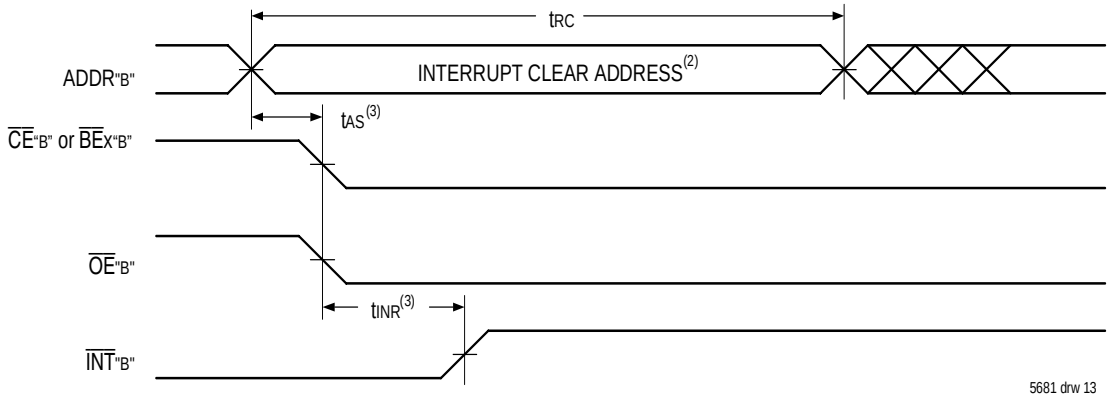
| | | 70X525X Ind'l Only | | |
|---|---|---|---|---|
| Symbol | Parameter | Min. | Max. | Unit |
| **INTERRUPT TIMING** | | | | |
| $t_{AS}$ | Address Set-up Time | 0 | — | ns |
| $t_{WR}$ | Write Recovery Time | 0 | — | ns |
| $t_{INS}$ | Interrupt Set Time | — | 45 | ns |
| $t_{INR}$ | Interrupt Reset Time | — | 45 | ns |

5681 tbl 12

## Waveform of Interrupt Timing(1)




5681 drw 12




5681 drw 13

**NOTES:**
1. If Port A is Port 1, Port B may be either Port 2 or Port 3. If Port A is either Port 2 or Port 3, Port B must be Port 1.
2. See Interrupt Truth Table II.
3. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
4. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is de-asserted first.

## Functional Description

The IDT70X525X provides three ports with separate control, address, and I/O pins that permit independent access for reads or writes to the two banks of memory. These devices have an automatic power down feature controlled by $\overline{BE}_0$ and $\overline{BE}_1$ on Port 1 and $\overline{CE}$ on Port 2 and Port 3. The $\overline{CE}$ (or $\overline{BE}_X$) controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ($\overline{CE}$ or $\overline{BE}_X$ = $V_{IH}$). When Port 1 is enabled, it has access to the full memory. When Port 2 is active it has access to Bank 1 of the memory. When Port 3 is active it has access to Bank 2 of the memory. See Truth Table I for a description of the Read/Write operation.

## Truth Table I – Read/Write Control

| | $\overline{BE}_0$ | $\overline{BE}_1$ | R/$\overline{W}$ | $\overline{CE}$ | $\overline{OE}$ | $D_0$-$D_{15}$ | Function |
|---|---|---|---|---|---|---|---|
| PORT 1 | H | H | X | X | X | Z | Port Deselected |
| | L | H | L | X | X | $DATA_{IN}$ | Data on port written into Memory Bank 0 |
| | L | H | H | X | L | $DATA_{OUT}$ | Data in Memory Bank 0 output on port |
| | H | L | L | X | X | $DATA_{IN}$ | Data on port written into Memory Bank 1 |
| | H | L | H | X | L | $DATA_{OUT}$ | Data in Memory Bank 1 output on port |
| | X | X | X | X | H | Z | Outputs Disabled |
| | L | L | X | X | X | X | Not Allowed |
| PORT 2 or PORT 3 | X | X | X | H | X | Z | Port Deselected |
| | X | X | L | L | X | $DATA_{IN}$ | Data on port written into Memory Bank(2) |
| | X | X | H | L | L | $DATA_{OUT}$ | Data in Memory Bank(2) output on port |
| | X | X | X | X | H | Z | Outputs Disabled |
| | H | H | X | H | X | Z | $\overline{BE}_0$ = $\overline{BE}_1$ = $\overline{CE}_{P3}$ = $V_{IH}$, Sleep mode |

5681 tbl 13

**NOTE:**
1. Both $\overline{BE}_0$, and $\overline{BE}_1$ cannot be active ($\overline{BE}x$ = $V_{IL}$) simultaneously.
2. Memory Bank 0 for Port 2. Memory Bank 1 for Port 3.

## Interrupts

If the user chooses the interrupt function, a memory location (mailbox or message center) is assigned to each port. Interrupt $\overline{INT}_{P1-P2}$ of Port 1 ($\overline{INT}_{P1-P2}$) is asserted when Port 2 writes to memory location FFE(HEX), where a write is defined as $\overline{CE} = R/\overline{W} = V_{IL}$ per Truth Table II. Port 1 clears the interrupt by accessing address location FFE when $\overline{BE}_0 = V_{IL}$, $R/\overline{W}$ is a "don't care". Interrupt $\overline{INT}_{P1-P3}$ of Port 1 ($\overline{INT}_{P1-P3}$) is asserted when Port 3 writes to memory location FFE (HEX), where a write is defined as $\overline{CE} = R/\overline{W} = V_{IL}$. Port 1 clears the interrupt by accessing address location FFE when $\overline{BE}_1 = V_{IL}$, $R/\overline{W}$ is a "don't care". Port 2's interrupt flag ($\overline{INT}_{P2-P1}$) is asserted when Port 1 writes to memory location FFF (HEX), where a write is defined as $\overline{BE}_0 = R/\overline{W} = V_{IL}$. Port 2 clears the interrupt by accessing address location FFF when $\overline{CE} = V_{IL}$, $R/\overline{W}$ is a "don't care". Likewise, Port 3's interrupt flag ($\overline{INT}_{P3-P1}$) is asserted when Port 1 writes to memory location FFF (HEX), where a write is defined as $\overline{BE}_1 = R/\overline{W} = V_{IL}$. Port 3 clears the interrupt by accessing address location FFF when $\overline{CE} = V_{IL}$, R/W is a "don't care".

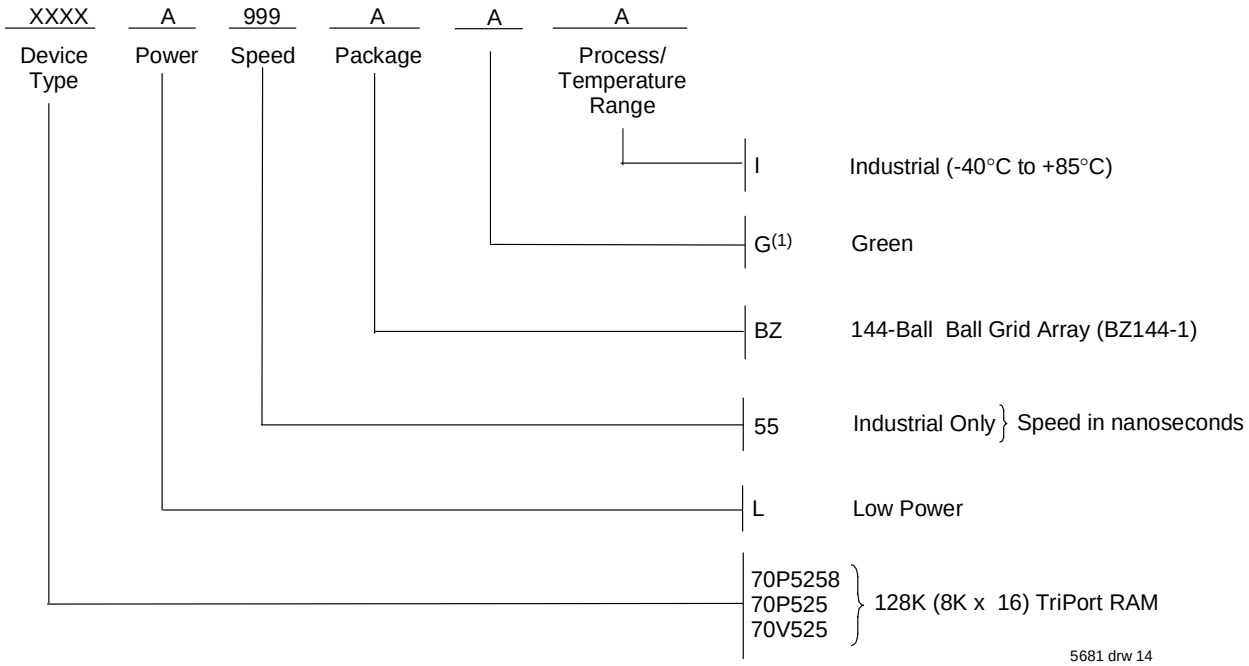
## Truth Table II - Interrupt Flag

| Port 1 | | | | | | | Port 2 or 3 | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $R/\overline{W}$ | $\overline{BE}_0$ | $\overline{BE}_1$ | $\overline{OE}$ | $A_{11} - A_0$ | $\overline{INT}_{P1-P2}$ | $\overline{INT}_{P1-P3}$ | $R/\overline{W}$ | $\overline{CE}$ | $\overline{OE}$ | $A_{11} - A_0$ | $\overline{INT}_{Px-P1}$ | Function |
| L | L | H | X | FFF | X | X | X | X | X | X | L | Set P2 $\overline{INT}$ Flag |
| X | X | X | X | X | X | X | X | L | L | FFF | H | Reset P2 $\overline{INT}$ Flag |
| L | H | L | X | FFF | X | X | X | X | X | X | L | Set P3 $\overline{INT}$ Flag |
| X | X | X | X | X | X | X | X | L | L | FFF | H | Reset P3 $\overline{INT}$ Flag |
| X | X | X | X | X | L | X | L | L | X | FFE | X | Set P1 $\overline{INT}_{P1-P2}$ Flag(1) |
| X | L | H | L | FFE | H | X | X | X | X | X | X | Reset P1 $\overline{INT}_{P1-P2}$ Flag |
| X | X | X | X | X | X | L | L | L | X | FFE | X | Set P1 $\overline{INT}_{P1-P3}$ Flag(2) |
| X | H | L | L | FFE | X | H | X | X | X | X | X | Reset P1 $\overline{INT}_{P1-P3}$ Flag |

5681 tbl 14

**NOTE:**
1. Port 2 sets the $\overline{INT}_{P1-P2}$ flag on Port 1 so all signals refer to Port 2.
2. Port 3 sets the $\overline{INT}_{P1-P3}$ flag on Port 1 so all signals refer to Port 3.

## Ordering Information




**NOTE:**
1. Green parts available. For specific speeds, packages and powers contact your sales office.

## Datasheet Document History

| | | |
|---|---|---|
| 10/14/03: | Initial datasheet | |
| 03/23/04: | Page 7 | Corrected $t_{OH}$ spec min to 5ns in AC Electrical Characteristics Table 10 |
| 5/26/05: | Page 1 | Added green availability to features |
| | Page 13 | Added green indicator to ordering information |
| | Page 1 & 13 | Replaced old logo ® with new ™ logo |
| 05/08/06: | Page 5 | Updated $V_{TERM}$ in Absolute Maximum Ratings table and added footnote 3 & 4 |
| 07/25/08: | Page 6 | Corrected a typo in the DC Chars table |
| 01/19/09: | Page 14 | Removed "IDT" from orderable part number |

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