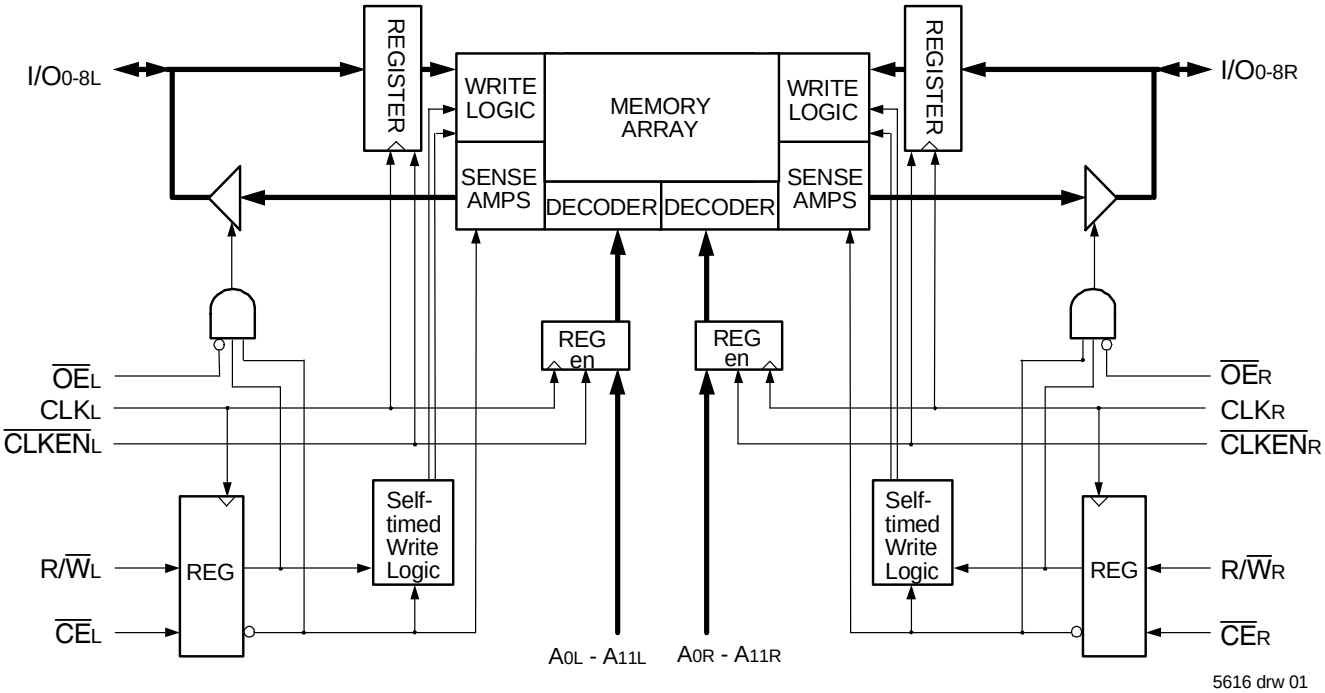
HIGH SPEED 3.3V (4K X 9) SYNCHRONOUS DUAL-PORT RAM

IDT70V914S

Features

- **High-speed clock-to-data output times**
  - *Commercial: 20/25ns (max.)*
  - *Industrial: 20/25ns (max.)*
- **Low-power operation**
  - *IDT70V914S*
    Active: 250 mW (typ.)
    Standby: 10 mW (typ.)
- **Architecture based on Dual-Port RAM cells**
  - *Allows full simultaneous access from both ports*
- **Synchronous operation**
  - *5ns setup to clock, 1ns hold on all control, data, and address inputs*
  - *Data input, address, and control registers*
  - *Fast 20ns clock to data out*
  - *Self-timed write allows fast cycle times*
  - *20ns cycle times, 50MHz operation*
- **LVTTL-compatible, single 3.3V (± 0.3V) power supply**
- **Clock Enable feature**
- **Guaranteed data output hold times**
- **Available in an 80-pin TQFP**
- **Industrial temperature range (-40°C to +85°C) is available**

Functional Block Diagram



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JANUARY 2009

Description

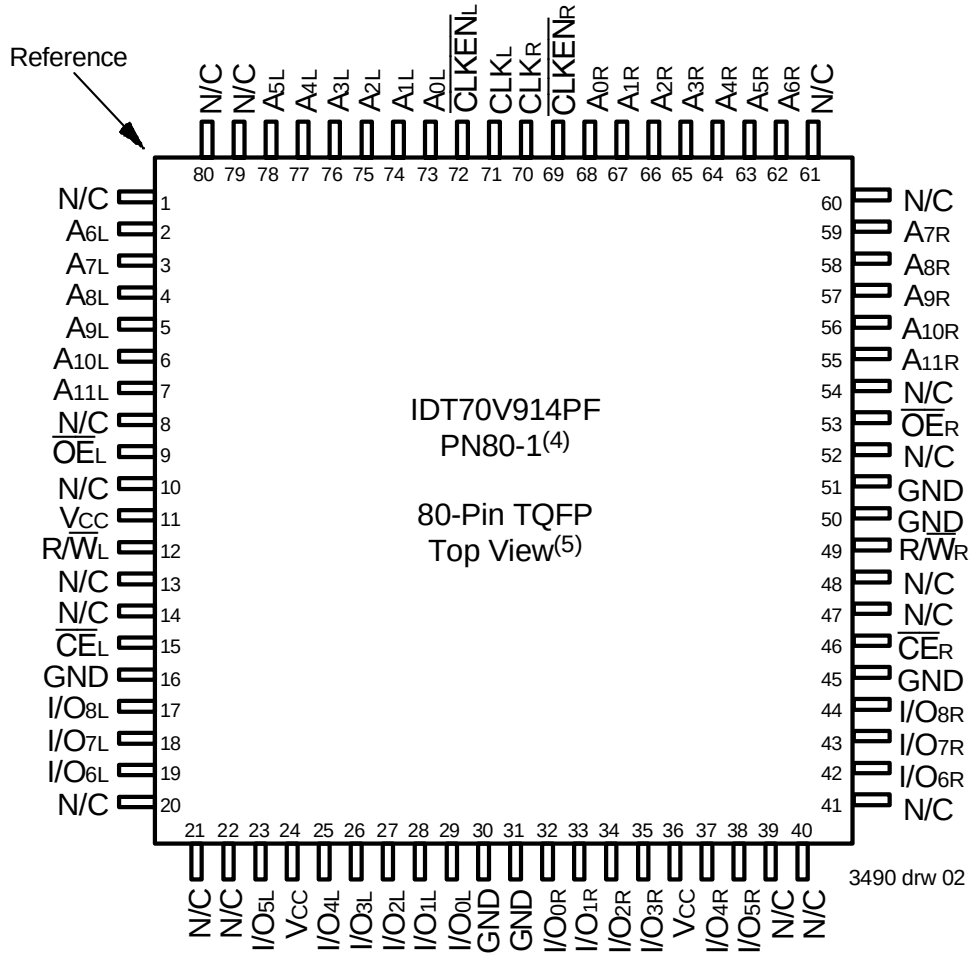
The IDT70V914 is a high-speed 4K x 9 bit synchronous Dual-Port RAM. The memory array is based on Dual-Port memory cells to allow simultaneous access from both ports. Registers on control, data, and address inputs provide low set-up and hold times. The timing latitude provided by this approach allow systems to be designed with very short cycle times. With an input data register, this device has been optimized for applications having unidirectional data flow or bi-directional data flow in bursts.

The IDT70V914 utilizes a 9-bit wide data path to allow for parity at the user's option. This feature is especially useful in data communication applications where it is necessary to use a parity bit for transmission/ reception error checking.

Fabricated using IDT's CMOS high-performance technology, these Dual-Ports typically operate on only 250mW of power at maximum high-speed clock-to-data output times as fast as 20ns. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

The IDT70V914 is packaged in an 80-pin TQFP.

Pin Configurations[1,2,3]



NOTES:
1. All V_{CC} pins must be connected to power supply.
2. All ground pins must be connected to ground supply.
3. Package body is approximately 14mm x 14mm x 1.4mm.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
V_{TERM}(2)	Terminal Voltage	-0.5 to V_{CC}	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
I_{OUT}	DC Output Current	50	mA

5616 tbl 01

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of $V_{TERM} \geq V_{CC}$ + 10%.

Capacitance

(T_A = +25°C, f = 1.0MHz) TQFP Only

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	9	pF

5616 tbl 04

NOTES:
1. These parameters are determined by device characterization, but are not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.

Maximum Operating Temperature and Supply Voltage(1,2)

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	3.3V ± 0.3
Industrial	-40°C to +85°C	0V	3.3V ± 0.3

5616 tbl 02

NOTES:
1. This is the parameter T_A. This is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	V_{CC}+0.3(2)	V
V_{IL}	Input Low Voltage	-0.3(1)	—	0.8	V

5616 tbl 03

NOTES:
1. $V_{IL} \geq$ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed V_{CC} + 0.3V.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{CC} = 3.3V ± 0.3)

Symbol	Parameter	Test Conditions	70V914S		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current(1)	V_{CC} = 3.6V, V_{IN} = 0V to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = +4mA	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	V

5616 tbl 05

NOTE:
1. At $V_{CC} \leq$ 2.0V, input leakages are undefined

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[4] (V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	Version	70V914S20 Com'l & Ind		70V914S25 Com'l & Ind		Unit
				Typ.[2]	Max.	Typ.[2]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IL}, Outputs Disabled f = f_{MAX}[1]	COM'L	80	140	75	130	mA
			IND	80	200	75	190	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IH} f = f_{MAX}[1]	COM'L	30	55	25	50	mA
			IND	30	85	25	80	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}[3] Active Port Outputs Disabled, f=f_{MAX}[1]	COM'L	55	85	45	80	mA
			IND	55	100	45	95	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE}_R$ and $\overline{CE}_L \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V, f = 0[2]	COM'L	3	15	3	15	mA
			IND	3	15	3	15	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	$\overline{CE}_{"A"} \leq$ 0.2V and $\overline{CE}_{"B"} \geq V_{CC}$ - 0.2V[3] $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V, Active Port Outputs Disabled f = f_{MAX}[1]	COM'L	55	85	45	80	mA
			IND	55	100	45	95	

5616 tbl 06

NOTES:

1. At f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/t_{CYC}, using "AC TEST CONDITIONS" at input levels of GND to 3V.
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
4. V_{CC} = 3.3V, T_A = 25°C for Typ, and are not production tested. $I_{CC\,DC}$ = 150mA (Typ).

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1,2 and 3

5616 tbl 07

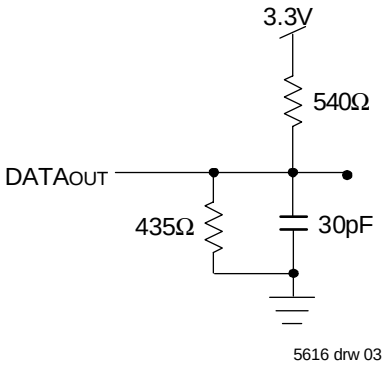


Figure 1. AC Output Test load.

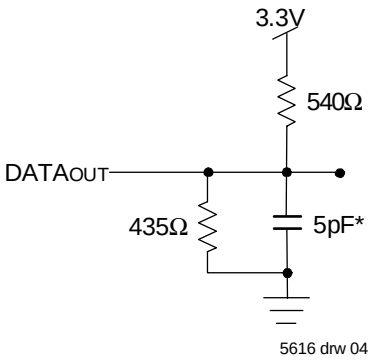


Figure 2. Output Test Load
(For t_{CKLZ}, t_{CKHZ}, t_{OLZ}, and t_{OHZ})
*Including scope and jig.

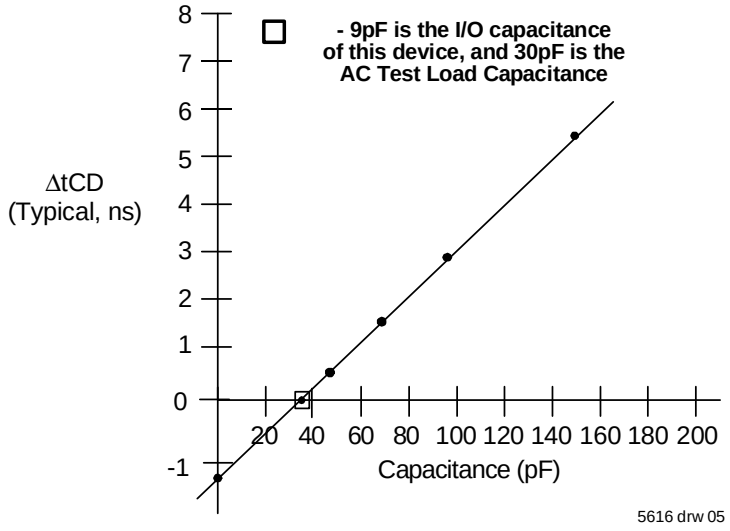


Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)

(Commercial: Vcc = 3.3V ± 0.3V)

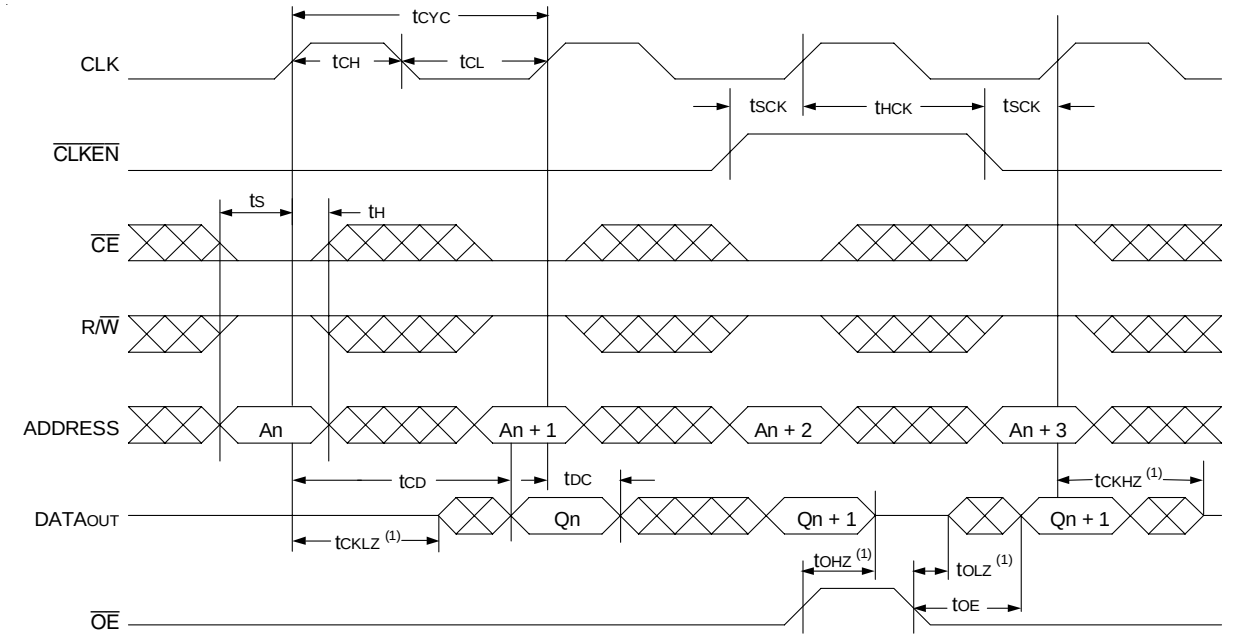
Symbol	Parameter	70914S20 Com'l & Ind		70914S25 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	20	—	25	—	ns
t_{CH}	Clock High Time	8	—	10	—	ns
t_{CL}	Clock Low Time	8	—	10	—	ns
t_{CD}	Clock High to Output Valid	—	20	—	25	ns
t_S	Registered Signal Set-up Time	5	—	6	—	ns
t_H	Registered Signal Hold Time	1	—	1	—	ns
t_{DC}	Data Output Hold After Clock High	3	—	3	—	ns
t_{CKLZ}	Clock High to Output Low-Z[1,2]	2	—	2	—	ns
t_{CKHZ}	Clock High to Output High-Z[1,2]	—	9	—	12	ns
t_{OE}	Output Enable to Output Valid	—	10	—	12	ns
t_{OLZ}	Output Enable to Output Low-Z[1,2]	0	—	0	—	ns
t_{OHZ}	Output Disable to Output High-Z[1,2]	—	9	—	11	ns
t_{SCK}	Clock Enable, Disable Set-up Time	5	—	6	—	ns
t_{HCK}	Clock Enable, Disable Hold Time	2	—	2	—	ns
Port-to-Port Delay						
t_{CWDD}	Write Port Clock High to Read Data Delay	—	35	—	45	ns
t_{CSS}	Clock-to-Clock Setup Time	—	15	—	20	ns

5616 tbl 08

NOTES:

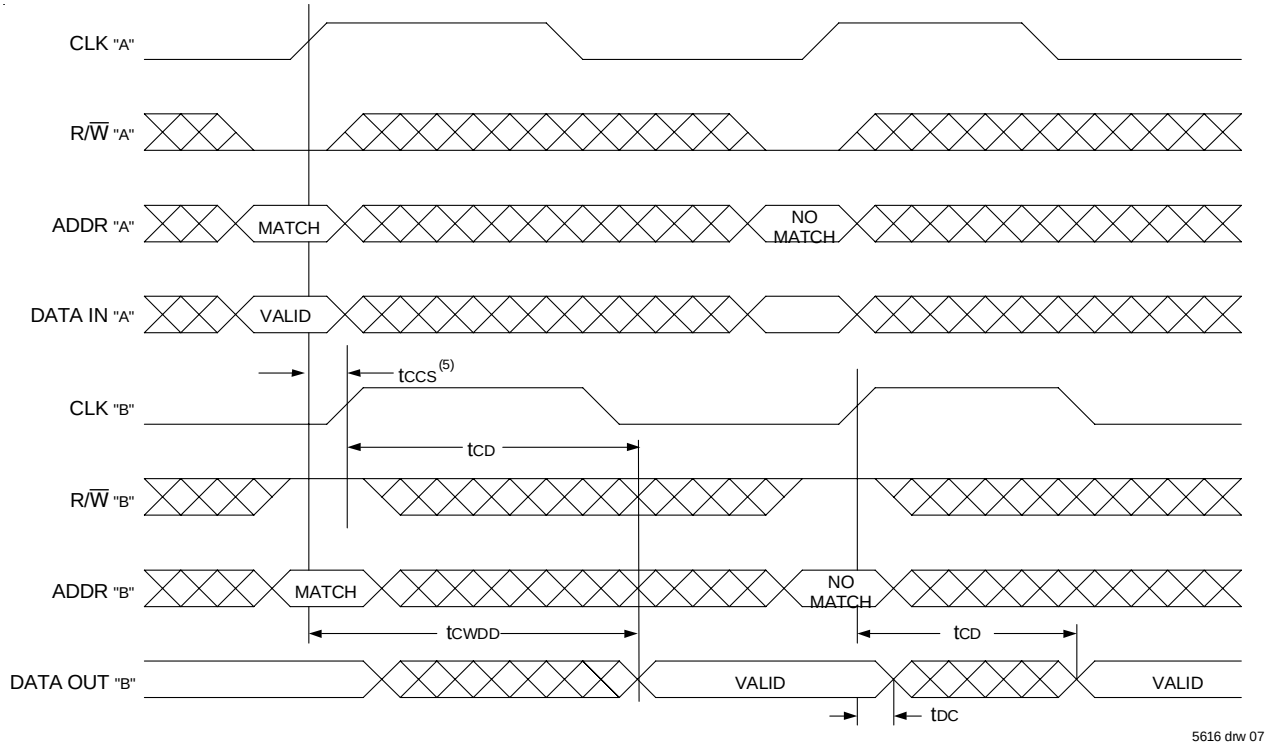
1. Transition is measured 0mV from Low or High impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.

Timing Waveform of Read Cycle, Either Side



5616 drw 06

Timing Waveform of Write with Port-to-Port Read(2,3,4)

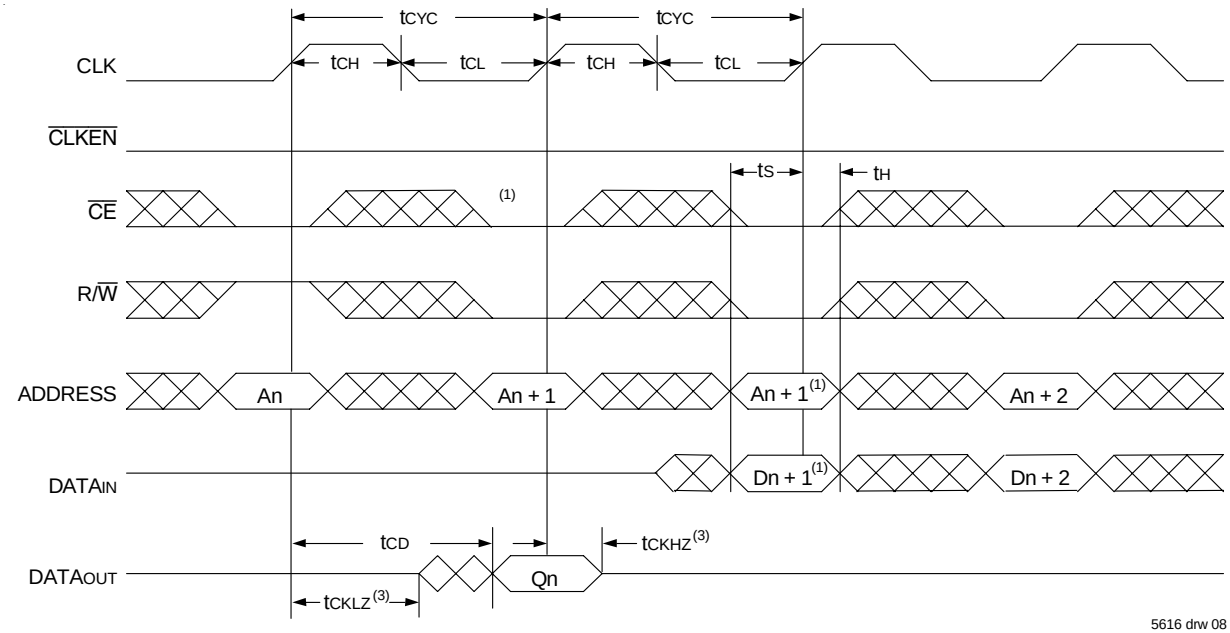


5616 drw 07

NOTES:

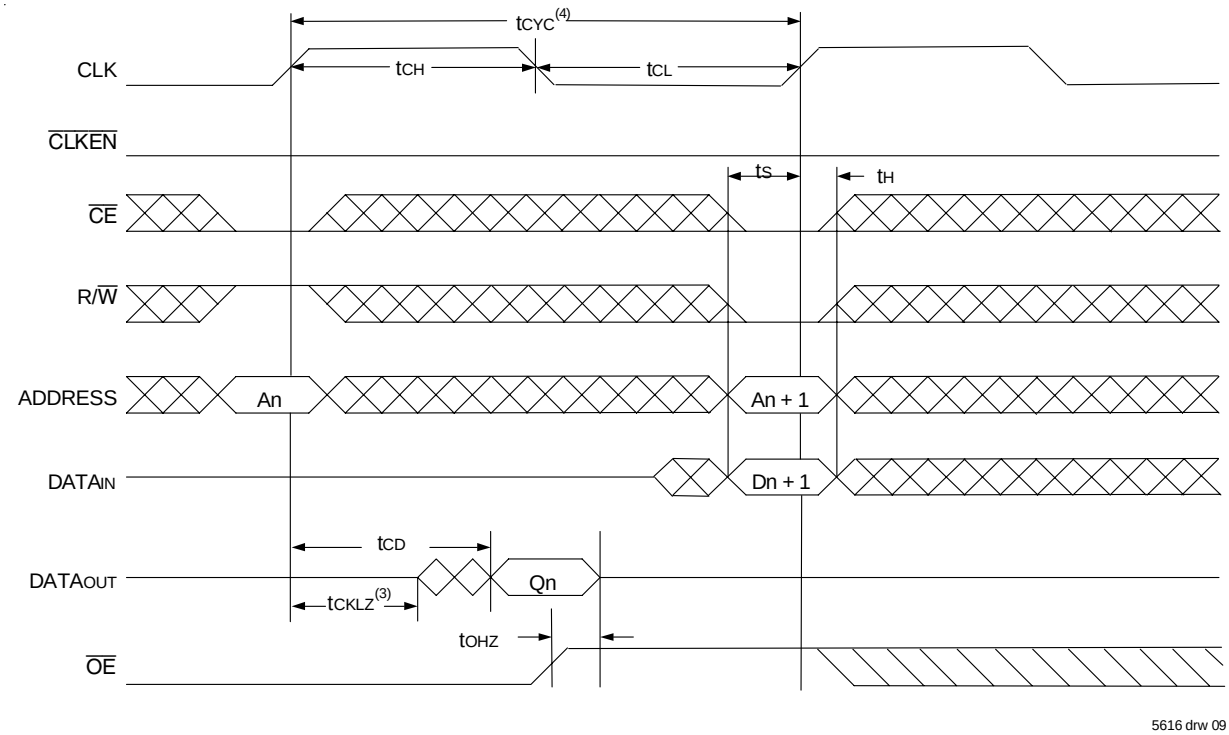
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. $\overline{CE}_L = \overline{CE}_R = V_{IL}$, $\overline{CLKEN}_L = \overline{CLKEN}_R = V_{IL}$.
3. $\overline{OE} = V_{IL}$ for the reading port, port 'B'.
4. All timing is the same for left and right ports. Ports "A" may be either the left or right port. Port "B" is opposite from port "A".
5. If $t_{CCS} \leq$ maximum specified, then data from right port READ is not valid until the maximum specified for t_{CWDD}.
   If t_{CCS} > maximum specified, then data from right port READ is not valid until $t_{CCS} + t_{CD}$. t_{CWDD} does not apply in this case.

Timing Waveform of Read-to-Write Cycle No. 1(1,2) (tCYC = min.)



5616 drw 08

Timing Waveform of Read-to-Write Cycle No. 2(4) (tCYC > min.)



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NOTES:

1. For tCYC = min.; data out coincident with the rising edge of the subsequent write clock can occur. To ensure writing to the correct address location, the write must be repeated on the second write clock rising edge. If $\overline{CE}$ = VIL, invalid data will be written into array. The An+1 must be rewritten on the following cycle.
2. $\overline{OE}$ LOW throughout.
3. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
4. For tCYC > min.; $\overline{OE}$ may be used to avoid data out coincident with the rising edge of the subsequent write clock. Use of $\overline{OE}$ will eliminate the need for the write to be repeated.

Functional Description

The IDT70V914 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide very short set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal. An asynchronous output enable is provided to ease asynchronous bus interfacing.

The internal write pulse width is dependent on the LOW to HIGH transitions of the clock signal allowing the shortest possible realized cycle times. Clock enable inputs are provided to stall the operation of the address and data input registers without introducing clock skew for very fast interleaved memory applications.

A HIGH on the $\overline{CE}$ input for one clock cycle will power down the internal circuitry to reduce static power consumption.

Truth Table I: Read/Write Control(1)

Inputs				Outputs	Mode
Synchronous(3)			Asynchronous		
CLK	$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	I/O0-8	
↑	H	X	X	High-Z	Deselected, Power-Down
↑	L	L	X	DATAIN	Selected and Write Enabled
↑	L	H	L	DATAOUT	Read Selected and Data Output Enable Read
↑	X	X	H	High-Z	Outputs Disabled

5616 tbl 09

Truth Table II: Clock Enable Function Table(1)

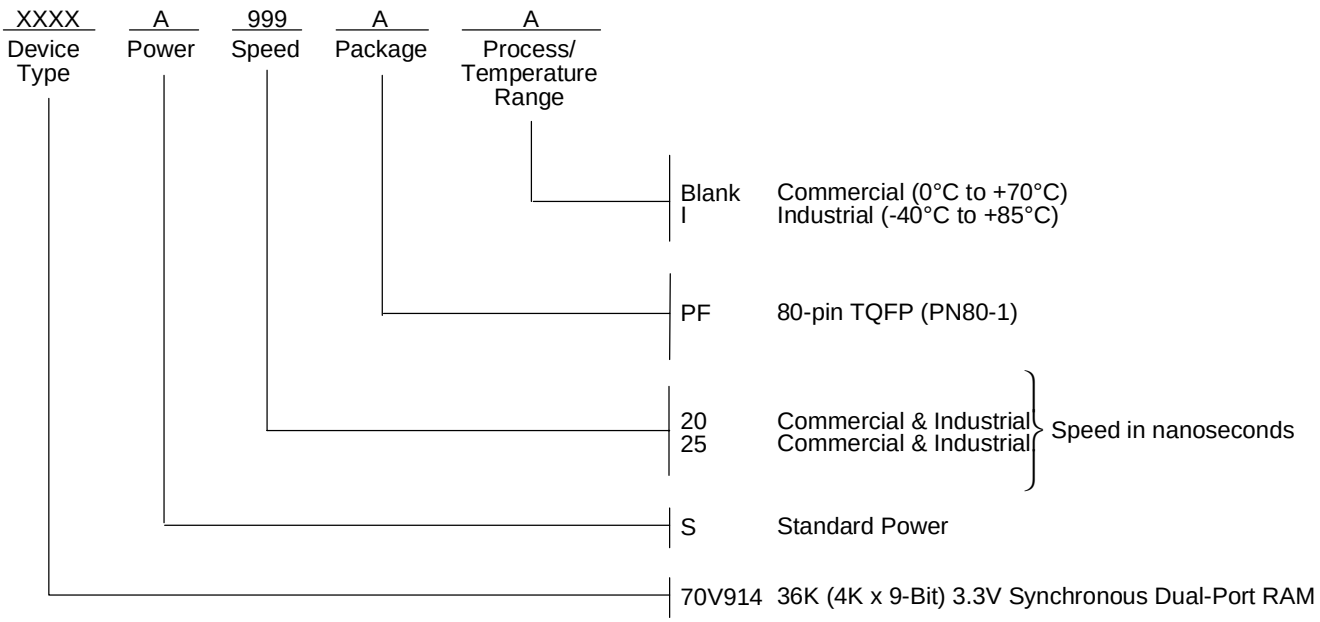
Mode	Inputs		Register Inputs		Register Outputs(4)	
	CLK(3)	$\overline{CLKEN}$(2)	ADDR	DATAIN	ADDR	DATAOUT
Load "1"	↑	L	H	H	H	H
Load "0"	↑	L	L	L	L	L
Hold (do nothing)	↑	H	X	X	NC	NC
	X	H	X	X	NC	NC

5616 tbl 10

NOTES:

1. 'H' = HIGH voltage level steady state, 'h' = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition, 'L' = LOW voltage level steady state 'l' = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition, 'X' = Don't care, 'NC' = No change
2. $\overline{CLKEN}$ = VIL must be clocked in during Power-Up.
3. Control signals are initialted and terminated on the rising edge of the CLK, depending on their input level. When R/$\overline{W}$ and $\overline{CE}$ are LOW, a write cycle is initiated on the LOW-to-HIGH transition of the CLK. Termination of a write cycle is done on the next LOW-to-HIGH transistion of the CLK.
4. The register outputs are internal signals from the register inputs being clocked in or disabled by $\overline{CLKEN}$.

Ordering Information



5616 drw 10

Datasheet Document History

1/20/00:	Initial Public Offering	
1/10/01:	Page 1	Fixed A_L and A_R numbers in drawing
	Page 4	Increased storage temperature parameter
		Clarified T_A parameter
	Page 5	DC Electrical parameters–changed wording from "open" to "disabled"
	Changed ±200mV to 0mV in notes	
01/29/09:	Page 10	Removed "IDT" from orderable part number

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