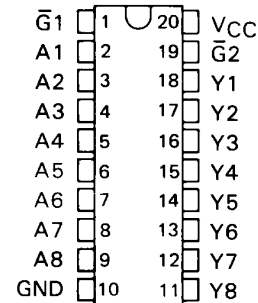


SN54ALS2540, SN54ALS2541, SN74ALS2540, SN74ALS2541 OCTAL LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

JUNE 1984—REVISED MAY 1986

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce DC Loading
- Outputs Have 25-Ω Series Resistor, So No External Resistors are Required
- Package Options Include Plastic "Small Outline" Packages, Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS2540, SN54ALS2541 . . . J PACKAGE
SN74ALS2540, SN74ALS2541 . . . DW OR N PACKAGE
(TOP VIEW)



description

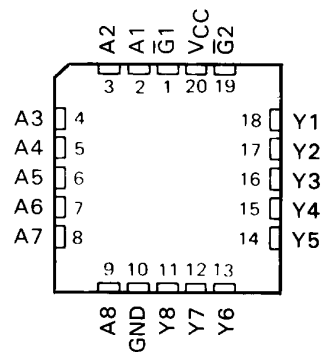
These octal buffers and line drivers are designed to drive capacitive input characteristics of MOS devices and have the performance of the popular SN54ALS240A/SN74ALS240A series. At the same time, they offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed-circuit-board layout.

The three-state control gate is a 2-input AND with active-low inputs such that if either $\bar{G}1$ or $\bar{G}2$ is high, all eight outputs are in the high-impedance state.

The 'ALS2540 offers inverting data and the 'ALS2541 offers true data at the outputs.

The SN54ALS' is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS' is characterized for operation from 0°C to 70°C .

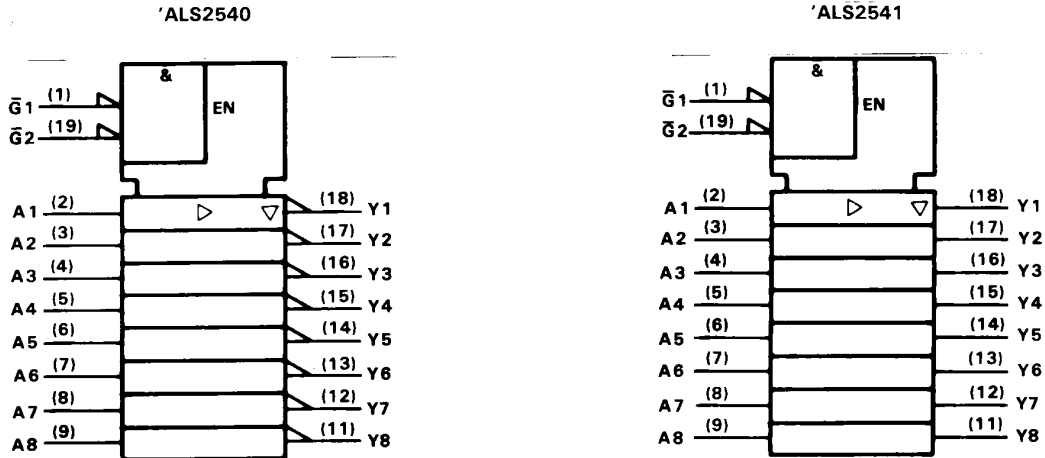
SN54ALS2540, SN54ALS2541 . . . FK PACKAGE
(TOP VIEW)



SN54ALS2540, SN54ALS2541, SN74ALS2540, SN74ALS2541 OCTAL LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

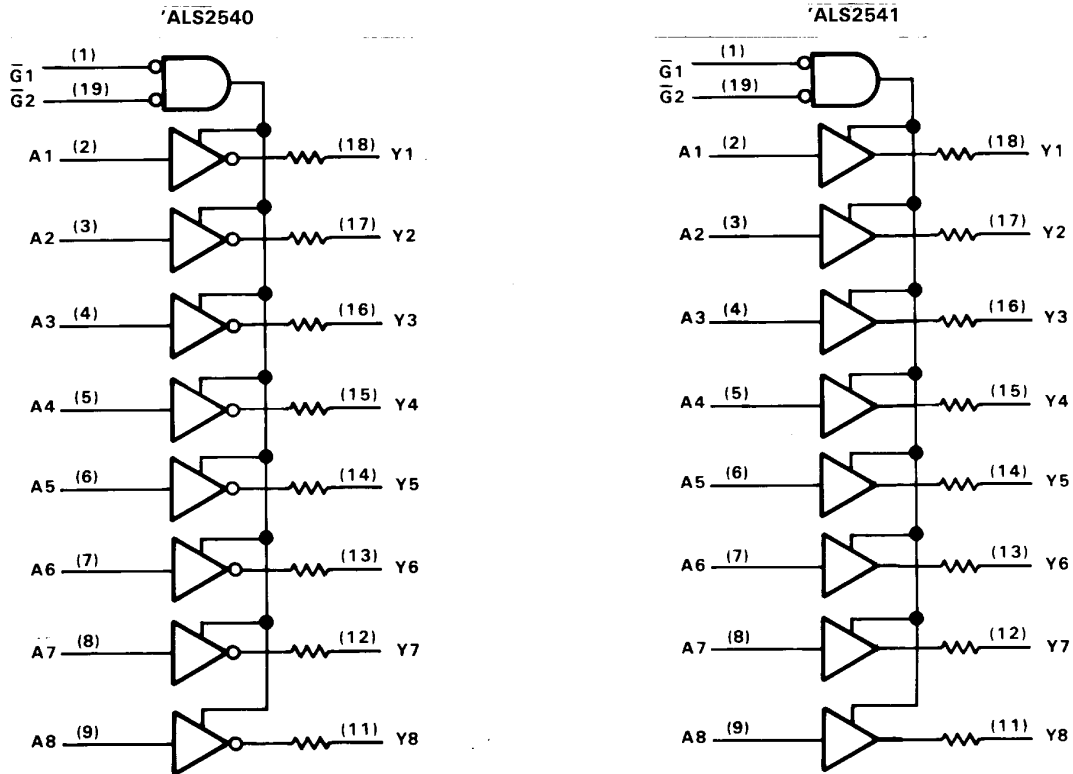
JUNE 1984—REVISED MAY 1986

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



All output resistors are 25 Ω .

SN54ALS2540, SN54ALS2541, SN74ALS2540, SN74ALS2541 OCTAL LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

JUNE 1984—REVISED MAY 1986

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range: SN54ALS2540, SN54ALS2541	-55°C to 125°C
SN74ALS2540, SN74ALS2541	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54ALS2540			SN74ALS2540			UNIT
		SN54ALS2541			SN74ALS2541			
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-0.4			-0.4	mA
I_{OL}	Low-level output current			12			12	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS2540			SN74ALS2540			UNIT
		SN54ALS2541			SN74ALS2541			
		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, $I_{OH} = -0.4\text{ mA}$	$V_{CC}-2$			$V_{CC}-2$			V
V_{OL}	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 1\text{ mA}$		0.15	0.5		0.15	0.5	V
	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 12\text{ mA}$		0.35	0.8		0.35	0.8	
I_{OZH}	$V_{CC} = 5.5\text{ V}$, $V_O = 2.7\text{ V}$			20			20	μA
I_{OZL}	$V_{CC} = 5.5\text{ V}$, $V_O = 0.4\text{ V}$			-20			-20	μA
I_{OH}	$V_{CC} = 4.5\text{ V}$, $V_O = 2\text{ V}$	-15			-15			mA
I_{OL}	$V_{CC} = 4.5\text{ V}$, $V_O = 2\text{ V}$	30			30			mA
I_I	$V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$			20			20	μA
I_{IL}	$V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$			-0.1			-0.1	mA
$I_{O\ddagger}$	$V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$	-15		-70	-15		-70	mA
I_{CC}	'ALS2540	$V_{CC} = 5.5\text{ V}$	Outputs high	5	10	5	10	mA
			Outputs low	13	22	13	22	
			Outputs disabled	11	19	11	19	
	'ALS2541	$V_{CC} = 5.5\text{ V}$	Outputs high	6	14	6	14	mA
			Outputs low	15	25	15	25	
			Outputs disabled	13.5	22	13.5	22	

[†]All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

SN54ALS2540, SN54ALS2541, SN74ALS2540, SN74ALS2541 OCTAL LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

JUNE 1984 – REVISED MAY 1986

'ALS2540 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = 25°C		V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX		UNIT		
			'ALS2540		SN54ALS2540			SN74ALS2540	
			TYP		MIN	MAX		MIN	MAX
t _{PLH}	A	Y	7.5	2	14	2	12	ns	
t _{PHL}			5.6	2	13	2	11		
t _{PZH}	\bar{G}	Y	9	5	18	5	15	ns	
t _{PZL}			12.6	8	24	8	20		
t _{PHZ}	\bar{G}	Y	4	1	12	1	10	ns	
t _{PLZ}			7	2	14	2	12		

'ALS2541 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = 25°C		V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX		UNIT		
			'ALS2541		SN54ALS2541			SN74ALS2541	
			TYP		MIN	MAX		MIN	MAX
t _{PLH}	A	Y	8.7	2	17	2	15	ns	
t _{PHL}			7	2	14	2	12		
t _{PZH}	\bar{G}	Y	9	5	18	5	15	ns	
t _{PZL}			12.6	8	24	8	20		
t _{PHZ}	\bar{G}	Y	4	1	12	1	10	ns	
t _{PLZ}			7	2	14	2	12		

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74ALS2540N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	Samples Not Available

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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