

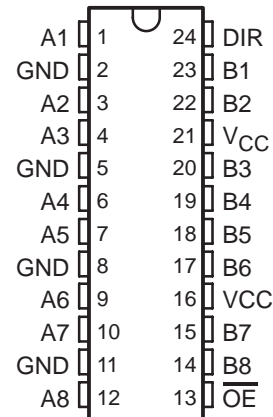
SN74BCT25642

25-Ω OCTAL BUS TRANSCEIVER

SCBS047C – DECEMBER 1989 – REVISED NOVEMBER 1993

- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)**
- **Designed to Facilitate Incident-Wave Switching for Line Impedances of 25 Ω or Greater**
- **Distributed V_{CC} and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs**
- **The A Port Features Open-Collector Outputs That Provide 188-mA I_{OL} to Allow for Heavy DC Loading on Open-Collector Outputs**
- **Eliminates Need for 3-State Overlap Protection on A Ports**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic 300-mil DIPs (NT)**

**DW OR NT PACKAGE
(TOP VIEW)**



description

This 25-Ω octal bus transceiver is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.

The SN74BCT25642 is capable of sinking 188-mA I_{OL} (A port), which facilitates switching 25-Ω transmission lines on the incident wave. It is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented transceivers. The distributed V_{CC} and GND pins minimize the noise generated by the simultaneous switching of the outputs.

The SN74BCT25642 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

| INPUTS | | OPERATION |
|-----------------|-----|------------------------------|
| \overline{OE} | DIR | |
| L | L | \overline{B} data to A bus |
| L | H | \overline{A} data to B bus |
| H | X | Isolation |

recommended operating conditions (see Note 2)

| | | MIN | NOM | MAX | UNIT |
|-----------------|--------------------------------|-----|-----|-----|------|
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | V |
| V _{IH} | High-level input voltage | 2 | | | V |
| V _{IL} | Low-level input voltage | | | 0.8 | V |
| V _{OH} | High-level output voltage | | | 5.5 | V |
| I _{IK} | Input clamp current | | | -18 | mA |
| I _{OH} | High-level output current | | | -3 | mA |
| I _{OL} | Low-level output current | | | 188 | mA |
| | | | | 24 | |
| T _A | Operating free-air temperature | 0 | | 70 | °C |

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|-------------------|-------------------------|---------------------------|---------------------------------|-----|------|------|------|
| V _{IK} | | V _{CC} = 4.5 V, | I _I = -18 mA | | | -1.2 | V |
| V _{OH} | Any B | V _{CC} = 4.75 V, | I _{OH} = -1 mA | 2.7 | | | V |
| | | V _{CC} = 4.5 V, | I _{OH} = -3 mA | 2.4 | 3.3 | | |
| V _{OL} | Any A | V _{CC} = 4.5 V | I _{OL} = 94 mA | | 0.42 | 0.55 | V |
| | | | I _{OL} = 188 mA | | | 0.7 | |
| | Any B | V _{CC} = 4.5 V, | I _{OL} = 24 mA | | 0.35 | 0.5 | |
| I _{OH} | Any A | V _{CC} = 4.5 V, | V _{OH} = 5.5 V | | | 0.1 | mA |
| I _I | A and B | V _{CC} = 5.5 V, | V _I = 5.5 V | | | 0.25 | mA |
| | DIR and \overline{OE} | | | | | 0.1 | |
| I _{IH} ‡ | A and B | V _{CC} = 5.5 V, | V _I = 2.7 V | | | 70 | μA |
| | DIR and \overline{OE} | | | | | 20 | |
| I _{IL} ‡ | A and B | V _{CC} = 5.5 V, | V _I = 0.5 V | | | -0.6 | mA |
| | DIR and \overline{OE} | | | | | -0.6 | |
| I _{OS} § | Any B | V _{CC} = 5.5 V, | V _O = 0 | -60 | | -150 | mA |
| I _{CCL} | A to B | V _{CC} = 5.5 V | | | 40 | 64 | mA |
| | B to A | | | | 78 | 125 | |
| I _{CCH} | A to B | V _{CC} = 5.5 V | | | 25 | 40 | mA |
| | B to A | | | | 34 | 55 | |
| I _{CCZ} | A to B | V _{CC} = 5.5 V | | | 7.6 | 13 | mA |
| C _i | Control inputs | V _{CC} = 5 V, | V _O = 2.5 V or 0.5 V | | | 8 | pF |
| C _{io} | A port | V _{CC} = 5 V, | V _I = 2.5 V or 0.5 V | | | 15 | pF |
| | B port | | | | | 8 | |

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed 10 ms.



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 5$ V, $T_A = 25^\circ$ C | | | $R1 = 500 \Omega^\dagger$, $R2 = 500 \Omega$ | | UNIT |
|-----------|-----------------|----------------|---------------------------------------|-----|------|--|------|------|
| | | | MIN | TYP | MAX | MIN | MAX | |
| t_{PLH} | A | B | 0.8 | 3.2 | 6 | 0.8 | 6.2 | ns |
| t_{PHL} | | | 0.5 | 2 | 3.9 | 0.5 | 4 | |
| t_{PLH} | B | A | 1.5 | 3.2 | 5.7 | 1.5 | 6.3 | ns |
| t_{PHL} | | | 1.7 | 4.5 | 4.8 | 1.7 | 5.9 | |
| t_{PLH} | \overline{OE} | A | 2.8 | 5.5 | 10.4 | 2.8 | 11.6 | ns |
| t_{PHL} | | | 4.6 | 8.6 | 11.3 | 4.6 | 11.3 | |
| t_{PZH} | \overline{OE} | B | 3.3 | 5.7 | 8.1 | 3.3 | 9.1 | ns |
| t_{PZL} | | | 3.8 | 6.6 | 8.8 | 3.8 | 9.8 | |
| t_{PHZ} | \overline{OE} | B | 1.8 | 4.6 | 7 | 1.8 | 7.3 | ns |
| t_{PLZ} | | | 1.4 | 4.3 | 6.7 | 1.4 | 7.3 | |

† For A port, $R1 = 100 \Omega$.

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|-------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74BCT25642DW | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74BCT25642DWE4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74BCT25642DWG4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74BCT25642DWR | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74BCT25642DWRE4 | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74BCT25642DWRG4 | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74BCT25642NT | ACTIVE | PDIP | NT | 24 | 15 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74BCT25642NTE4 | ACTIVE | PDIP | NT | 24 | 15 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74BCT25642DWR | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74BCT25642DWR | SOIC | DW | 24 | 2000 | 346.0 | 346.0 | 41.0 |

NT (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

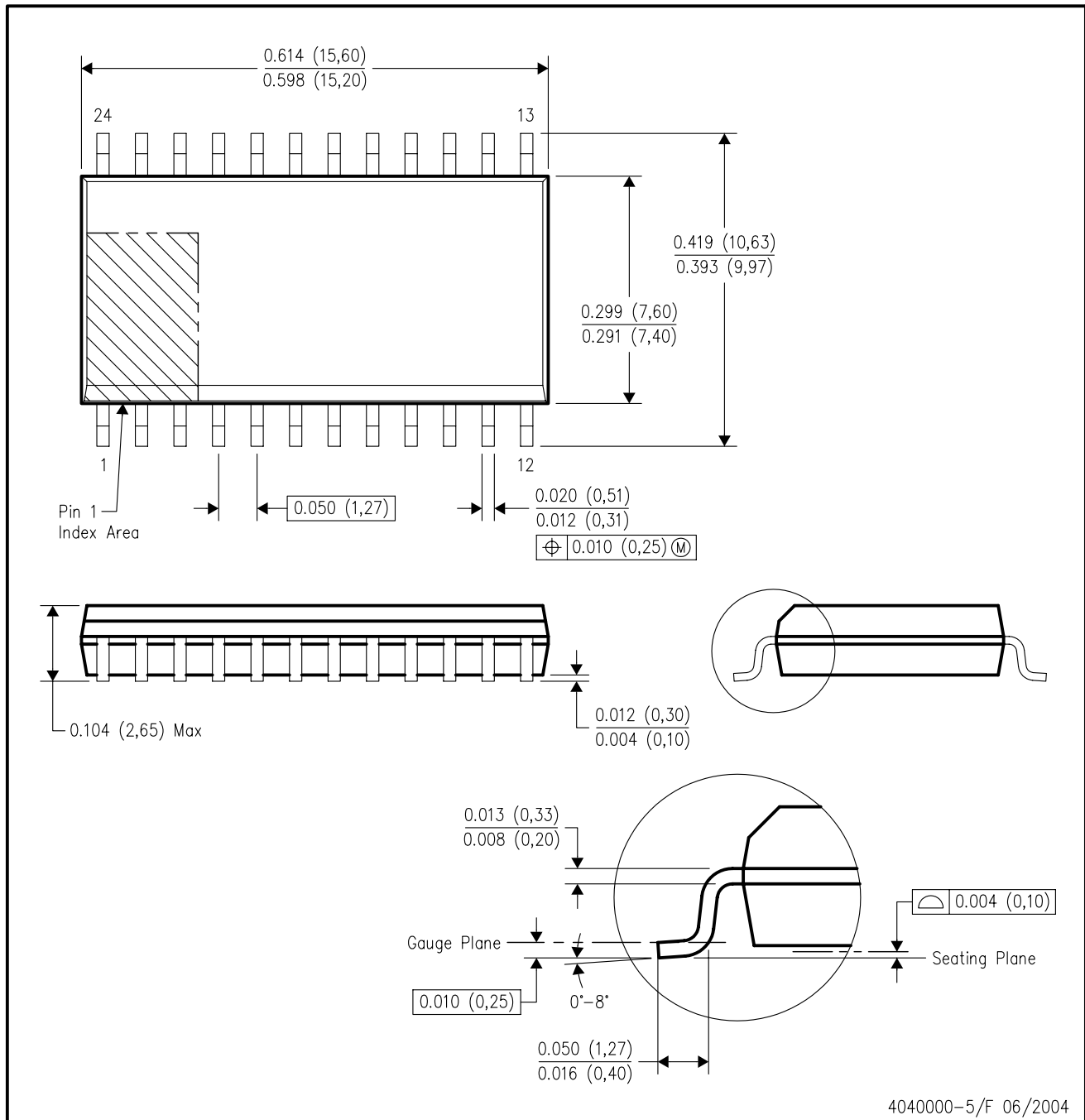
24 PINS SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

DW (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

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